TH1520 Video Input User Manual

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Figures & Tables

List of Abbreviations

Abbreviations	Full Spelling	Chinese Explanation
CSI	Camera Serial Interface	相机串行接口
DPCC	Defect Pixel Cluster Correction	坏点簇纠正
HDR	High Dynamic Range	高动态范围
IPI	Image Pixel Interface	图像像素接口
ISP	Image Signal Processor	图像信号处理器
LSC	Lens Shade Correction	镜头阴影矫正
MIPI	Mobile Industry Processor Interface	移动产业处理器接口
WDR	Wide Dynamic Range	宽动态范围
3A	Auto Focus, Auto White Balance, Auto Exposure	自动对焦、自动白平衡、自动曝光
3DNR	3D Noise Reduction	3D 降噪

1 MIPI CSI

1.1 Overview

The chip has two MIPI CSI modules named CSI2 and CSI2X2. The CSI2 module is composed of a 4 lane MIPI CSI host controller and a 4lane D-PHY RX. The CSI2X2 module is composed of one 4lane MIPI CSI host controller, one 2lane MIPI CSI host controller and two 2lane D-PHY RX which can be configured to aggregated mode or non-aggregated mode.
The CSI2 and CSI2X2 functional block diagrams are shown in Figure & Table 1-1and Figure & Table 1-2.

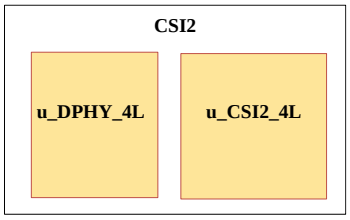


Figure & Table 1-1 CSI2 functional block diagram

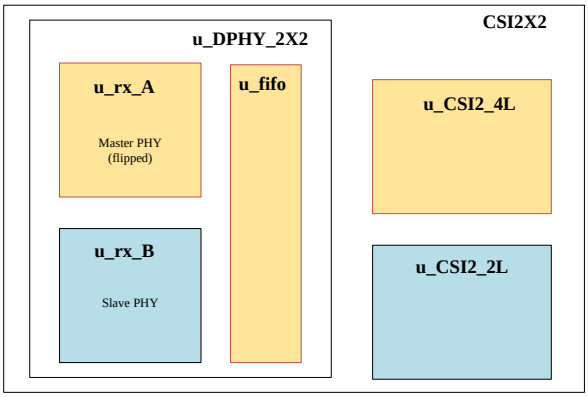


Figure & Table 1-2 CSI2X2 functional block diagram

The MIPI CSI host controller follows MIPI Alliance Specification *MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2), Version 1.2, January 2014*, providing a PPI interface compatible with MIPI Alliance standards with the PHY docking end. The pixel output terminal provides 3 Image Pixel Interfaces (IPIs) for image data transmission of multiple virtual channels, at the same time the controller provides standard AMBA APB2.0 interface for the control of MIPI CSI controller and D-PHY.
The D-PHY RX follows MIPI Alliance Specification *MIPI Alliance Specification for D-PHY, Version 1.2, September 2014*. The D-PHY RX has up to 4 data lanes, and the maximum rate of each data lane is 2.5Gbps, providing PPI interface compatible with MIPI Alliance standards to interface with external MIPI controllers.

1.2 Main Features

The CSI2's controller is the same as the CSI2X2's 4lane controller, which can work up to 4lane mode. The CSI2X2's 2lane controller can work up to 2lane mode. The three controllers all have the following features:

- Compliant with MIPI Alliance standards
- Three IPI ports for WDR scene requirement
- Supports up to 13MP@30fps or 8MP@60fps input sensor pixel data
- Supports a variety of bpp of RAW image input, such as 8/10/12/16 bpp
- Dynamically configurable multi-lane merging
- Long and short packet decoding
- Timing accurate signaling of frame and line synchronization packets
- Several frame format
  - General frame or digital interlaced video with or without accurate sync timing
  - Data type and virtual channel interleaving
- Error detection and correction: PHY level\Packet level\Line level\Frame level

The CSI2's RX D-PHY has the following features:

- Compliant with MIPI Alliance standards
- Up to 4 D-PHY RX data lanes
- Up to 2.5Gbps per lane

The CSI2X2's RX D-PHY is composed of A PHY and B PHY, the two PHYs have the following features:

- Compliant with MIPI Alliance standards
- A PHY and B PHY each have up to 4 D-PHY RX data lanes
- Up to 2.5Gbps per lane
- A PHY and B PHY can work independently in 2lane non-aggregated mode or 4lane aggregate mode

1.3 Interface

Figure & Table 1-3 Pin description table

Pin Name	Direction	Width	Description
MIPI_CSI_REXT	IO	1	Reference resistor connection PAD
MIPI_CSI_CLKP	IO	1	Positive D-PHY differential clock line
MIPI_CSI_CLKN	IO	1	Negative D-PHY differential clock line
MIPI_CSI_DATAP0	IO	1	Positive D-PHY differential data line
MIPI_CSI_DATAN0	IO	1	Negative D-PHY differential data line
MIPI_CSI_DATAP1	IO	1	Positive D-PHY differential data line
MIPI_CSI_DATAN1	IO	1	Negative D-PHY differential data line

Pin Name	Direction	Width	Description
MIPI_CSI_DATAP2	IO	1	Positive D-PHY differential data line
MIPI_CSI_DATAN2	IO	1	Negative D-PHY differential data line
MIPI_CSI_DATAP3	IO	1	Positive D-PHY differential data line
MIPI_CSI_DATAN3	IO	1	Negative D-PHY differential data line
MIPI_CSI2X2_A_REXT	IO	1	Reference resistor connection PAD
MIPI_CSI2X2_A_CLKP	IO	1	Positive D-PHY differential clock line
MIPI_CSI2X2_A_CLKN	IO	1	Negative D-PHY differential clock line
MIPI_CSI2X2_A_DATAP0	IO	1	Positive D-PHY differential data line
MIPI_CSI2X2_A_DATAN0	IO	1	Negative D-PHY differential data line
MIPI_CSI2X2_A_DATAP1	IO	1	Positive D-PHY differential data line
MIPI_CSI2X2_A_DATAN1	IO	1	Negative D-PHY differential data line
MIPI_CSI2X2_A_DATAP2	IO	1	Positive D-PHY differential data line
MIPI_CSI2X2_A_DATAN2	IO	1	Negative D-PHY differential data line
MIPI_CSI2X2_A_DATAP3	IO	1	Positive D-PHY differential data line
MIPI_CSI2X2_A_DATAN3	IO	1	Negative D-PHY differential data line
MIPI_CSI2X2_B_REXT	IO	1	Reference resistor connection PAD
MIPI_CSI2X2_B_CLKP	IO	1	Positive D-PHY differential clock line
MIPI_CSI2X2_B_CLKN	IO	1	Negative D-PHY differential clock line
MIPI_CSI2X2_B_DATAP0	IO	1	Positive D-PHY differential data line
MIPI_CSI2X2_B_DATAN0	IO	1	Negative D-PHY differential data line
MIPI_CSI2X2_B_DATAP1	IO	1	Positive D-PHY differential data line
MIPI_CSI2X2_B_DATAN1	IO	1	Negative D-PHY differential data line
MIPI_CSI2X2_B_DATAP2	IO	1	Positive D-PHY differential data line
MIPI_CSI2X2_B_DATAN2	IO	1	Negative D-PHY differential data line
MIPI_CSI2X2_B_DATAP3	IO	1	Positive D-PHY differential data line
MIPI_CSI2X2_B_DATAN3	IO	1	Negative D-PHY differential data line

1.4 Function Description

1.4.1 Function Overview

1.4.1.1 CSI2 Function Overview

The overall functional block diagram of CSI2 module is shown in Figure & Table 1-4.

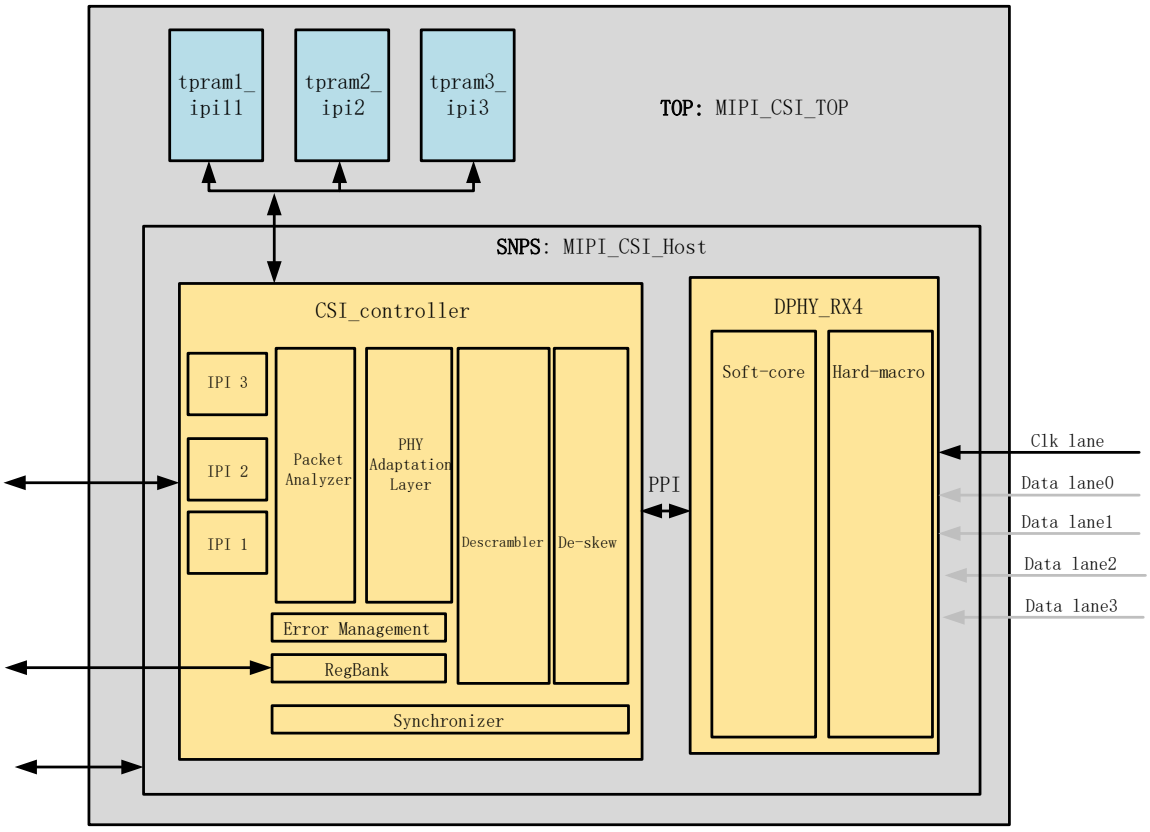


Figure & Table 1-4 CSI2 overall functional block diagram

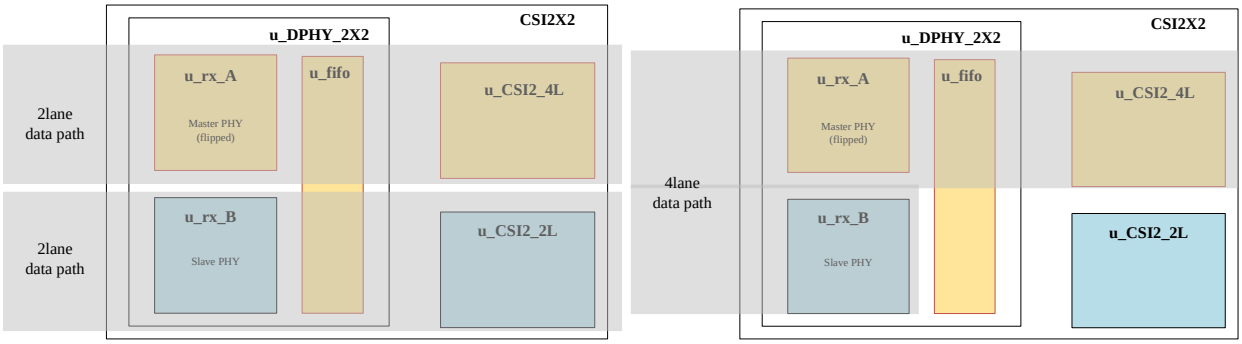
The main blocks of CSI2 are as follows:

- De-skew: Realign them to a common clock (rxbyteclkhs) to compensate for skew between data lanes.
- Descrambler: If enabled, this converts the PPI scrambled data to its original values by using the same LFSR seeds used by the transmitter.
- PHY Adaptation Layer: It is responsible for managing the PHY interface, including PHY error handling.
- Package Analyzer: If required, data lane merging is implemented, together with header decoding, error detection and correction, frame size error detection, and CRC error detection.
- IPI: This block converts the data received through CSI-2 packets from byte to pixel format and outputs a pixel data bus together with Vertical and Horizontal synchronism signal in a parallel format, similar to an RGB interface.
- Error Management: Notifies and monitors the error conditions on the CSI-2 link.

- Register Bank: The register bank is accessible through a standard AMBA-APB slave interface, providing access to the MIPI CSI registers for configuration and control. There is also a fully programmable interrupt generator to inform the system about certain events.
- Synchronizer: This module contains all the synchronizers used to implement CDC functions.

1.4.1.2 CSI2X2 Function Overview

The overall functional block diagram of CSI2X2 module is shown in Figure & Table 1-5.



(1) Non-aggregated mode (2) Aggregated mode

Figure & Table 1-5 CSI2X2 overall functional block diagram

The CSI2X2's default mode is non-aggregated mode. During this mode, CSI2X2's 2lane controller and B PHY work together and CSI2X2's 4lane controller and A PHY work together, the usage of the two groups is the same as CSI2 module.

The CSI2X2 can work in aggregated mode through configuring MIPI_CSI_FIFO_CTRL. MIPI_CSI2X2_FIFO_ENABLE register field. During this mode, A PHY and B PHY are aggregated together, where A is the master PHY, which is used to provide the clock lane. The aggregated 4lane PHY combination and the 4lane controller together form a 4lane data path.

1.4.2 Error Detection and Interrupt

The INI_ST_<group> registers are associated with error condition reporting. These registers trigger the interrupt signal which is synchronous with the AMBA-APB clock.

The Interrupt Force registers (INT_FORCE_<group>) are used for test purposes.

MIPI CSI is possible to monitor the following errors:

- Frame errors such as incorrect frame sequence, reception of a CRC error in the most recent frame, and the mismatch between Frame Start and Frame End.
- Line error such as incorrect line sequence and mismatch between Line Start and Line End.
- Packet errors such as payload CRC and ECC (D-PHY)
- PHY errors such as synchronization pattern mismatch
- IPI-level errors

1.5 Usage

1.5.1 CSI2 Usage

1.5.1.1 Start up MIPI CSI2

The MIPI CSI startup process is as follows:

1. Release MIPI CSI from reset.
2. Configure MIPI CSI.
3. Set or clear PHY reset.
4. Release PHY test codes from reset.

1.5.1.2 Initialize MIPI CSI2

The MIPI CSI initialization process is as follows:

1. Release PHY test codes from reset.
2. Configure the PHY frequency range.
3. Perform additional PHY test code configuration (optional).
4. Set or clear PHY from reset.
5. Configure the number of active lanes.
6. Configure the data ID values (optional).
7. Define errors to be masked.
8. Release MIPI CSI from reset.
9. Check that data lanes are in stop state.

1.5.1.3 Configure IPI

The MIPI CSI configuring IPI process is as follows:

1. Select virtual channel and data type to be processed by IPI.
2. Select the IPI mode.
3. Configure the IPI horizontal frame information.
4. If controller timing mode, configure the IPI vertical frame information.

1.5.1.4 Start and Stop the High Speed Reception Mode

The MIPI CSI starting high speed reception mode process is as follows:

1. Check that clock lane is in HS mode.
2. Start the camera image capture.
3. Monitor the interruption for error reports.

The MIPI CSI stopping high speed reception mode process is as follows:

1. Stop the camera image capture.
2. Set up the camera to stop HS clock transmission.
3. Check that the clock lane is not in HS mode.

4. Request the camera to enter ULPM (optional).

1.5.1.5 Detect Errors

The MIPI CSI detecting errors process is as follows:

1. Read INT_ST_MAIN.
2. Read INT_ST_<group>.

1.5.1.6 Enter and Exit ULPM

The MIPI CSI entering ULPM process is as follows:

1. Request the camera device to enter ULPM (clock and/or data lanes).
2. Check that the controller reports ULPM active (clock and/or data lanes).

The MIPI CSI exiting ULPM process is as follows:

1. Request the camera device to exit ULPM (clock and/or data lanes).
2. Check that the controller reports ULPM is not active (clock and/or data lanes).

1.5.2 CSI2X2 Usage

1.5.2.1 Non-Aggregated Mode

The CSI2X2's default mode is non-aggregated mode. During this mode, CSI2X2's 2lane controller and B PHY work together and CSI2X2's 4lane controller and A PHY work together, the usage of the two groups is the same as CSI2 module.

1.5.2.2 Aggregated Mode

When CSI2X2 module works in aggregated mode，the main differences from CSI2 are as follows:

- Before startup, configure MIPI_CSI_FIFO_CTRL.MIPI_CSI2X2_FIFO_ENABLE register field to enable aggregated mode of CSI2X2.
- The initialization process of A PHY and B PHY are different from the PHY of CSI2.
- In aggregation mode, switch the test port of the 4lane controller through the MIPI_CSI_FIFO_CTRL. MIPI_CSI2X2_FIFO_MODE register field and then choose to configure the register of A PHY or B PHY.

2 VIPRE

2.1 Overview

VIPRE is divided into the following parts: GLUE, MIPI2DMA and MUX logic. The overall structure diagram is shown in Figure & Table 2-1.

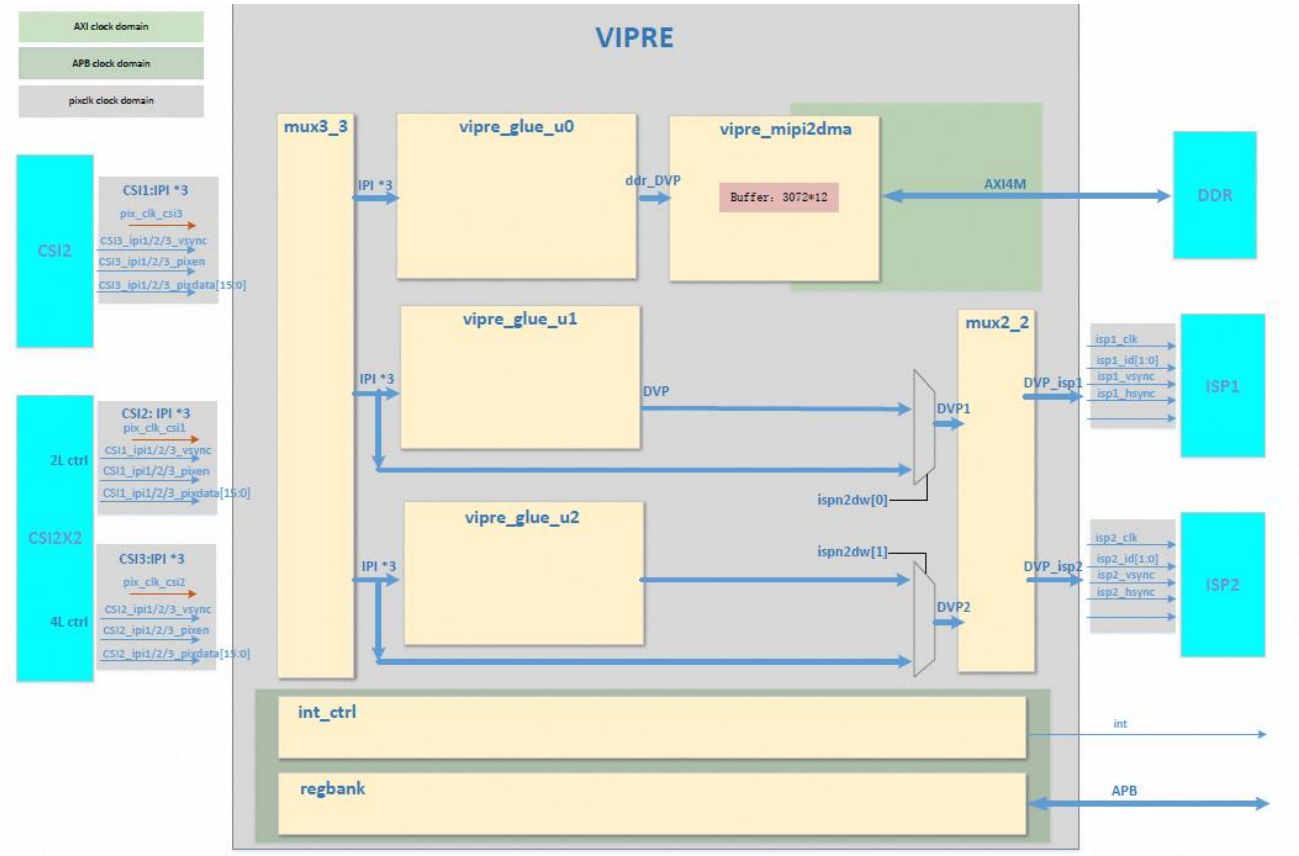


Figure & Table 2-1 VIPRE functional block diagram

The basic functions of each functional module are introduced as follows:

- VIPRE_GLUE part: Corresponds to the functional module "vipre_glue_u0/1/2" in the overall block diagram, the overall realization of the glue logic between the MIPI-IPI interface and the ISP-DVP interface, the completion of the function mainly has the following two types of functions:
  - Supports two types of HDR input of ordinary multi-channel IPI output HDR data and Sony DOL type, and realizes the conversion of two types of HDR input to ISP-DVP interface.
  - Supports cropping resolution function for the original input of MIPI-IPI interface.
- VIPRE_MIPI2DMA part: Corresponds to the functional module "vipre_mipi2dma" in the overall block diagram, realizes the function of writing DDR to the DVP input image, and can support HDR writing of up to three exposures.

- MUX switching part: In addition to the above three types of main functional modules, VIPRE internally has 3 out of 3 and 2 out of 2 mux functions for IPI input and DVP output, as shown in the overall block diagram "mux3_3" and "mux2_2".
  - MUX3_3 has an additional reset recovery function. That is, after the VIPRE is reset as a whole, the input image can be received again from a new complete frame.

2.2 Main Features

The VIPRE has the following features:

- VIPRE_GLUE part features are as follows:
  - Compatible with MIPI CSI output of different HDR sensors with different ID rules.
  - In HDR input mode, the ID number corresponding to Vsync of the output DVP interface and the ID number corresponding to valid are programmable.
  - In HDR mode, whether to generate manually and the generated position of the Vsync signal manually generated by the DVP interface can be configured.
  - The pixels output by the IPI interface of MIPI CSI are finally strobed out of the effective data area and sent to the ISP according to the interval configuration and resolution configuration.
  - Error flag register, error interrupt generation and interrupt mask.
- VIPRE_MIPI2DMA part features are as follows:
  - Supports sensor input of RAW6, RAW7, RAW8, RAW10 and RAW12.
  - Supports the largest sensor input scene to 5M (horizontal up to 2600)@60fps&RAW12.
  - Supports memory access mode of M frame mode and N line mode.
  - Supports 2 exposure or 3 exposure HDR sensor input data access memory.
- Other features:
  - 3 out of 3 mux function, the subsequent three data paths can choose any of the 3 input MIPI CSI controllers as the sensor input source.
  - The mux2_2 module's 2 selection 2 function can realize the rear two ISP channel input sources to arbitrarily select the output of the input two data paths.
  - The two bits of the register field ispndw can respectively realize the bypass function of the two data paths.

2.3 Function Description

2.3.1 VIPRE_GLUE

2.3.1.1 Compatible with Different ID Coding Rules

Compatible with HDR sensors with different ID coding rules, and for HDR sensors with different ID coding rules, such as OV's VC HDR mode or Sony's DOL HDR mode, the VIPRE module can achieve the compatibility of different ID coding rules, the correct ID number is parsed from the IPI output

and sent to the DVP interface of the ISP, and it supports the programmable configuration of the ID number.

2.3.1.2 Programmable Position of the Vsync

In HDR mode, for different sensor types, you can choose whether the Vsync signal of the non-first frame exposure is manually generated by the VIPRE module or is consistent with the IPI input.

2.3.1.3 Compatible with Sony Style DOL Sensor

Compatible support is provided for the special encoding format of Sony DOL sensor. It is possible to determine which of the four ID columns is selected as the ID column to decode ID information by configuring the register, and at the same time, through the programmable matching register and the mask register, the adaptation of flexible ID coding rules can be realized.

2.3.1.4 Strobe Effect Area

The pixels output by the IPI interface of MIPI CSI are finally strobed out of the effective data area and sent to the ISP according to the margin configuration and resolution configuration.

2.3.1.5 Error and Interrupt

Mainly generates two types of errors. After each type of error is generated, it will trigger the generation of interrupt signals that can be masked by the register.

- The first type of error: In HDR mode, multiple IPI data valid signals or frame synchronization signals are used to control the error register. This type of error register is used to indicate that the data bandwidth of the IPI interface is less than that of MIPI D-PHY. Multiple IPI caused by data bandwidth has frame synchronization signal overlap or data valid signal overlap.
- The second type of error: In HDR or DOL mode, the isp_vsync and isp_hsync signals of the final output DVP interface are combined to control the error register. This type of error register is used to indicate the DVP interface frame synchronization signal overlap and the line synchronization signal overlap caused by a setting error.

2.3.2 VIPRE_MIPI2DMA

2.3.2.1 Pixel Storage Format

- The data bit width of AXI bus is fixed at 128bit, and the arrangement of different RAW data for each 32bit is shown in Figure & Table 2-2.

数据格式	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RAW6	3	2	1	0
RAW7	3	2	1	0
RAW8	3	2	1	0
RAW10	1		0	
RAW12	1		0	
RAW10-splicing	2	1	0	

(1) Low-bit mode (default)

数据格式	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RAW6	3	2	1	0
RAW7	3	2	1	0
RAW8	3	2	1	0
RAW10	1		0	
RAW12	1		0	
RAW10-splicing	2	1	0	

(2) High-bit mode

Figure & Table 2-2 Pixel storage format

- Supports different RAW arrangement storage modes with configurable registers, such as low-bit mode and high-bit mode as shown in Figure & Table 2-2, to adapt to different input position requirements of ISP.
- The RAW10-splicing data format is a special data arrangement method for RAW10 data that saves bandwidth. Compared with the normal RAW10 arrangement method, the bus bandwidth utilization rate is increased by 30%, but the data arrangement software is less operability.

2.3.2.2 Image Storage and Trigger Interrupt Mode?

According to the different ways of triggering the completion interrupt after the input RAW image data is stored in the memory, it can be divided into M frame mode and N line mode.

- M frame mode: In this mode, MIPI2DMA writes to DDR in the manner of M frame cyclic writing, M is configurable from 1 to 4, and the M start addresses of M frames can be dynamically configured.
- N-line mode: MIPI2DMA in this mode opens up the address space according to the maximum K lines of pixel storage lines, and writes to the DDR according to the K line cyclic writing method. The K line start address and K value can be dynamically configured, and each time the storage is completed N line triggers the completion interrupt, so the configuration needs to ensure that K>N.

2.3.2.3 M Frame Mode

- Up to M start addresses can be configured, M is configurable from 1 to 4.
- When the M frame start addresses of M frames are 4, 8, 16, and 16, the address alignment requirements are 64byte, 128byte, and 256byte alignment.
- In M frame mode, in addition to the normal resolution information of HORIZON_mipi2dma and VERTICAL_mipi2dma, additional resolution auxiliary information such as STRIDE, HORIZON_CNT128 and READNUM need to be configured. The three register configuration rules are as follows:
  - STRIDE configuration rules: Configure STRIDE to the size of the address space occupied by single-line images (in bytes). Note that the memory space occupied by different RAW formats is different. STRIDE >= HORIZON_mipi2dma is required, and the STRIDE size is 4, 8, 16 when Burstlen. The address alignment requirements are distinguished: 64byte, 128byte and 256byte alignment.

- HORIZON_CNT128 configuration rules: HORIZON_CNT128 = STRIDE_min/16, STRIDE_min is the minimum value of the address space occupied by a single line of image data that meets the 16byte alignment requirements (the address space is in bytes).
- READNUM configuration rules: READNUM = ⌈HORIZON_CNT128/BURSTLEN⌉, that is, READNUM is the value of HORIZON divided by the burst transmission length BURSTLEN and rounded up.
- BURSTREM configuration rules: Configure as the remainder of HORIZON_CNT128 that cannot be divisible by BURSTLEN, and configure the BURSTLEN value when the remainder is 0.
- Example 1: For example, the input RAW image with 1920*1080 - RAW12 - burstlen = 4:
  1920*16/8 = 3840, that is, at least 3840 address space is required to store a row; 3840/64 = 60, that is, 3840 is 64byte aligned; so STRIDE can be configured as 3840 + 64*n (n = 0, 1, 2...)
  STRIDE_min = 3840, STRIDE_min/16 = 240, that is, HORIZON_CNT128 = 240;
  READNUM = ⌈HORIZON_CNT128/BURSTLEN⌉ = ⌈240/4⌉ = 60.
- Example 2: For example, the input RAW image with a resolution of 1080*720 - RAW6 - burstlen = 4:
  1080*8/8 = 1080, that is, at least 1080 address space is required to store a row; 1080/64 = 16.875, that is, 1080 is non-64byte aligned, 17*64 = 1088 is 64byte aligned; so STRIDE can be configured as 1088 + 64*n (N = 0, 1, 2...)
  1080/16 = 67.4, so the minimum value of a row of 16byte alignment is 68*16 = 1088, so STRIDE_min=1088;
  STRIDE_min = 1088, STRIDE_min/16 = 68, that is, HORIZON_CNT128 = 68;
  READNUM = ⌈HORIZON_CNT128/BURSTLEN⌉ = ⌈68/4⌉ = 17.
- Example 3: For example, 1920*1080 - RAW10_splicing - burstlen = 16 input RAW image:
  ⌈1920/3*32⌉/8 = 2560, that is, storing a row requires at least 2560 address space; 2560/256 = 10, that is, 2560 is 256byte aligned; so STRIDE can be configured as 2560 + 256*n (n = 0, 1, 2...)
  STRIDE_min = 2560, STRIDE_min/16 = 160, that is, HORIZON_CNT128 = 160;
  READNUM = ⌈HORIZON_CNT128/BURSTLEN⌉ = ⌈160/4⌉ = 40.
  Note: Only BURSTREM is configured so that when READNUM != HORIZON_CNT128/BURSTLEN, that is, when HORIZON_CNT128 is not divisible by BURSTLEN, the data at the end of the last line of each frame will be written to DDR in time, instead of waiting for the next line to come and push it out.

- There is an end interrupt at the end of each frame. You can check which frame of the M frame is interrupted through the status register.
- With M frame overflow interrupt: The main control CPU needs to update the current read frame and read row in real time through the configuration status register, and trigger the M frame overflow interrupt when the data row is written to cover the data row that has not been read.

2.3.2.4 N Line Mode

- You can configure the starting address of the K-row pixel storage row. When the starting address of the K-row storage space is 4, 8, or 16, the address alignment requirements are 64byte, 128byte, and 256byte alignment.
- The configurable range of row K and row N are both 1~8191, and requires K > N, N > 8.
- In addition to the resolution information, additional stride information needs to be configured.
- In N-line mode, the configuration rules of M_STRIDE, HORIZON_CNT128, READNUM and BURSTREM are the same as those of M-frame mode.
- An interrupt is triggered when every N rows are written. The main control CPU needs to update which row of the K row is currently read through the configuration status register, and trigger the N row overflow interrupt when the data row is written to cover the data row that has not been read.
- How many N rows of data have been written in the current frame can be queried through the register.

2.3.2.5 Start-Stop Mechanism

MIPI2MDA has a start-stop function, the start-stop operation processing flow is explained as follows (Figure & Table 2-6 flow chart is consistent with the operation described below):

- Start function
  The register can be configured to set the MIPI2DMA start register to 1 to start the effective pixel input of the ddr_DVP interface and allow the AXI bus request to be initiated. The MIPI2DMA module captures a new complete frame and starts the DDR write operation.
- Stop mechanism
  In the normal startup state of the MIPI2DMA module, you can first configure the startup register to be set to 0 (stop MIPI input and stop bus request), then wait for the completion of the bus IDLE and issue a successful stop interrupt, and finally configure the MIPI2DMA local reset to complete a complete MIPI2DMA module stop operation.
- The time interval between receiving the stop completion interrupt and resetting
  There must be at least an interval between receiving the stop completion interrupt and reset (3 APB cycles + 3 pixclk cycles + 2 AXI cycles). The absolute software time requirement is that the interval between interrupt and reset is at least 100ns.

2.3.3 VIPRE Resolution Settings

- Inside VIPRE, there are two types of resolutions: GLUE and MIPI2DMA, which need to be configured correctly.
- The GLUE part needs to configure the input image resolution of three groups of IPI interfaces according to the actual MIPI IPI output image resolution.
  Note: In DOL-HDR mode, you still need to set the GLUE resolution register according to the actual IPI input image resolution, that is, the resolution row information needs to include the

ID column. At the same time, the GLUE clipping part needs to be configured correctly in the VIPRE non-bypass mode in order to ensure the normal operation of GLUE.

- The resolution information of MIPI2DMA should also be correctly configured according to the actual input resolution information of MIPI2DMA after trimming by GLUE.

2.3.4 VIPRE Reset Settings

There are soft reset control of three data channels inside VIPRE:

- VIPRE internal register MIPI2DMA_RSTN_PULSE controls the reset of vipre_glue_u0+VIPRE_MIPI2DMA independently. The operation attribute of the register is W1AC, which does not affect the APB clock domain of MIPI2DMA, nor does it affect the working status of VIPRE's other functional modules other than vipre_glue_u0 and VIPRE_MIPI2DMA.
- VIPRE internal register GLUE1_RSTN_P independently controls the reset of vipre_glue_u1, and the register operation attribute is W1AC.
- VIPRE internal register GLUE2_RSTN_PULSE independently controls the reset of vipre_glue_u2, and the register operation attribute is W1AC.

2.4 Usage

2.4.1 VIPRE_GLUE

2.4.1.1 Mux Function

Configure the register field MUX3_2/csin2isp1 to set which of the three MIPI CSI controller outputs corresponds to vipre_glue_u1.
Configure the register field MUX3_2/csin2isp2 to set which of the three MIPI CSI controller outputs corresponds to vipre_glue_u2.
Configure the register field MUX3_2/csin2ddr to set which of the three MIPI CSI controller outputs corresponds to vipre_glue_u0.
Configure the register field MUX3_2/dvpn2isp1 to set which DVP outputs to ISP1.
Configure the register field MUX3_2/dvpn2isp2 to set which DVP outputs to ISP2.
Configure the register field ISPSEL/ispn2dw to set whether mux3_3 outputs bypass to DVP1|2 or not.

2.4.1.2 Compatible with Sony Style DOL Sensor

Configure the register field MODSEL/modsel to set the mode of the input sensor.
Configure the register field HDRCTRL0/strobe4_1 to select which of the 4 ID columns is used to decode the ID value.
Configure the register field HDRCTRL2/idcode_dol1 to set the ID code setting of the first exposure image that needs to be matched.
Configure the register field HDRCTRL2/idmask_dol1 to set the ID code setting of the first exposure image that needs to be masked.

Configure the register field HDRCTRL3/idcode_dol2 to set the ID code setting of the first exposure image that needs to be matched.
Configure the register field HDRCTRL3/idmask_dol2 to set the ID code setting of the first exposure image that needs to be masked.
Configure the register field HDRCTRL4/idcode_dol3 to set the ID code setting of the first exposure image that needs to be matched.
Configure the register field HDRCTRL4/idmask_dol3 to set the ID code setting of the first exposure image that needs to be masked.

2.4.1.3 Programmable Position of the Vsync

Configure the register field HDRCTRL0/vsyncen to decide whether to artificially generate a Vsync signal other than the first exposure frame.
Configure this register field HDRCTRL0/vsync_posedgenum_2 to determine the number of rising edges of Hsync before the artificially generated second Vsync.
Configure this register field HDRCTRL1/vsync_posedgenum_3 to determine the number of rising edges of Hsync before the artificially generated third Vsync.
As this register field HDRCTRL0/vsync_delay_2: existing when vsyncen = 1 and ranging from 1 to 8191. This (vsync_delay_2 + 3) is used to set the number of cycles delay between the last count rising edge of IPI pixen and the generating of second hand generated Vsync pulse.
As this register field HDRCTRL1/vsync_delay_3: existing when vsyncen = 1 and ranging from 1 to 8191. This (vsync_delay_3 + 3) is used to set the number of cycles delay between the last count rising edge of IPI pixen and the generating of second hand generated Vsync pulse.
The timing diagrams of the two different configuration situations are shown in Figure & Table 2-3 and Figure & Table 2-4.

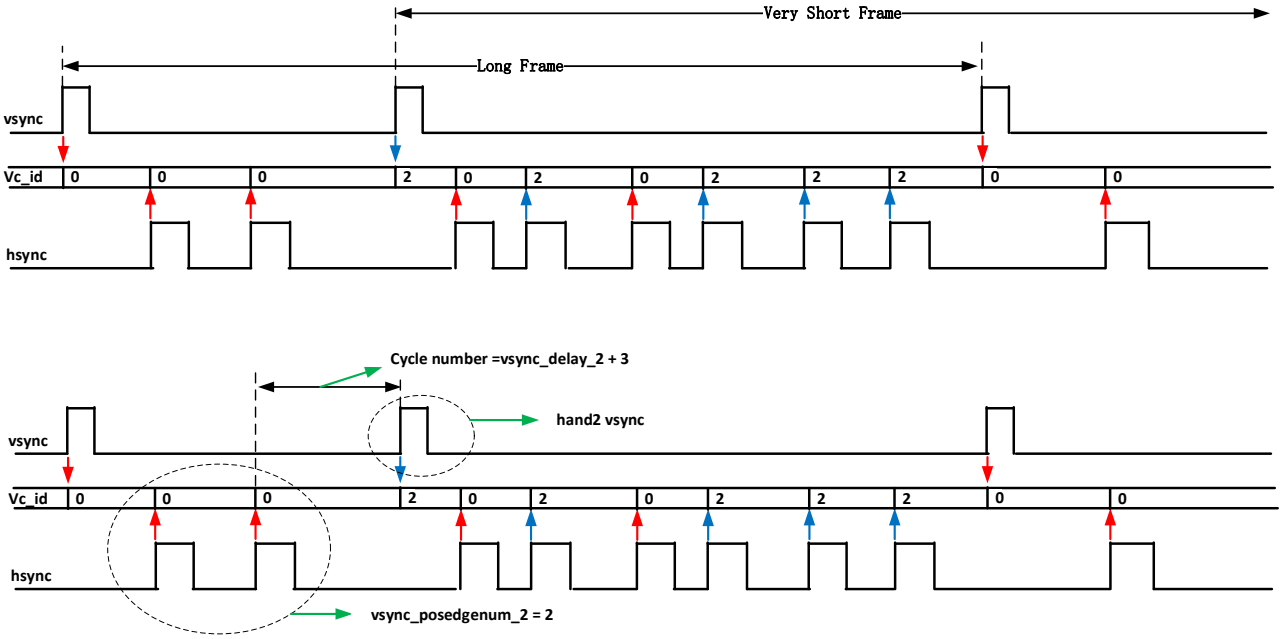


Figure & Table 2-3 vsync_posedgenum_2 != 0 situation

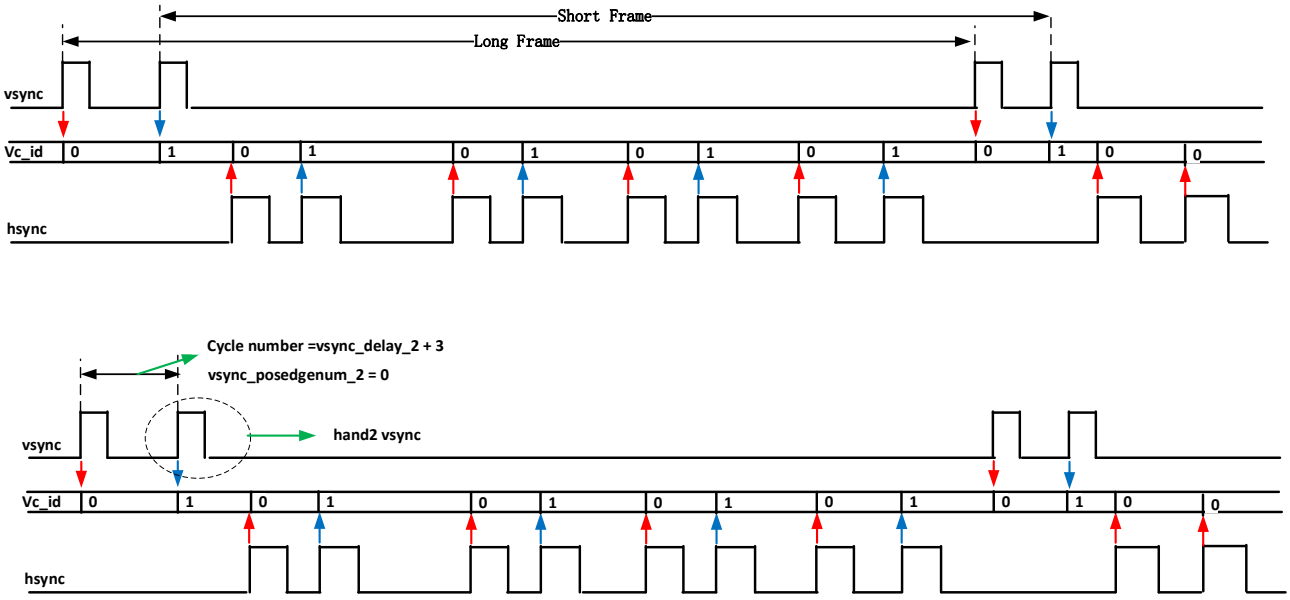


Figure & Table 2-4 vsync_posedgenum_2 = 0 situation

2.4.1.4 Programmable ID Number

Configure the register field IDNUM/id_hand1 to set the ID number corresponding to the Vsync signal of the first frame of exposure image.
Configure the register field IDNUM/id_hand2 to set the ID number corresponding to the Vsync signal of the second frame of exposure image.
Configure the register field IDNUM/id_hand3 to set the ID number corresponding to the Vsync signal of the third frame of exposure image.
Configure the register field IDNUM/id1 to set the ID number corresponding to the pixen signal of the first frame of exposure image.
Configure the register field IDNUM/id2 to set the ID number corresponding to the pixen signal of the second frame of exposure image.
Configure the register field IDNUM/id3 to set the ID number corresponding to the pixen signal of the third frame of exposure image.

2.4.1.5 Strobe Effect Area

Configure the register field IDNUM/id1 to set the ID number corresponding to the pixen signal of the first frame of exposure image.
Configure the register fields VMARGINCFG_IPIx/ipix_vbp, VMARGINCFG_IPIx/ipix_vfp, HMARGINCFG_IPIx/ipix_hbp, HMARGINCFG_IPIx/ipix_hbp, RESCFG/horizon and RESCFG/vertical to select effective area，the margin parameter meaning map is shown in Figure & Table 2-5.

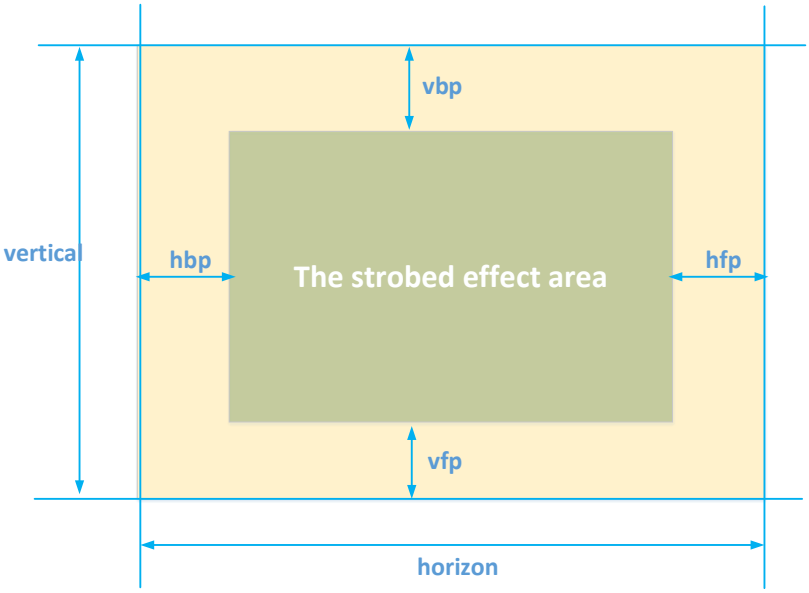


Figure & Table 2-5 Margin parameter meaning map

2.4.1.6 Error and Interrupt

Configure the register field ERR_MASK/int_mask to set the ID number corresponding to the pixen signal of the first frame of exposure image.

By reading the ERR_MASK/hdroverlap_err register, judge whether the output Vsync and hsync overlap in HDR mode.

By reading the ERR_MASK/doloverlap_err register, judge whether the output Vsync and hsync overlap in DOL mode.

By reading the ERR_MASK/vsyncoverlap_err register, judge whether the output of multiple IPI Vsync overlap in HDR mode.

By reading the ERR_MASK/pixenoverlap_err register, judge whether the output of multiple IPI pixen overlap in HDR mode.

2.4.2 VIPRE_MIPI2DMA

The working process of VIPRE_MIPI2DMA is shown in Figure & Table 2-6.

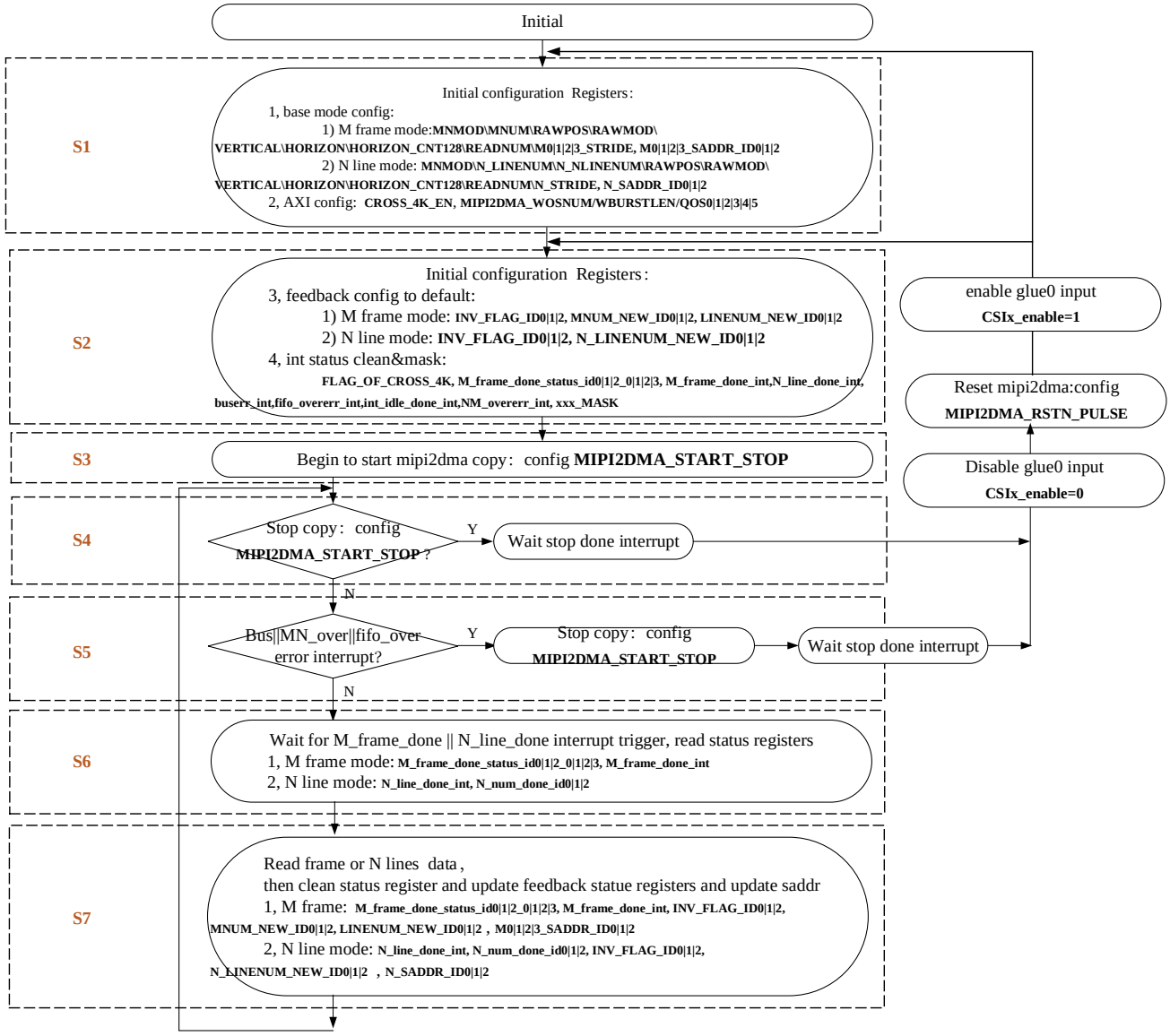


Figure & Table 2-6 VIPRE_MIPI2DMA work flow

1. Basic mode configuration, after this step is configured, if it is not necessary in the normal working process, there is no need to dynamically update.
   - M frame mode: Configuration switch to M frame mode (MNMOD), M frame loop upper limit (MNUM), RAW data storage location (RAWPOS), RAW image format (RAWMOD), horizontal and vertical resolution (VERTICAL_mipi2dma&HORIZON_mipi2dma), resolution auxiliary information (HORIZON_CNT128&READNUM&M0|1|2|3_STRIDE), frame start address (M0|1|2|3_SADDR_ID0|1|2), etc.

     Note: M0|1|2|3_SADDR_ID0|1|2 distinguishes the start addresses of different ID channels corresponding to different M frames.
   - N-line mode: Configuration switch to N-frame mode (MNMOD), K-line loop upper limit (N_LINENUM), N-line count value (N_NLINENUM), RAW data storage location (RAWPOS), RAW image format (RAWMOD), horizontal and vertical resolution

(VERTICAL_mipi2dma&HORIZON_mipi2dma), resolution auxiliary information (HORIZON_CNT128&READNUM& N_STRIDE), frame start address (N_SADDR_ID0|1|2), etc.
Note: N_SADDR_ID0|1|2 distinguishes the start address of the different ID channels corresponding to the K row.

2. Basic register initialization operation, this step is executed after MIPI2DMA is executed for the first time or MIPI2DMA is reset.
   - M frame mode: Set the feedback status register (INV_FLAG_ID0|1|2, MNUM_NEW_ID0|1|2, LINENUM_NEW_ID0|1|2) to the initial value, and initialize the interrupt status register: FLAG_OF_CROSS_4K, M_frame_done_status_id0|1|2_0|1|2|3, M_frame_done_int, N_line_done_int, buserr_int, fifo_overerr_int, int_idle_done_int, NM_overerr_int, xxx_MASK.
   - N-line mode: Set the feedback status register (INV_FLAG_ID0|1|2, N_LINENUM_NEW_ID0|1|2) to the initial value, and initialize the interrupt status register: FLAG_OF_CROSS_4K, M_frame_done_status_id0|1|2_0|1|2|3, M_frame_done_int, N_line_done_int, buserr_int, fifo_overerr_int, int_idle_done_int, NM_overerr_int, xxx_MASK.
3. Configure to start MIPI2DMA data transfer (MIPI2DMA_START_STOP).
4. Configure whether to stop MIPI2DMA data transfer (MIPI2DMA_START_STOP):
   - Stop: After waiting for the stop completion interrupt, first configure csix_enable = 0 to stop the input of vipre_glue_u0, configure the register to reset the MIPI2DMA module (MIPI2DMA_RSTN_PULSE), and then configure csix_enable = 1 to enable the input of vipre_glue_u0 and then jump to step 2 to start a new transfer.
   - Do not stop: jump to step 5.
5. Whether to trigger the bus error interrupt (bus error) or data overwrite error interrupt (MN_over error) or FIFO overflow error interrupt (fifo_over error) during the execution of data transfer:
   - Trigger: Configure to stop MIPI2DMA data transfer (MIPI2DMA_START_STOP), and then wait for the stop to complete the interrupt, configure the register to reset the MIPI2DMA module (MIPI2DMA_RSTN_PULSE), and then jump to step 2 to start a new transfer.
   - No trigger: jump to step 6.
6. Wait for the frame transfer completion interrupt or N line transfer completion interrupt, and read the status register to obtain the current transfer information:
   - M frame mode: Wait for the frame transfer completion interrupt (M_frame_done) to be triggered, and the transfer completion interrupt status information can be obtained by reading the register M_frame_done_int, and reading the register M_frame_done_status_id0|1|2_0|1|2|3 to obtain the current frame completion interrupt corresponding to which ID channel in which frame in the M frame.
   - N-line mode: Wait for the triggering of the N-line transfer completion interrupt (N_line_done), and read the register N_line_done_int to obtain the transfer completion interrupt status information, and read the register N_num_done_id0|1|2 to get how many N lines have been completed in the current transfer frame's handling.
7. Read frame data or N rows of data, and configure the feedback register to feedback the processing progress of the current main control CPU on the transported image data:

- M frame mode: The main control CPU processes the frame data that has been transported by MIPI2DMA, and after the processing is completed, first clear the corresponding interrupt status register (M_frame_done_status_id0|1|2_0|1|2|3, M_frame_done_in); then configure the feedback status register to update MIPI2DMA the main control CPU's processing progress of the transferred image data (INV_FLAG_ID0|1|2, MNUM_NEW_ID0|1|2, LINENUM_NEW_ID0|1|2), where INV_FLAG_ID0|1|2 corresponds to the frame completion flags of different ID channels register, the main control CPU is required to invert this flag register after each M frame is processed. MNUM_NEW_ID0|1|2 identifies which frame of the M frame is currently or will be processed by the main control CPU, LINENUM_NEW_ID0|1| 2 identifies which line in the current frame is currently or will be processed by the main control CPU. These three types of feedback information are used to detect data coverage errors and must be updated in time. Finally, if necessary, the register M0|1|2|3_SADDR_ID0|1 can be configured |2 to update the frame start address. This update operation will take effect in the next transport for the current MIPI2DMA transport frame, and will take effect immediately for the remaining transport frames.
- N line mode: The control CPU processes the N-line data that has been transported by MIPI2DMA. After the processing is completed, the corresponding interrupt status register (N_line_done_status_id0|1|2, N_line_done_in) is first cleared; then the feedback status register is configured to update the master to MIPI2DMA. Control the CPU processing progress of the transferred image data (INV_FLAG_ID0|1|2, N_LINENUM_NEW_ID0|1|2), where INV_FLAG_ID0|1|2 corresponds to the K line completion flag register of different ID channels, and requires the main control CPU to read K after each K N_LINENUM_NEW_ID0|1|2 identifies which line of the current K line is currently or will be processed by the main control CPU. These two types of feedback information are used to detect data overwriting errors and must be updated in time. Finally, if necessary, the register N_SADDR_ID0|1|2 can be configured to update the start address of row K. This update operation will take effect in the next movement for the current MIPI2DMA moving K rows. For the K rows moved by the remaining ID channels, effective immediately.

NOTE

- Each step in the flowchart is marked with configuration registers that need to be paid attention to. For a more detailed explanation of the functions of these registers, see Chapter 5.
- The ID information of the ID channel corresponds to the long, medium and short exposures from the vipre_glue_u0 module of the MIPI2DMA front end. The suffix id0 in the MIPI2DMA register corresponds to ID = 0, the suffix id1 corresponds to ID = 1, and the suffix id2 corresponds to ID = 2.

2.5 Register Description

2.5.1 Register Memory Map

Register	Offset	Description	Section/Page
G1_MUX3_2	0x0	MUX3_2 configuration register	2.5.2.1/25

Register	Offset	Description	Section/Page
G1_MODSEL	0x4	Mode select configuration register	2.5.2.2/26
G1_IDNUM	0x8	ISP ID number configuration register	2.5.2.3/27
G1_RESCFG	0xc	Resolution parameter configuration register	2.5.2.4/27
G1_HDRCTRL0	0x10	HDR control register 0	2.5.2.5/28
G1_HDRCTRL1	0x14	HDR control register 1	2.5.2.6/29
G1_HDRCTRL2	0x18	HDR control register 2: Sony DOL long exposure ID rule and mask	2.5.2.7/29
G1_HDRCTRL3	0x1c	HDR control register 2: Sony DOL short exposure ID rule and mask	2.5.2.8/30
G1_HDRCTRL4	0x20	HDR control register 2: Sony DOL very short exposure ID rule and mask	2.5.2.9/30
G1_ERR_MASK	0x24	Error and interrupt mask control register	2.5.2.10/30
G1_VMARGINCFG_IPI1	0x28	Vertical margin parameter configuration register	2.5.2.11/31
G1_HMARGINCFG_IPI1	0x2c	Horizontal margin parameter configuration register	2.5.2.12/32
G1_VMARGINCFG_IPI2	0x30	Vertical margin parameter configuration register	2.5.2.13/32
G1_HMARGINCFG_IPI2	0x34	Horizontal margin parameter configuration register	2.5.2.14/32
G1_VMARGINCFG_IPI3	0x38	Vertical margin parameter configuration register	2.5.2.15/33
G1_HMARGINCFG_IPI3	0x3c	Horizontal margin parameter configuration register	2.5.2.16/33
G1_RESCFG2	0x40	Resolution parameter configuration register	2.5.2.17/34
G1_RESCFG3	0x44	Resolution parameter configuration register	2.5.2.18/34
G2_RESEV	0x48	MUX3_2 configuration register	2.5.2.19/35
G2_MODSEL	0x4c	Mode select configuration register	2.5.2.20/35
G2_IDNUM	0x50	ISP ID number configuration register	2.5.2.21/35
G2_RESCFG	0x54	Resolution parameter configuration	2.5.2.22/36

Register	Offset	Description	Section/Page
		register	
G2_HDRCTRL0	0x58	HDR control register 0	2.5.2.23/37
G2_HDRCTRL1	0x5c	HDR control register 1	2.5.2.24/37
G2_HDRCTRL2	0x60	HDR control register 2: Sony DOL long exposure ID rule and mask	2.5.2.25/38
G2_HDRCTRL3	0x64	HDR control register 2: Sony DOL short exposure ID rule and mask	2.5.2.26/38
G2_HDRCTRL4	0x68	HDR control register 2: Sony DOL very short exposure ID rule and mask	2.5.2.27/39
G2_ERR_MASK	0x6c	Error and interrupt mask control register	2.5.2.28/39
G2_VMARGINCFG_IPI1	0x70	Vertical margin parameter configuration register	2.5.2.29/40
G2_HMARGINCFG_IPI1	0x74	Horizontal margin parameter configuration register	2.5.2.30/40
G2_VMARGINCFG_IPI2	0x78	Vertical margin parameter configuration register	5.2.31/41
G2_HMARGINCFG_IPI2	0x7c	Horizontal margin parameter configuration register	2.5.2.32/41
G2_VMARGINCFG_IPI3	0x80	Vertical margin parameter configuration register	2.5.2.33/42
G2_HMARGINCFG_IPI3	0x84	Horizontal margin parameter configuration register	2.5.2.34/42
G2_RESCFG2	0x88	Resolution parameter configuration register	2.5.2.35/43
G2_RESCFG3	0x8c	Resolution parameter configuration register	2.5.2.36/43
ISPSEL	0x90	Select GLUE of ISP to bypass or not	2.5.2.37/44
G0_RESEV	0x150	MUX3_2 configuration register	2.5.2.38/44
G0_MODSEL	0x154	Mode select configuration register	2.5.2.39/44
G0_IDNUM	0x158	ISP ID number configuration register	2.5.2.40/45
G0_RESCFG	0x15c	Resolution parameter configuration register	2.5.2.41/46
G0_HDRCTRL0	0x160	HDR control register 0	2.5.2.42/46

Register	Offset	Description	Section/Page
G0_HDRCTRL1	0x164	HDR control register 1	2.5.2.43/47
G0_HDRCTRL2	0x168	HDR control register 2: Sony DOL long exposure ID rule and mask	2.5.2.44/47
G0_HDRCTRL3	0x16c	HDR control register 2: Sony DOL short exposure ID rule and mask	2.5.2.45/48
G0_HDRCTRL4	0x170	HDR control register 2: Sony DOL very short exposure ID rule and mask	2.5.2.46/48
G0_ERR_MASK	0x174	Error and interrupt mask control register	2.5.2.47/49
G0_VMARGINCFG_IPI1	0x178	Vertical margin parameter configuration register	2.5.2.48/49
G0_HMARGINCFG_IPI1	0x17c	Horizontal margin parameter configuration register	2.5.2.49/50
G0_VMARGINCFG_IPI2	0x180	Vertical margin parameter configuration register	2.5.2.50/50
G0_HMARGINCFG_IPI2	0x184	Horizontal margin parameter configuration register	2.5.2.51/51
G0_VMARGINCFG_IPI3	0x188	Vertical margin parameter configuration register	2.5.2.52/51
G0_HMARGINCFG_IPI3	0x18c	Horizontal margin parameter configuration register	2.5.2.53/52
G0_RESCFG2	0x190	Resolution parameter configuration register	2.5.2.54/52
G0_RESCFG3	0x194	Resolution parameter configuration register	2.5.2.55/52
MIPI2DMA_CTRL0	0x198	mipi2dma ctrl0	2.5.2.56/53
MIPI2DMA_CTRL1	0x19c	mipi2dma ctrl1	2.5.2.57/54
MIPI2DMA_CTRL2	0x1a0	mipi2dma ctrl2	2.5.2.58/54
MIPI2DMA_CTRL3	0x1a4	mipi2dma ctrl3	2.5.2.59/55
MIPI2DMA_CTRL4	0x1a8	mipi2dma ctrl4	2.5.2.60/55
MIPI2DMA_CTRL5	0x1ac	mipi2dma ctrl5	2.5.2.61/56
MIPI2DMA_CTRL6	0x1b0	mipi2dma ctrl6	2.5.2.62/56
MIPI2DMA_CTRL7	0x1b4	mipi2dma ctrl7	2.5.2.63/57
MIPI2DMA_CTRL8	0x1b8	mipi2dma ctrl8	2.5.2.64/57

Register	Offset	Description	Section/Page
MIPI2DMA_CTRL9	0x1bc	mipi2dma ctrl9	2.5.2.65/58
MIPI2DMA_CTRL10	0x1c0	mipi2dma ctrl10	2.5.2.66/58
MIPI2DMA_CTRL11	0x1c4	mipi2dma ctrl11	2.5.2.67/58
MIPI2DMA_CTRL12	0x1c8	mipi2dma ctrl12	2.5.2.68/59
MIPI2DMA_CTRL13	0x1cc	mipi2dma ctrl13	2.5.2.69/59
MIPI2DMA_CTRL14	0x1d0	mipi2dma ctrl14	2.5.2.70/59
MIPI2DMA_CTRL15	0x1d4	mipi2dma ctrl15	2.5.2.71/60
MIPI2DMA_CTRL16	0x1d8	mipi2dma ctrl16	2.5.2.72/60
MIPI2DMA_CTRL17	0x1dc	mipi2dma ctrl17	2.5.2.73/60
MIPI2DMA_CTRL18	0x1e0	mipi2dma ctrl18	2.5.2.74/61
MIPI2DMA_CTRL19	0x1e4	mipi2dma ctrl19	2.5.2.75/61
MIPI2DMA_CTRL20	0x1e8	mipi2dma ctrl20	2.5.2.76/61
MIPI2DMA_CTRL21	0x1ec	mipi2dma ctrl21	2.5.2.77/62
MIPI2DMA_CTRL22	0x1f0	mipi2dma ctrl22	2.5.2.78/62
MIPI2DMA_CTRL23	0x1f4	mipi2dma ctrl23	2.5.2.79/62
MIPI2DMA_CTRL24	0x1f8	mipi2dma ctrl24	2.5.2.80/63
MIPI2DMA_CTRL25	0x1fc	mipi2dma ctrl25	2.5.2.81/64
MIPI2DMA_CTRL26	0x200	mipi2dma ctrl26	2.5.2.82/64
MIPI2DMA_CTRL27	0x204	mipi2dma ctrl27	2.5.2.83/64
MIPI2DMA_CTRL28	0x208	mipi2dma ctrl28	2.5.2.84/64
MIPI2DMA_CTRL29	0x20c	mipi2dma ctrl29	2.5.2.85/65
MIPI2DMA_CTRL30	0x210	mipi2dma ctrl30	2.5.2.86/65
MIPI2DMA_CTRL31	0x214	mipi2dma ctrl31	2.5.2.87/65
MIPI2DMA_CTRL32	0x218	mipi2dma ctrl32	2.5.2.88/66
MIPI2DMA_CTRL33	0x21c	mipi2dma ctrl33	2.5.2.89/66
MIPI2DMA_CTRL34	0x220	mipi2dma ctrl34	2.5.2.90/66
MIPI2DMA_CTRL35	0x224	mipi2dma ctrl35	2.5.2.91/67
MIPI2DMA_CTRL36	0x228	mipi2dma ctrl36	2.5.2.92/67
MIPI2DMA_CTRL37	0x22c	mipi2dma ctrl37	2.5.2.93/67

Register	Offset	Description	Section/Page
MIPI2DMA_CTRL38	0x230	mipi2dma ctrl38	2.5.2.94/67
MIPI2DMA_CTRL39	0x234	mipi2dma ctrl39	2.5.2.95/68
MIPI2DMA_CTRL40	0x238	mipi2dma ctrl40	2.5.2.96/68
MIPI2DMA_CTRL41	0x23c	mipi2dma ctrl41	2.5.2.97/68
MIPI2DMA_CTRL42	0x240	mipi2dma ctrl42	2.5.2.98/69
MIPI2DMA_CTRL43	0x244	mipi2dma ctrl43	2.5.2.99/69
MIPI2DMA_CTRL44	0x248	mipi2dma ctrl44	2.5.2.100/70
MIPI2DMA_CTRL45	0x24c	mipi2dma ctrl45	2.5.2.101/71
MIPI2DMA_CTRL46	0x250	mipi2dma ctrl46	2.5.2.102/72
MIPI2DMA_CTRL47	0x254	mipi2dma ctrl47	2.5.2.103/72
MIPI2DMA_CTRL48	0x258	mipi2dma ctrl48	2.5.2.104/72
MIPI2DMA_CTRL49	0x25c	mipi2dma ctrl49	2.5.2.105/72
MIPI2DMA_CTRL50	0x260	mipi2dma ctrl50	2.5.2.106/73
MIPI2DMA_CTRL51	0x264	mipi2dma ctrl51	2.5.2.107/73

2.5.2 Register and Field Description

2.5.2.1 G1_MUX3_2

- Description: MUX3_2 configuration register
- Offset: 0x0; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x0

Bits	Name	Access	Description
[31:11]	RESV1	RW	Reserved field Value After Reset: 0x0
[10]	CSI1_ENABLE	RW	CSI1 input enable, default 0, not inout Value After Reset: 0x0
[9]	CSI2_ENABLE	RW	CSI2 input enable, default 0, not inout Value After Reset: 0x0
[8]	CSI3_ENABLE	RW	CSI3 input enable, default 0, not inout Value After Reset: 0x0
[7]	DVPN2ISP2	RW	Select which DVP to ISP2, default DVP2.

Bits	Name	Access	Description
			0: DVP2-ISP2 1: DVP1-ISP2 Value After Reset: 0x0
[6]	DVPN2ISP1	RW	Select which DVP to ISP1, default DVP1. 0: DVP1-ISP1 1: DVP2-ISP1 Value After Reset: 0x0
[5:4]	CSIN2DDR	RW	Select which CSI to GlUE0, default CSI1. 00: CSI1-GLUE0 01: CSI2-GLUE0 10|11: CSI3-Glue0 Value After Reset: 0x0
[3:2]	CSIN2ISP1	RW	Select which CSI to GLUE1, default CSI1. 00: CSI1-GLUE1 01: CSI2-GlUE1 10|11: CSI3-Glue1 Value After Reset: 0x0
[1:0]	CSIN2ISP2	RW	Select which CSI to GlUE2, default CSI1. 00: CSI1-GLUE2 01: CSI2-GLUE2 10|11: CSI3-GLUE2 Value After Reset: 0x0

2.5.2.2 G1_MODSEL

- Description: Mode select configuration register
- Offset: 0x4; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x0

Bits	Name	Access	Description
[31:3]	RESV2	RW	Reserved field Value After Reset: 0x0
[2:0]	MODSEL	RW	Select which mode of sensor. 000|101|111: Normal signal exposure mode 001: Normal HDR 2-frame mode 010: Normal HDR 3-frame mode

Bits	Name	Access	Description
			011: Sony DOL HDR 2-frame mode 100: Sony DOL HDR 3-frame mode Value After Reset: 0x0

2.5.2.3 G1_IDNUM

- Description: ISP ID number configuration register. Configures the ID numbers of the IPI interface for long, short and very short explosure to 0\1\2 respectively.
- Offset: 0x8; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x924

Bits	Name	Access	Description
[31:12]	RESV3	RW	Reserved field Value After Reset: 0x0
[11:10]	ID_THIRD_VSYNC	RW	Reserved field Value After Reset: 0x2
[9:8]	ID_SECOND_VSYNC	RW	Reserved field Value After Reset: 0x1
[7:6]	ID_FIRST_VSYNC	RW	Reserved field Value After Reset: 0x0
[5:4]	ID3	RW	Reserved field Value After Reset: 0x2
[3:2]	ID2	RW	Reserved field Value After Reset: 0x1
[1:0]	ID1	RW	Reserved field Value After Reset: 0x0

2.5.2.4 G1_RESCFG

- Description: Resolution parameter configuration register. Note that the resolution parameter here is the actual resolution passed by the IPI1 interface including margin information.
- Offset: 0xc; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x7800438

Bits	Name	Access	Description
[31:29]	RESV4	RW	Reserved field Value After Reset: 0x0

Bits	Name	Access	Description
[28:16]	IPI1_HORIZON	RW	Horizontal resolution with margin, default 1920 Value After Reset: 0x780
[15:13]	RESV4_5	RW	Reserved field Value After Reset: 0x0
[12:0]	IPI1_VERTICAL	RW	Vertical resolution with margin, default 1080 Value After Reset: 0x438

2.5.2.5 G1_HDRCTRL0

- Description: HDR control register 0
- Offset: 0x10; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2

Bits	Name	Access	Description
[31:29]	RESV5	RW	Reserved field Value After Reset: 0x0
[28:27]	STROBE4_1	RW	Strobe 4 of 1 in Sony ID column 00: Column 1 as ID data 01: Column 2 as ID data 10: Column 3 as ID data 11: Column 4 as ID data Value After Reset: 0x0
[26:14]	VSYNC_POSEDGENUM_SECOND	RW	Exists: vsyncen==1; range from 0 to 8191 This value is used to set the second hand generated Vsync pulse to be generated after which several IPI pixen rising edges. Value After Reset: 0x0
[13:1]	VSYNC_DELAY_SECOND	RW	Exists: vsyncen==1; range from 3 to 8191 This (value+3) is used to set the number of cycles delay between the last count rising edge of IPI pixen and the generating of third hand generated Vsync pulse. Value After Reset: 0x1
[0]	VSYNCEN	RW	Select whether the other exposure frames under multi-exposure need to be generated by hardware. 1: Enable hardware generation 0: Disable

Bits	Name	Access	Description
			Value After Reset: 0x0

2.5.2.6 G1_HDRCTRL1

- Description: HDR control register 1
- Offset: 0x14; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x8

Bits	Name	Access	Description
[31:27]	RESV6	RW	Reserved field Value After Reset: 0x0
[26:14]	VSYNC_POSEDGENUM_THIRD	RW	Exists: vsyncen==1; range from 0 to 8191 This value is used to set the third hand generated Vsync pulse to be generated after which several IPI pixen rising edges. Value After Reset: 0x0
[13:1]	VSYNC_DELAY_THIRD	RW	Exists: vsyncen==1; range from 1 to 8191 This (value+3) is used to set the number of cycles delay between the last count rising edge of IPI pixen and the generating of third hand generated Vsync pulse. Value After Reset: 0x4
[0]	RESV6_5	RW	Value After Reset: 0x0

2.5.2.7 G1_HDRCTRL2

- Description: HDR control register 2: Sony DOL long exposure ID rule and mask
- Offset: 0x18; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0xfd80fd9

Bits	Name	Access	Description
[31:28]	RESV7	RW	Reserved field Value After Reset: 0x0
[27:16]	IDMASK_DOL1	RW	Active high, DOL long exposure mask bit Value After Reset: 0xFD8
[15:12]	RESV7_5	RW	Reserved field Value After Reset: 0x0
[11:0]	IDCODE_DOL1	RW	DOL long exposure ID code bit

Bits	Name	Access	Description
			Value After Reset: 0xFD9

2.5.2.8 G1_HDRCTRL3

- Description: HDR control register 2: Sony DOL short exposure ID rule and mask
- Offset: 0x1c; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0xfd80fda

Bits	Name	Access	Description
[31:28]	RESV8	RW	Reserved field Value After Reset: 0x0
[27:16]	IDMASK_DOL2	RW	Active high, DOL short exposure mask bit Value After Reset: 0xFD8
[15:12]	RESV9	RW	Reserved field Value After Reset: 0x0
[11:0]	IDCODE_DOL2	RW	DOL short exposure ID code bit Value After Reset: 0xFDA

2.5.2.9 G1_HDRCTRL4

- Description: HDR control register 2: Sony DOL very short exposure ID rule and mask
- Offset: 0x20; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0xfd80fdc

Bits	Name	Access	Description
[31:28]	RESV10	RW	Reserved field Value After Reset: 0x0
[27:16]	IDMASK_DOL3	RW	Active high, DOL very short exposure mask bit Value After Reset: 0xFD8
[15:12]	RESV11	RW	Reserved field Value After Reset: 0x0
[11:0]	IDCODE_DOL3	RW	DOL very short exposure ID code bit Value After Reset: 0xFDC

2.5.2.10 G1_ERR_MASK

- Description: Error and interrupt mask control register
- Offset: 0x24; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910

- Default Value: 0x1f0

Bits	Name	Access	Description
[31:10]	RESV12	RW	Reserved field Value After Reset: 0x0
[9]	INTERRUPT	W1C	Active high Value After Reset: 0x0
[8:4]	MASK	RW	Active high. Write 1 to mask the interrupt. mask[0]: pixenoverlap_err_mask mask[1]: vsynoverlap_err_mask mask[2]: hdroverlap_err_mask mask[3]: doloverlap_err_mask mask[4]: interrupt_mask Value After Reset: 0x1F
[3]	DOLOVERLAP_ERR	W1C	Active high, DOL Vsync and pixen overlap error Value After Reset: 0x0
[2]	HDROVERLAP_ERR	W1C	Active high, HDR Vsync and pixen overlap error Value After Reset: 0x0
[1]	VSYNCOVERLAP_ERR	W1C	Active high, HDR Vsync overlap error Value After Reset: 0x0
[0]	PIXENOVERLAP_ERR	W1C	Active high, HDR pixen overlap error Value After Reset: 0x0

2.5.2.11 G1_VMARGINCFG_IPI1

- Description: Vertical margin parameter configuration register
- Offset: 0x28; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	RESV13	RW	Reserved field Value After Reset: 0x0
[28:16]	IPI1_VBP	RW	Vertical margin of VBP, default 0 Value After Reset: 0x0
[15:13]	RESV14	RW	Reserved field Value After Reset: 0x0

Bits	Name	Access	Description
[12:0]	IPI1_VFP	RW	Vertical margin of VFP, default 0 Value After Reset: 0x0

2.5.2.12 G1_HMARGINCFG_IPI1

- Description: Horizontal margin parameter configuration register
- Offset: 0x2c; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	RESV15	RW	Reserved field Value After Reset: 0x0
[28:16]	IPI1_HBP	RW	Vertical margin of HBP, default 0 Value After Reset: 0x0
[15:13]	RESV16	RW	Reserved field Value After Reset: 0x0
[12:0]	IPI1_HFP	RW	Vertical margin of HFP, default 0 Value After Reset: 0x0

2.5.2.13 G1_VMARGINCFG_IPI2

- Description: Vertical margin parameter configuration register
- Offset: 0x30; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	RESV17	RW	Reserved field Value After Reset: 0x0
[28:16]	IPI2_VBP	RW	Vertical margin of VBP, default 0 Value After Reset: 0x0
[15:13]	RESV18	RW	Reserved field Value After Reset: 0x0
[12:0]	IPI2_VFP	RW	Vertical margin of VFP, default 0 Value After Reset: 0x0

2.5.2.14 G1_HMARGINCFG_IPI2

- Description: Horizontal margin parameter configuration register

- Offset: 0x34; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	RESV19	RW	Reserved field Value After Reset: 0x0
[28:16]	IPI2_HBP	RW	Vertical margin of HBP, default 0 Value After Reset: 0x0
[15:13]	RESV20	RW	Reserved field Value After Reset: 0x0
[12:0]	IPI2_HFP	RW	Vertical margin of HFP, default 0 Value After Reset: 0x0

2.5.2.15 G1_VMARGINCFG_IPI3

- Description: Vertical margin parameter configuration register
- Offset: 0x38; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	RESV21	RW	Reserved field Value After Reset: 0x0
[28:16]	IPI3_VBP	RW	Vertical margin of VBP, default 0 Value After Reset: 0x0
[15:13]	RESV22	RW	Reserved field Value After Reset: 0x0
[12:0]	IPI3_VFP	RW	Vertical margin of VFP, default 0 Value After Reset: 0x0

2.5.2.16 G1_HMARGINCFG_IPI3

- Description: Horizontal margin parameter configuration register
- Offset: 0x3c; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	RESV23	RW	Reserved field Value After Reset: 0x0

Bits	Name	Access	Description
[28:16]	IPI3_HBP	RW	Vertical margin of HBP, default 0 Value After Reset: 0x0
[15:13]	RESV24	RW	Reserved field Value After Reset: 0x0
[12:0]	IPI3_HFP	RW	Vertical margin of HFP, default 0 Value After Reset: 0x0

2.5.2.17 G1_RESCFG2

- Description: Resolution parameter configuration register. Note that the resolution parameter here is the actual resolution passed by the IPI2 interface including margin information.
- Offset: 0x40; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x7800438

Bits	Name	Access	Description
[31:29]	RESV25	RW	Reserved field Value After Reset: 0x0
[28:16]	IPI2_HORIZON	RW	Horizontal resolution with margin, default 1920 Value After Reset: 0x780
[15:13]	RESV25_5	RW	Reserved field Value After Reset: 0x0
[12:0]	IPI2_VERTICAL	RW	Vertical resolution with margin, default 1080 Value After Reset: 0x438

2.5.2.18 G1_RESCFG3

- Description: Resolution parameter configuration register. Note that the resolution parameter here is the actual resolution passed by the IPI3 interface including margin information.
- Offset: 0x44; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x7800438

Bits	Name	Access	Description
[31:29]	RESV26	RW	Reserved field Value After Reset: 0x0
[28:16]	IPI3_HORIZON	RW	Horizontal resolution with margin, default 1920 Value After Reset: 0x780
[15:13]	RESV26_5	RW	Reserved field

Bits	Name	Access	Description
			Value After Reset: 0x0
[12:0]	IPI3_VERTICAL	RW	Vertical resolution with margin, default 1080 Value After Reset: 0x438

2.5.2.19 G2_RESEV

- Description: MUX3_2 configuration register
- Offset: 0x48; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	G2_RESV1	RW	Reserved field Value After Reset: 0x0

2.5.2.20 G2_MODSEL

- Description: Mode select configuration register
- Offset: 0x4c; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x0

Bits	Name	Access	Description
[31:3]	G2_RESV2	RW	Reserved field Value After Reset: 0x0
[2:0]	G2_MODSEL	RW	Select which mode of sensor. 000|101|111: Normal signal exposure mode 001: Normal HDR 2-frame mode 010: Normal HDR 3-frame mode 011: Sony DOL HDR 2-frame mode 100: Sony DOL HDR 3-frame mode Value After Reset: 0x0

2.5.2.21 G2_IDNUM

- Description: ISP ID number configuration register. Configures the ID numbers of the IPI interface for long, short and very short explosure to 0\1\2 respectively.
- Offset: 0x50; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x924

Bits	Name	Access	Description
[31:12]	G2_RESV3	RW	Reserved field Value After Reset: 0x0
[11:10]	G2_ID_THIRD_VSYNC	RW	ID corresponding to the third Vsync of ISP Value After Reset: 0x2
[9:8]	G2_ID_SECOND_VSYNC	RW	ID corresponding to the second Vsync of ISP Value After Reset: 0x1
[7:6]	G2_ID_FIRST_VSYNC	RW	ID corresponding to the first Vsync of ISP Value After Reset: 0x0
[5:4]	G2_ID3	RW	For HDR mode: ID corresponding to pixen of IPI3 For DOL mode: ID corresponding to the very short exposure ISP hsync Value After Reset: 0x2
[3:2]	G2_ID2	RW	For HDR mode: ID corresponding to pixen of IPI2 For DOL mode: ID corresponding to the short exposure ISP hsync Value After Reset: 0x1
[1:0]	G2_ID1	RW	For HDR mode: ID corresponding to pixen of IPI1 For DOL mode: ID corresponding to the long exposure ISP hsync Value After Reset: 0x0

2.5.2.22 G2_RESCFG

- Description: Resolution parameter configuration register. Note that the resolution parameter here is the actual resolution passed by the IPI1 interface including margin information.
- Offset: 0x54; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x7800438

Bits	Name	Access	Description
[31:29]	G2_RESV4	RW	Reserved field Value After Reset: 0x0
[28:16]	G2_IPI1_HORIZON	RW	Horizontal resolution with margin, default 1920 Value After Reset: 0x780
[15:13]	G2_RESV4_5	RW	Reserved field Value After Reset: 0x0

Bits	Name	Access	Description
[12:0]	G2_IPI1_VERTICAL	RW	Vertical resolution with margin, default 1080 Value After Reset: 0x438

2.5.2.23 G2_HDRCTRL0

- Description: HDR control register 0
- Offset: 0x58; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2

Bits	Name	Access	Description
[31:29]	G2_RESV5	RW	Reserved field Value After Reset: 0x0
[28:27]	G2_STROBE4_1	RW	Strobe 4 of 1 in Sony ID column 00: Column 1 as ID data 01: Column 2 as ID data 10: Column 3 as ID data 11: Column 4 as ID data Value After Reset: 0x0
[26:14]	G2_VSYNC_POSEDGENUM_SECOND	RW	Exists: vsyncen==1; range from 0 to 8191 This value is used to set the second hand generated Vsync pulse to be generated after which several IPI pixen rising edges. Value After Reset: 0x0
[13:1]	G2_VSYNC_DELAY_SECOND	RW	Exists: vsyncen==1; range from 1 to 8191 This (value+3) is used to set the number of cycles delay between the last count rising edge of IPI pixen and the generating of third hand generated Vsync pulse. Value After Reset: 0x1
[0]	G2_VSYNCEN	RW	Select whether the other exposure frames under multi-exposure need to be generated by hardware. 1: Enable hardware generation 0: Disable Value After Reset: 0x0

2.5.2.24 G2_HDRCTRL1

- Description: HDR control register 1
- Offset: 0x5c; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910

- Default Value: 0x8

Bits	Name	Access	Description
[31:27]	G2_RESV6	RW	Reserved field Value After Reset: 0x0
[26:14]	G2_VSYNC_POSEDGENUM_THIRD	RW	Exists: vsyncen==1; range from 0 to 8191 This value is used to set the third hand generated Vsync pulse to be generated after which several IPI pixen rising edges. Value After Reset: 0x0
[13:1]	G2_VSYNC_DELAY_THIRD	RW	Exists: vsyncen==1; range from 3 to 8191 This (value+3) is used to set the number of cycles delay between the last count rising edge of IPI pixen and the generating of third hand generated Vsync pulse. Value After Reset: 0x4
[0]	G2_RESV6_5	RW	Value After Reset: 0x0

2.5.2.25 G2_HDRCTRL2

- Description: HDR control register 2: Sony DOL long exposure ID rule and mask
- Offset: 0x60; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0xfd80fd9

Bits	Name	Access	Description
[31:28]	G2_RESV7	RW	Reserved field Value After Reset: 0x0
[27:16]	G2_IDMASK_DOL1	RW	Active high, DOL long exposure mask bit Value After Reset: 0xFD8
[15:12]	G2_RESV7_5	RW	Reserved field Value After Reset: 0x0
[11:0]	G2_IDCODE_DOL1	RW	DOL long exposure ID code bit Value After Reset: 0xFD9

2.5.2.26 G2_HDRCTRL3

- Description: HDR control register 2: Sony DOL short exposure ID rule and mask
- Offset: 0x64; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0xfd80fda

Bits	Name	Access	Description
[31:28]	G2_RESV8	RW	Reserved field Value After Reset: 0x0
[27:16]	G2_IDMASK_DOL2	RW	Active high, DOL short exposure mask bit Value After Reset: 0xFD8
[15:12]	G2_RESV9	RW	Reserved field Value After Reset: 0x0
[11:0]	G2_IDCODE_DOL2	RW	DOL short exposure ID code bit Value After Reset: 0xFDA

2.5.2.27 G2_HDRCTRL4

- Description: HDR control register 2: Sony DOL very short exposure ID rule and mask
- Offset: 0x68; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0xfd80fdc

Bits	Name	Access	Description
[31:28]	G2_RESV10	RW	Reserved field Value After Reset: 0x0
[27:16]	G2_IDMASK_DOL3	RW	Active high, DOL very short exposure mask bit Value After Reset: 0xFD8
[15:12]	G2_RESV11	RW	Reserved field Value After Reset: 0x0
[11:0]	G2_IDCODE_DOL3	RW	DOL very short exposure ID code bit Value After Reset: 0xFDC

2.5.2.28 G2_ERR_MASK

- Description: Error and interrupt mask control register
- Offset: 0x6c; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x1f0

Bits	Name	Access	Description
[31:10]	G2_RESV12	RW	Reserved field Value After Reset: 0x0
[9]	G2_INTERRUPT	W1C	Active high Value After Reset: 0x0

Bits	Name	Access	Description
[8:4]	G2_MASK	RW	Active high. Write 1 to mask the interrupt. mask[0]: pixenoverlap_err_mask mask[1]: vsynoverlap_err_mask mask[2]: hdroverlap_err_mask mask[3]: doloverlap_err_mask mask[4]: interrupt_mask Value After Reset: 0x1F
[3]	G2_DOLOVERLAP_ERR	W1C	Active high, DOL Vsync and pixen overlap error Value After Reset: 0x0
[2]	G2_HDROVERLAP_ERR	W1C	Active high, HDR Vsync and pixen overlap error Value After Reset: 0x0
[1]	G2_VSYNCOVERLAP_ERR	W1C	Active high, HDR Vsync overlap error Value After Reset: 0x0
[0]	G2_PIXENOVERLAP_ERR	W1C	Active high, HDR pixen overlap error Value After Reset: 0x0

2.5.2.29 G2_VMARGINCFG_IPI1

- Description: Vertical margin parameter configuration register
- Offset: 0x70; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	G2_RESV13	RW	Reserved field Value After Reset: 0x0
[28:16]	G2_IPI1_VBP	RW	Vertical margin of VBP, default 0 Value After Reset: 0x0
[15:13]	G2_RESV14	RW	Reserved field Value After Reset: 0x0
[12:0]	G2_IPI1_VFP	RW	Vertical margin of VFP, default 0 Value After Reset: 0x0

2.5.2.30 G2_HMARGINCFG_IPI1

- Description: Horizontal margin parameter configuration register
- Offset: 0x74; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910

- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	G2_RESV15	RW	Reserved field Value After Reset: 0x0
[28:16]	G2_IPI1_HBP	RW	Vertical margin of HBP, default 0 Value After Reset: 0x0
[15:13]	G2_RESV16	RW	Reserved field Value After Reset: 0x0
[12:0]	G2_IPI1_HFP	RW	Vertical margin of HFP, default 0 Value After Reset: 0x0

2.5.2.31 G2_VMARGINCFG_IPI2

- Description: Vertical margin parameter configuration register
- Offset: 0x78; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	G2_RESV17	RW	Reserved field Value After Reset: 0x0
[28:16]	G2_IPI2_VBP	RW	Vertical margin of VBP, default 0 Value After Reset: 0x0
[15:13]	G2_RESV18	RW	Reserved field Value After Reset: 0x0
[12:0]	G2_IPI2_VFP	RW	Vertical margin of VFP, default 0 Value After Reset: 0x0

2.5.2.32 G2_HMARGINCFG_IPI2

- Description: Horizontal margin parameter configuration register
- Offset: 0x7c; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	G2_RESV19	RW	Reserved field Value After Reset: 0x0
[28:16]	G2_IPI2_HBP	RW	Vertical margin of HBP, default 0

Bits	Name	Access	Description
			Value After Reset: 0x0
[15:13]	G2_RESV20	RW	Reserved field Value After Reset: 0x0
[12:0]	G2_IPI2_HFP	RW	Vertical margin of HFP, default 0 Value After Reset: 0x0

2.5.2.33 G2_VMARGINCFG_IPI3

- Description: Vertical margin parameter configuration register
- Offset: 0x80; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	G2_RESV21	RW	Reserved field Value After Reset: 0x0
[28:16]	G2_IPI3_VBP	RW	Vertical margin of VBP, default 0 Value After Reset: 0x0
[15:13]	G2_RESV22	RW	Reserved field Value After Reset: 0x0
[12:0]	G2_IPI3_VFP	RW	Vertical margin of VFP, default 0 Value After Reset: 0x0

2.5.2.34 G2_HMARGINCFG_IPI3

- Description: Horizontal margin parameter configuration register
- Offset: 0x84; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	G2_RESV23	RW	Reserved field Value After Reset: 0x0
[28:16]	G2_IPI3_HBP	RW	Vertical margin of HBP, default 0 Value After Reset: 0x0
[15:13]	G2_RESV24	RW	Reserved field Value After Reset: 0x0
[12:0]	G2_IPI3_HFP	RW	Vertical margin of HFP, default 0

Bits	Name	Access	Description
			Value After Reset: 0x0

2.5.2.35 G2_RESCFG2

- Description: Resolution parameter configuration register. Note that the resolution parameter here is the actual resolution passed by the IPI2 interface including margin information.
- Offset: 0x88; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x7800438

Bits	Name	Access	Description
[31:29]	G2_RESV25	RW	Reserved field Value After Reset: 0x0
[28:16]	G2_IPI2_HORIZON	RW	Horizontal resolution with margin, default 1920 Value After Reset: 0x780
[15:13]	G2_RESV25_5	RW	Reserved field Value After Reset: 0x0
[12:0]	G2_IPI2_VERTICAL	RW	Vertical resolution with margin, default 1080 Value After Reset: 0x438

2.5.2.36 G2_RESCFG3

- Description: Resolution parameter configuration register. Note that the resolution parameter here is the actual resolution passed by the IPI3 interface including margin information.
- Offset: 0x8c; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x7800438

Bits	Name	Access	Description
[31:29]	G2_RESV26	RW	Reserved field Value After Reset: 0x0
[28:16]	G2_IPI3_HORIZON	RW	Horizontal resolution with margin, default 1920 Value After Reset: 0x780
[15:13]	G2_RESV26_5	RW	Reserved field Value After Reset: 0x0
[12:0]	G2_IPI3_VERTICAL	RW	Vertical resolution with margin, default 1080 Value After Reset: 0x438

2.5.2.37 ISPSEL

- Description: Select GLUE of ISP to bypass or not.
- Offset: 0x90
- Default Value: 0x0

Bits	Name	Access	Description
[31:2]	RESV27	RW	Reserved field Value After Reset: 0x0
[1:0]	ISPN2DW	RW	Select whether to choose bypass mode, default bypass mode. Ispn2dw[0]: Default 0, bypass mode, mux3_3 output bypass to DVP1. 1: Non bypass mode Ispn2dw[1]: Default 0, bypass mode, mux3_3 output bypass to DVP2. 1: Non bypass mode Value After Reset: 0x0

2.5.2.38 G0_RESEV

- Description: MUX3_2 configuration register
- Offset: 0x150
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	G0_RES	RW	Reserved field Value After Reset: 0x0

2.5.2.39 G0_MODSEL

- Description: Mode select configuration register
- Offset: 0x154
- Default Value: 0x0

Bits	Name	Access	Description
[31:3]	G0_RESV2	RW	Reserved field Value After Reset: 0x0
[2:0]	G0_MODSEL	RW	Select which mode of sensor.

Bits	Name	Access	Description
			000|101|111: Normal signal exposure mode 001: Normal HDR 2-frame mode 010: Normal HDR 3-frame mode 011: Sony DOL HDR 2-frame mode 100: Sony DOL HDR 3-frame mode Value After Reset: 0x0

2.5.2.40 G0_IDNUM

- Description: ISP ID number configuration register. Configures the ID numbers of the IPI interface for long, short and very short explosure to 0\1\2 respectively.
- Offset: 0x158
- Default Value: 0x924

Bits	Name	Access	Description
[31:12]	G0_RESV3	RW	Reserved field Value After Reset: 0x0
[11:10]	G0_ID_THIRD_VSYNC	RW	ID corresponding to the third Vsync of ISP Value After Reset: 0x2
[9:8]	G0_ID_SECOND_VSYNC	RW	ID corresponding to the second Vsync of ISP Value After Reset: 0x1
[7:6]	G0_ID_FIRST_VSYNC	RW	ID corresponding to the first Vsync of ISP Value After Reset: 0x0
[5:4]	G0_ID3	RW	For HDR mode: ID corresponding to pixen of IPI3 For DOL mode: ID corresponding to the very short exposure ISP hsync Value After Reset: 0x2
[3:2]	G0_ID2	RW	For HDR mode: ID corresponding to pixen of IPI2 For DOL mode: ID corresponding to the short exposure ISP hsync Value After Reset: 0x1
[1:0]	G0_ID1	RW	For HDR mode: ID corresponding to pixen of IPI1 For DOL mode: ID corresponding to the long exposure ISP hsync Value After Reset: 0x0

2.5.2.41 G0_RESCFG

- Description: Resolution parameter configuration register. Note that the resolution parameter here is the actual resolution passed by the IPI1 interface including margin information.
- Offset: 0x15c
- Default Value: 0x7800438

Bits	Name	Access	Description
[31:29]	G0_RESV4	RW	Reserved field Value After Reset: 0x0
[28:16]	G0_IPI1_HORIZON	RW	Horizontal resolution with margin, default 1920 Value After Reset: 0x780
[15:13]	G0_RESV4_5	RW	Reserved field Value After Reset: 0x0
[12:0]	G0_IPI1_VERTICAL	RW	Vertical resolution with margin, default 1080 Value After Reset: 0x438

2.5.2.42 G0_HDRCTRL0

- Description: HDR control register 0
- Offset: 0x160
- Default Value: 0x2

Bits	Name	Access	Description
[31:29]	G0_RESV5	RW	Reserved field Value After Reset: 0x0
[28:27]	G0_STROBE4_1	RW	Strobe 4 of 1 in Sony ID column 00: Column 1 as ID data 01: Column 2 as ID data 10: Column 3 as ID data 11: Column 4 as ID data Value After Reset: 0x0
[26:14]	G0_VSYNC_POSEDGENUM_SECOND	RW	Exists: vsyncen==1; range from 0 to 8191 This value is used to set the second hand generated Vsync pulse to be generated after which several IPI pixen rising edges. Value After Reset: 0x0
[13:1]	G0_VSYNC_DELAY_SECOND	RW	Exists: vsyncen==1; range from 1 to 8191 This (value+3) is used to set the number of cycles delay

Bits	Name	Access	Description
			between the last count rising edge of IPI pixen and the generating of third hand generated Vsync pulse. Value After Reset: 0x1
[0]	G0_VSYNCEN	RW	Select whether the other exposure frames under multi-exposure need to be generated by hardware. 1: Enable hardware generation 0: Disable Value After Reset: 0x0

2.5.2.43 G0_HDRCTRL1

- Description: HDR control register 1
- Offset: 0x164
- Default Value: 0x8

Bits	Name	Access	Description
[31:27]	G0_RESV6	RW	Reserved field Value After Reset: 0x0
[26:14]	G0_VSYNC_POSEDGENUM_THIRD	RW	Exists: vsyncen==1; range from 0 to 8191 This value is used to set the third hand generated Vsync pulse to be generated after which several IPI pixen rising edges. Value After Reset: 0x0
[13:1]	G0_VSYNC_DELAY_THIRD	RW	Exists: vsyncen==1; range from 3 to 8191 This (value+3) is used to set the number of cycles delay between the last count rising edge of IPI pixen and the generating of third hand generated Vsync pulse. Value After Reset: 0x4
[0]	G0_RESV6_5	RW	Value After Reset: 0x0

2.5.2.44 G0_HDRCTRL2

- Description: HDR control register 2: Sony DOL long exposure ID rule and mask
- Offset: 0x168
- Default Value: 0xfd80fd9

Bits	Name	Access	Description
[31:28]	G0_RESV7	RW	Reserved field

Bits	Name	Access	Description
			Value After Reset: 0x0
[27:16]	G0_IDMASK_DOL1	RW	Active high, DOL long exposure mask bit Value After Reset: 0xFD8
[15:12]	G0_RESV7_5	RW	Reserved field Value After Reset: 0x0
[11:0]	G0_IDCODE_DOL1	RW	DOL long exposure ID code bit Value After Reset: 0xFD9

2.5.2.45 G0_HDRCTRL3

- Description: HDR control register2: Sony DOL short exposure ID rule and mask
- Offset: 0x16c
- Default Value: 0xfd80fda

Bits	Name	Access	Description
[31:28]	G0_RESV8	RW	Reserved field Value After Reset: 0x0
[27:16]	G0_IDMASK_DOL2	RW	Active high, DOL short exposure mask bit Value After Reset: 0xFD8
[15:12]	G0_RESV9	RW	Reserved field Value After Reset: 0x0
[11:0]	G0_IDCODE_DOL2	RW	DOL short exposure ID code bit Value After Reset: 0xFDA

2.5.2.46 G0_HDRCTRL4

- Description: HDR control register 2: Sony DOL very short exposure ID rule and mask
- Offset: 0x170
- Default Value: 0xfd80fdc

Bits	Name	Access	Description
[31:28]	G0_RESV10	RW	Reserved field Value After Reset: 0x0
[27:16]	G0_IDMASK_DOL3	RW	Active high, DOL very short exposure mask bit Value After Reset: 0xFD8
[15:12]	G0_RESV11	RW	Reserved field

Bits	Name	Access	Description
			Value After Reset: 0x0
[11:0]	G0_IDCODE_DOL3	RW	DOL very short exposure ID code bit Value After Reset: 0xFDC

2.5.2.47 G0_ERR_MASK

- Description: Error and interrupt mask control register
- Offset: 0x174
- Default Value: 0x1f0

Bits	Name	Access	Description
[31:10]	G0_RESV12	RW	Reserved field Value After Reset: 0x0
[9]	G0_INTERRUPT	W1C	Active high Value After Reset: 0x0
[8:4]	G0_MASK	RW	Active high. Write 1 to mask the interrupt. mask[0]: pixenoverlap_err_mask mask[1]: vsynoverlap_err_mask mask[2]: hdroverlap_err_mask mask[3]: doloverlap_err_mask mask[4]: interrupt_mask Value After Reset: 0x1F
[3]	G0_DOLOVERLAP_ERR	W1C	Active high, DOL Vsync and pixen overlap error Value After Reset: 0x0
[2]	G0_HDROVERLAP_ERR	W1C	Active high, HDR Vsync and pixen overlap error Value After Reset: 0x0
[1]	G0_VSYNCOVERLAP_ERR	W1C	Active high, HDR Vsync overlap error Value After Reset: 0x0
[0]	G0_PIXENOVERLAP_ERR	W1C	Active high, HDR pixen overlap error Value After Reset: 0x0

2.5.2.48 G0_VMARGINCFG_IPI1

- Description: Vertical margin parameter configuration register
- Offset: 0x178
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	G0_RESV13	RW	Reserved field Value After Reset: 0x0
[28:16]	G0_IPI1_VBP	RW	Vertical margin of VBP, default 0 Value After Reset: 0x0
[15:13]	G0_RESV14	RW	Reserved field Value After Reset: 0x0
[12:0]	G0_IPI1_VFP	RW	Vertical margin of VFP, default 0 Value After Reset: 0x0

2.5.2.49 G0_HMARGINCFG_IPI1

- Description: Horizontal margin parameter configuration register
- Offset: 0x17c
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	G0_RESV15	RW	Reserved field Value After Reset: 0x0
[28:16]	G0_IPI1_HBP	RW	Vertical margin of HBP, default 0 Value After Reset: 0x0
[15:13]	G0_RESV16	RW	Reserved field Value After Reset: 0x0
[12:0]	G0_IPI1_HFP	RW	Vertical margin of HFP, default 0 Value After Reset: 0x0

2.5.2.50 G0_VMARGINCFG_IPI2

- Description: Vertical margin parameter configuration register
- Offset: 0x180
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	G0_RESV17	RW	Reserved field Value After Reset: 0x0
[28:16]	G0_IPI2_VBP	RW	Vertical margin of VBP, default 0 Value After Reset: 0x0

Bits	Name	Access	Description
[15:13]	G0_RESV18	RW	Reserved field Value After Reset: 0x0
[12:0]	G0_IPI2_VFP	RW	Vertical margin of VFP, default 0 Value After Reset: 0x0

2.5.2.51 G0_HMARGINCFG_IPI2

- Description: Horizontal margin parameter configuration register
- Offset: 0x184
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	G0_RESV19	RW	Reserved field Value After Reset: 0x0
[28:16]	G0_IPI2_HBP	RW	Vertical margin of HBP, default 0 Value After Reset: 0x0
[15:13]	G0_RESV20	RW	Reserved field Value After Reset: 0x0
[12:0]	G0_IPI2_HFP	RW	Vertical margin of HFP, default 0 Value After Reset: 0x0

2.5.2.52 G0_VMARGINCFG_IPI3

- Description: Vertical margin parameter configuration register
- Offset: 0x188
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	G0_RESV21	RW	Reserved field Value After Reset: 0x0
[28:16]	G0_IPI3_VBP	RW	Vertical margin of VBP, default 0 Value After Reset: 0x0
[15:13]	G0_RESV22	RW	Reserved field Value After Reset: 0x0
[12:0]	G0_IPI3_VFP	RW	Vertical margin of VFP, default 0 Value After Reset: 0x0

2.5.2.53 G0_HMARGINCFG_IPI3

- Description: Horizontal margin parameter configuration register
- Offset: 0x18c
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	G0_RESV23	RW	Reserved field Value After Reset: 0x0
[28:16]	G0_IPI3_HBP	RW	Vertical margin of HBP, default 0 Value After Reset: 0x0
[15:13]	G0_RESV24	RW	Reserved field Value After Reset: 0x0
[12:0]	G0_IPI3_HFP	RW	Vertical margin of HFP, default 0 Value After Reset: 0x0

2.5.2.54 G0_RESCFG2

- Description: Resolution parameter configuration register. Note that the resolution parameter here is the actual resolution passed by the IPI2 interface including margin information.
- Offset: 0x190
- Default Value: 0x7800438

Bits	Name	Access	Description
[31:29]	G0_RESV25	RW	Reserved field Value After Reset: 0x0
[28:16]	G0_IPI2_HORIZON	RW	Horizontal resolution with margin, default 1920 Value After Reset: 0x780
[15:13]	G0_RESV25_5	RW	Reserved field Value After Reset: 0x0
[12:0]	G0_IPI2_VERTICAL	RW	Vertical resolution with margin, default 1080 Value After Reset: 0x438

2.5.2.55 G0_RESCFG3

- Description: Resolution parameter configuration register. Note that the resolution parameter here is the actual resolution passed by the IPI3 interface including margin information.
- Offset: 0x194
- Default Value: 0x7800438

Bits	Name	Access	Description
[31:29]	G0_RESV26	RW	Reserved field Value After Reset: 0x0
[28:16]	G0_IPI3_HORIZON	RW	Horizontal resolution with margin, default 1920 Value After Reset: 0x780
[15:13]	G0_RESV26_5	RW	Reserved field Value After Reset: 0x0
[12:0]	G0_IPI3_VERTICAL	RW	Vertical resolution with margin, default 1080 Value After Reset: 0x438

2.5.2.56 MIPI2DMA_CTRL0

- Description: mipi2dma ctrl0
- Offset: 0x198
- Default Value: 0x0

Bits	Name	Access	Description
[31:7]	MIPI2DMA_RESV1	RW	Reserved field Value After Reset: 0x0
[6:4]	RAWMOD	RW	Default 0, 0|6|7: RAW6 1: RAW7 2: RAW8 3: RAW10 4: RAW12 5: RAW10-splicing Value After Reset: 0x0
[3]	RAWPOS	RW	0: Low bit mode (default) 1: High bit mode Value After Reset: 0x0
[2:1]	MNUM	RW	0: 1 frame (default) 1: 2 frame to cycle 2: 3 frame to cycle 3: 4 frame to cycle Value After Reset: 0x0
[0]	MNMOD	RW	0: M frame mode (default) 1: N line mode

Bits	Name	Access	Description
			Value After Reset: 0x0

2.5.2.57 MIPI2DMA_CTRL1

- Description: mipi2dma ctrl1
- Offset: 0x19c
- Default Value: 0x30001

Bits	Name	Access	Description
[31:24]	MIPI2DMA_RESV3	RW	Reserved field Value After Reset: 0x0
[23:16]	MIPI2DMA_WBURSTLEN	RW	AXI4 write burst length, (MIPI2DMA_WBURSTLEN + 1) = 4 means burstlength equal 4. Only supports for 4, 8 and 16. Value After Reset: 0x3
[15:10]	MIPI2DMA_RESV4	RW	Reserved field Value After Reset: 0x0
[9:0]	MIPI2DMA_WOSNUM	RW	AXI4 write burst outstanding, default is 1, ranges from 1~1023. Cannot configure this to 0. Value After Reset: 0x1

2.5.2.58 MIPI2DMA_CTRL2

- Description: mipi2dma ctrl2
- Offset: 0x1a0
- Default Value: 0xff8400

Bits	Name	Access	Description
[31:24]	MIPI2DMA_RESV5	RW	Reserved field Value After Reset: 0x0
[23:20]	MIPI2DMA_QOS5	RW	FIFO waterlevel higher 7/8 depth Value After Reset: 0xF
[19:16]	MIPI2DMA_QOS4	RW	FIFO waterlevel lower 7/8 depth Value After Reset: 0xF
[15:12]	MIPI2DMA_QOS3	RW	FIFO waterlevel lower ¾ depth Value After Reset: 0x8
[11:8]	MIPI2DMA_QOS2	RW	FIFO waterlevel lower ½ depth

Bits	Name	Access	Description
			Value After Reset: 0x4
[7:4]	MIPI2DMA_QOS1	RW	FIFO waterlevel lower ¼ depth Value After Reset: 0x0
[3:0]	MIPI2DMA_QOS0	RW	FIFO waterlevel lower 1/8 depth Value After Reset: 0x0

2.5.2.59 MIPI2DMA_CTRL3

- Description: mipi2dma ctrl3
- Offset: 0x1a4
- Default Value: 0x4380780

Bits	Name	Access	Description
[31:29]	MIPI2DMA_RESV6	RW	Reserved field Value After Reset: 0x0
[28:16]	VERTICAL_MIPI2DMA	RW	Every exposure vertical resolution with margin, default 1080 Value After Reset: 0x438
[15:13]	MIPI2DMA_RESV7	RW	Reserved field Value After Reset: 0x0
[12:0]	HORIZON_MIPI2DMA	RW	Every exposure horizontal resolution with margin, default 1920 Value After Reset: 0x780

2.5.2.60 MIPI2DMA_CTRL4

- Description: mipi2dma ctrl4
- Offset: 0x1a8
- Default Value: 0x1e0078

Bits	Name	Access	Description
[31:27]	BURSTREM	RW	BURSTREM = HORIZON_CNT128/(MIPI2DMA_WBURSTLEN + 1), when the remainder is 0, BURSTREM = (MIPI2DMA_WBURSTLEN + 1) Value After Reset: 0x0
[26:16]	READNUM	RW	Number of 128*burstlen for rd of 128fifo READNUM =

Bits	Name	Access	Description
			[HORIZON_CNT128/(MIPI2DMA_WBURSTLEN + 1)] Default: 30 (for RAW6&1920&burst = 4) Value After Reset: 0x1E
[15:11]	MIPI2DMA_RESV9	RW	Reserved field Value After Reset: 0x0
[10:0]	HORIZON_CNT128	RW	Number of 128 for rd of 128fifo HORIZON_CNT128 = STRIDE_min/16, STRIDE_min is the size of the address space occupied by the 16byte aligned one line (in bytes) Default: 120 (for RAW6&1920) Value After Reset: 0x78

2.5.2.61 MIPI2DMA_CTRL5

- Description: mipi2dma ctrl5
- Offset: 0x1ac
- Default Value: 0xa0014

Bits	Name	Access	Description
[31:29]	MIPI2DMA_RESV10	RW	Reserved field Value After Reset: 0x0
[28:16]	N_NLINENUM	RW	The number of lines to count for interrupt Value After Reset: 0xA
[15:13]	MIPI2DMA_RESV11	RW	Reserved field Value After Reset: 0x0
[12:0]	N_LINENUM	RW	Total number of lines of the N line mode store space, must be larger than N_NLINENUM. Value After Reset: 0x14

2.5.2.62 MIPI2DMA_CTRL6

- Description: mipi2dma ctrl6
- Offset: 0x1b0
- Default Value: 0x780

Bits	Name	Access	Description
[31:16]	MIPI2DMA_RESV12	RW	Reserved field Value After Reset: 0x0

Bits	Name	Access	Description
[15:0]	N_STRIDE	RW	The address range occupied by one line When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x780

2.5.2.63 MIPI2DMA_CTRL7

- Description: mipi2dma ctrl7
- Offset: 0x1b4
- Default Value: 0x7800780

Bits	Name	Access	Description
[31:16]	M0_STRIDE	RW	The address range occupied by one line When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x780
[15:0]	M1_STRIDE	RW	The address range occupied by one line When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x780

2.5.2.64 MIPI2DMA_CTRL8

- Description: mipi2dma ctrl8
- Offset: 0x1b8
- Default Value: 0x7800780

Bits	Name	Access	Description
[31:16]	M2_STRIDE	RW	The address range occupied by one line When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x780
[15:0]	M3_STRIDE	RW	The address range occupied by one line When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively.

Bits	Name	Access	Description
			Value After Reset: 0x780

2.5.2.65 MIPI2DMA_CTRL9

- Description: mipi2dma ctrl9
- Offset: 0x1bc
- Default Value: 0x0

Bits	Name	Access	Description
[31:3]	MIPI2DMA_RESV13	RW	Reserved field Value After Reset: 0x0
[2]	GLUE1_RSTN_PULSE	W1S	GLUE1 soft reset control Value After Reset: 0x0
[1]	GLUE2_RSTN_PULSE	W1S	GLUE2 soft reset control Value After Reset: 0x0
[0]	MIPI2DMA_RSTN_PULSE	W1S	RST for MIPI2DMA module, actual register access is W1SAC, waive the error of register test for W1S Value After Reset: 0x0

2.5.2.66 MIPI2DMA_CTRL10

- Description: mipi2dma ctrl10
- Offset: 0x1c0
- Default Value: 0x0

Bits	Name	Access	Description
[31:1]	MIPI2DMA_RESV14	RW	Reserved field Value After Reset: 0x0
[0]	MIPI2DMA_START_STOP	RW	0: Stop 1: Start to DMA copy Value After Reset: 0x0

2.5.2.67 MIPI2DMA_CTRL11

- Description: mipi2dma ctrl11
- Offset: 0x1c4
- Default Value: 0x0

Bits	Name	Access	Description
[31:3]	MIPI2DMA_RESV15	RW	Reserved field Value After Reset: 0x0
[2]	INV_FLAG_ID2	RW	Software should invert this bit very M frame done or N_LINENUM done for ID2 channel. Value After Reset: 0x0
[1]	INV_FLAG_ID1	RW	Software should invert this bit very M frame done or N_LINENUM done for ID1 channel. Value After Reset: 0x0
[0]	INV_FLAG_ID0	RW	Software should invert this bit very M frame done or N_LINENUM done for ID0 channel. Value After Reset: 0x0

2.5.2.68 MIPI2DMA_CTRL12

- Description: mipi2dma ctrl12
- Offset: 0x1c8
- Default Value: 0x0

Bits	Name	Access	Description
[31:13]	MIPI2DMA_RESV16	RW	Reserved field Value After Reset: 0x0
[12:0]	N_LINENUM_NEW_ID0	RW	New read line of N mode Value After Reset: 0x0

2.5.2.69 MIPI2DMA_CTRL13

- Description: mipi2dma ctrl13
- Offset: 0x1cc
- Default Value: 0x0

Bits	Name	Access	Description
[31:13]	MIPI2DMA_RESV17	RW	Reserved field Value After Reset: 0x0
[12:0]	N_LINENUM_NEW_ID1	RW	New read line of N mode Value After Reset: 0x0

2.5.2.70 MIPI2DMA_CTRL14

- Description: mipi2dma ctrl14

- Offset: 0x1d0
- Default Value: 0x0

Bits	Name	Access	Description
[31:13]	MIPI2DMA_RESV18	RW	Reserved field Value After Reset: 0x0
[12:0]	N_LINENUM_NEW_ID2	RW	New read line of N mode Value After Reset: 0x0

2.5.2.71 MIPI2DMA_CTRL15

- Description: mipi2dma ctrl15
- Offset: 0x1d4
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	MIPI2DMA_RESV19	RW	Reserved field Value After Reset: 0x0
[7:0]	N_SADDR_ID0_H	RW	N_SADDR_ID0[39:32] Value After Reset: 0x0

2.5.2.72 MIPI2DMA_CTRL16

- Description: mipi2dma ctrl16
- Offset: 0x1d8
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	N_SADDR_ID0_L	RW	N_SADDR_ID0[31:0] When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x0

2.5.2.73 MIPI2DMA_CTRL17

- Description: mipi2dma ctrl17
- Offset: 0x1dc
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	MIPI2DMA_RESV20	RW	Reserved field Value After Reset: 0x0
[7:0]	N_SADDR_ID1_H	RW	N_SADDR_ID1[39:32] Value After Reset: 0x0

2.5.2.74 MIPI2DMA_CTRL18

- Description: mipi2dma ctrl18
- Offset: 0x1e0
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	N_SADDR_ID1_L	RW	N_SADDR_ID1[31:0] When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x0

2.5.2.75 MIPI2DMA_CTRL19

- Description: mipi2dma ctrl19
- Offset: 0x1e4
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	MIPI2DMA_RESV21	RW	Reserved field Value After Reset: 0x0
[7:0]	N_SADDR_ID2_H	RW	N_SADDR_ID2[39:32] Value After Reset: 0x0

2.5.2.76 MIPI2DMA_CTRL20

- Description: mipi2dma ctrl20
- Offset: 0x1e8
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	N_SADDR_ID2_L	RW	N_SADDR_ID2[31:0] When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and

Bits	Name	Access	Description
			256byte alignment respectively. Value After Reset: 0x0

2.5.2.77 MIPI2DMA_CTRL21

- Description: mipi2dma ctrl21
- Offset: 0x1ec
- Default Value: 0x0

Bits	Name	Access	Description
[31:27]	MIPI2DMA_RESV22	RW	Reserved field Value After Reset: 0x0
[26:16]	N_NUM_DONE_ID1	RO	How many n line ready, frame end to clear Value After Reset: 0x0
[15:11]	MIPI2DMA_RESV23	RW	Reserved field Value After Reset: 0x0
[10:0]	N_NUM_DONE_ID0	RO	How many n line ready, frame end to clear Value After Reset: 0x0

2.5.2.78 MIPI2DMA_CTRL22

- Description: mipi2dma ctrl22
- Offset: 0x1f0
- Default Value: 0x0

Bits	Name	Access	Description
[31:11]	MIPI2DMA_RESV24	RW	Reserved field Value After Reset: 0x0
[10:0]	N_NUM_DONE_ID2	RO	How many n line ready, frame end to clear Value After Reset: 0x0

2.5.2.79 MIPI2DMA_CTRL23

- Description: mipi2dma ctrl23
- Offset: 0x1f4
- Default Value: 0x0

Bits	Name	Access	Description
[31]	MIPI2DMA_RESV25	RW	Reserved field

Bits	Name	Access	Description
			Value After Reset: 0x0
[30:29]	MNUM_NEW_ID1	RW	0: One frame overall 1: Two 2: Three 3: Four Value After Reset: 0x0
[28:16]	LINENUM_NEW_ID1	RW	New read line of M frame mode Value After Reset: 0x0
[15]	MIPI2DMA_RESV26	RW	Reserved field Value After Reset: 0x0
[14:13]	MNUM_NEW_ID0	RW	0: One frame overall 1: Two 2: Three 3: Four Value After Reset: 0x0
[12:0]	LINENUM_NEW_ID0	RW	New read line of M frame mode Value After Reset: 0x0

2.5.2.80 MIPI2DMA_CTRL24

- Description: mipi2dma ctrl24
- Offset: 0x1f8
- Default Value: 0x0

Bits	Name	Access	Description
[31:15]	MIPI2DMA_RESV27	RW	Reserved field Value After Reset: 0x0
[14:13]	MNUM_NEW_ID2	RW	0: One frame overall 1: Two 2: Three 3: Four Value After Reset: 0x0
[12:0]	LINENUM_NEW_ID2	RW	New read line of M frame mode Value After Reset: 0x0

2.5.2.81 MIPI2DMA_CTRL25

- Description: mipi2dma ctrl25
- Offset: 0x1fc
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	MIPI2DMA_RESV28	RW	Reserved field Value After Reset: 0x0
[7:0]	M0_SADDR_ID0_H	RW	M0_SADDR_ID0[39:32] Value After Reset: 0x0

2.5.2.82 MIPI2DMA_CTRL26

- Description: mipi2dma ctrl26
- Offset: 0x200
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	M0_SADDR_ID0_L	RW	M0_SADDR_ID0[31:0] When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x0

2.5.2.83 MIPI2DMA_CTRL27

- Description: mipi2dma ctrl27
- Offset: 0x204
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	MIPI2DMA_RESV29	RW	Reserved field Value After Reset: 0x0
[7:0]	M0_SADDR_ID1_H	RW	M0_SADDR_ID1[39:32] Value After Reset: 0x0

2.5.2.84 MIPI2DMA_CTRL28

- Description: mipi2dma ctrl28
- Offset: 0x208
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	M0_SADDR_ID1_L	RW	M0_SADDR_ID1[31:0] When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x0

2.5.2.85 MIPI2DMA_CTRL29

- Description: mipi2dma ctrl29
- Offset: 0x20c
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	MIPI2DMA_RESV30	RW	Reserved field Value After Reset: 0x0
[7:0]	M0_SADDR_ID2_H	RW	M0_SADDR_ID2[39:32] Value After Reset: 0x0

2.5.2.86 MIPI2DMA_CTRL30

- Description: mipi2dma ctrl30
- Offset: 0x210
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	M0_SADDR_ID2_L	RW	M0_SADDR_ID2[31:0] When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x0

2.5.2.87 MIPI2DMA_CTRL31

- Description: mipi2dma ctrl31
- Offset: 0x214
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	MIPI2DMA_RESV31	RW	Reserved field Value After Reset: 0x0

Bits	Name	Access	Description
[7:0]	M1_SADDR_ID0_H	RW	M1_SADDR_ID0[39:32] Value After Reset: 0x0

2.5.2.88 MIPI2DMA_CTRL32

- Description: mipi2dma ctrl32
- Offset: 0x218
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	M1_SADDR_ID0_L	RW	M1_SADDR_ID0[31:0] When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x0

2.5.2.89 MIPI2DMA_CTRL33

- Description: mipi2dma ctrl33
- Offset: 0x21c
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	MIPI2DMA_RESV32	RW	Reserved field Value After Reset: 0x0
[7:0]	M1_SADDR_ID1_H	RW	M1_SADDR_ID1[39:32] Value After Reset: 0x0

2.5.2.90 MIPI2DMA_CTRL34

- Description: mipi2dma ctrl34
- Offset: 0x220
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	M1_SADDR_ID1_L	RW	M1_SADDR_ID1[31:0] When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x0

2.5.2.91 MIPI2DMA_CTRL35

- Description: mipi2dma ctrl35
- Offset: 0x224
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	MIPI2DMA_RESV33	RW	Reserved field Value After Reset: 0x0
[7:0]	M1_SADDR_ID2_H	RW	M1_SADDR_ID2[39:32] Value After Reset: 0x0

2.5.2.92 MIPI2DMA_CTRL36

- Description: mipi2dma ctrl36
- Offset: 0x228
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	M1_SADDR_ID2_L	RW	M1_SADDR_ID2[31:0] When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x0

2.5.2.93 MIPI2DMA_CTRL37

- Description: mipi2dma ctrl37
- Offset: 0x22c
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	MIPI2DMA_RESV34	RW	Reserved field Value After Reset: 0x0
[7:0]	M2_SADDR_ID0_H	RW	M2_SADDR_ID0[39:32] Value After Reset: 0x0

2.5.2.94 MIPI2DMA_CTRL38

- Description: mipi2dma ctrl38
- Offset: 0x230
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	M2_SADDR_ID0_L	RW	M2_SADDR_ID0[31:0] When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x0

2.5.2.95 MIPI2DMA_CTRL39

- Description: mipi2dma ctrl39
- Offset: 0x234
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	MIPI2DMA_RESV35	RW	Reserved field Value After Reset: 0x0
[7:0]	M2_SADDR_ID1_H	RW	M2_SADDR_ID1[39:32] Value After Reset: 0x0

2.5.2.96 MIPI2DMA_CTRL40

- Description: mipi2dma ctrl40
- Offset: 0x238
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	M2_SADDR_ID1_L	RW	M2_SADDR_ID1[31:0] When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x0

2.5.2.97 MIPI2DMA_CTRL41

- Description: mipi2dma ctrl41
- Offset: 0x23c
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	MIPI2DMA_RESV36	RW	Reserved field Value After Reset: 0x0

Bits	Name	Access	Description
[7:0]	M2_SADDR_ID2_H	RW	M2_SADDR_ID2[39:32] Value After Reset: 0x0

2.5.2.98 MIPI2DMA_CTRL42

- Description: mipi2dma ctrl42
- Offset: 0x240
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	M2_SADDR_ID2_L	RW	M2_SADDR_ID2[31:0] When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x0

2.5.2.99 MIPI2DMA_CTRL43

- Description: mipi2dma ctrl43
- Offset: 0x244
- Default Value: 0x0

Bits	Name	Access	Description
[31:12]	MIPI2DMA_RESV37	RW	Reserved field Value After Reset: 0x0
[11]	M_FRAME_DONE_STATUS_ID0_0	W1C	Status of frame done Value After Reset: 0x0
[10]	M_FRAME_DONE_STATUS_ID0_1	W1C	Status of frame done Value After Reset: 0x0
[9]	M_FRAME_DONE_STATUS_ID0_2	W1C	Status of frame done Value After Reset: 0x0
[8]	M_FRAME_DONE_STATUS_ID0_3	W1C	Status of frame done Value After Reset: 0x0
[7]	M_FRAME_DONE_STATUS_ID1_0	W1C	Status of frame done Value After Reset: 0x0
[6]	M_FRAME_DONE_STATUS_ID1_1	W1C	Status of frame done Value After Reset: 0x0

Bits	Name	Access	Description
[5]	M_FRAME_DONE_STATUS_ID1_2	W1C	Status of frame done Value After Reset: 0x0
[4]	M_FRAME_DONE_STATUS_ID1_3	W1C	Status of frame done Value After Reset: 0x0
[3]	M_FRAME_DONE_STATUS_ID2_0	W1C	Status of frame done Value After Reset: 0x0
[2]	M_FRAME_DONE_STATUS_ID2_1	W1C	Status of frame done Value After Reset: 0x0
[1]	M_FRAME_DONE_STATUS_ID2_2	W1C	Status of frame done Value After Reset: 0x0
[0]	M_FRAME_DONE_STATUS_ID2_3	W1C	Status of frame done Value After Reset: 0x0

2.5.2.100 MIPI2DMA_CTRL44

- Description: mipi2dma ctrl44
- Offset: 0x248
- Default Value: 0x3f0000

Bits	Name	Access	Description
[31:22]	MIPI2DMA_RESV38	RW	Reserved field Value After Reset: 0x0
[21]	BUSERR_MASK	RW	Write 0 to open the interrupt. Value After Reset: 0x1
[20]	FIFO_OVERERR_MASK	RW	Write 0 to open the interrupt. Value After Reset: 0x1
[19]	IDLE_DONE_MASK	RW	Write 0 to open the interrupt. Value After Reset: 0x1
[18]	MN_OVERERR_MASK	RW	Write 0 to open the interrupt. Value After Reset: 0x1
[17]	NLINE_DONE_MASK	RW	Write 0 to open the interrupt. Value After Reset: 0x1
[16]	MFRAME_DONE_MASK	RW	Write 0 to open the interrupt. Value After Reset: 0x1

Bits	Name	Access	Description
[15:9]	MIPI2DMA_RESV39	RW	Reserved field Value After Reset: 0x0
[8]	N_FRAME_END_STATE_P_ID0	W1C	id0 channel N frame end state Value After Reset: 0x0
[7]	N_FRAME_END_STATE_P_ID1	W1C	id1 channel N frame end state Value After Reset: 0x0
[6]	N_FRAME_END_STATE_P_ID2	W1C	id2 channel N frame end state Value After Reset: 0x0
[5]	BUSERR_INT	W1C	Bus error interrupt state Value After Reset: 0x0
[4]	FIFO_OVERERR_REQ_INT	W1C	FIFO overflow error interrupt state Value After Reset: 0x0
[3]	INT_IDLE_DONE_INT	W1C	Bus idle done interrupt state Value After Reset: 0x0
[2]	NM_OVERERR_REQ_INT	W1C	Data cover error interrupt state Value After Reset: 0x0
[1]	N_LINE_DONE_INT	W1C	N line done interrupt state Value After Reset: 0x0
[0]	M_FRAME_DONE_INT	W1C	M frame done interrupt state Value After Reset: 0x0

2.5.2.101 MIPI2DMA_CTRL45

- Description: mipi2dma ctrl45
- Offset: 0x24c
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	MIPI2DMA_RESV40	RW	Reserved field Value After Reset: 0x0
[7:0]	M3_SADDR_ID0_H	RW	M3_SADDR_ID0_H Value After Reset: 0x0

2.5.2.102 MIPI2DMA_CTRL46

- Description: mipi2dma ctrl46
- Offset: 0x250
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	M3_SADDR_ID0_L	RW	M3_SADDR_ID0_L When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x0

2.5.2.103 MIPI2DMA_CTRL47

- Description: mipi2dma ctrl47
- Offset: 0x254
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	MIPI2DMA_RESV41	RW	Reserved field Value After Reset: 0x0
[7:0]	M3_SADDR_ID1_H	RW	M3_SADDR_ID1_H Value After Reset: 0x0

2.5.2.104 MIPI2DMA_CTRL48

- Description: mipi2dma ctrl48
- Offset: 0x258
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	M3_SADDR_ID1_L	RW	M3_SADDR_ID1_L When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x0

2.5.2.105 MIPI2DMA_CTRL49

- Description: mipi2dma ctrl49
- Offset: 0x25c

- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	MIPI2DMA_RESV42	RW	Reserved field Value After Reset: 0x0
[7:0]	M3_SADDR_ID2_H	RW	M3_SADDR_ID2_H Value After Reset: 0x0

2.5.2.106 MIPI2DMA_CTRL50

- Description: mipi2dma ctrl50
- Offset: 0x260
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	M3_SADDR_ID2_L	RW	M3_SADDR_ID2_L When MIPI2DMA_BURSTLEN is 4, 8, 16, address alignment requirements are 64byte, 128byte and 256byte alignment respectively. Value After Reset: 0x0

2.5.2.107 MIPI2DMA_CTRL51

- Description: mipi2dma ctrl51
- Offset: 0x264
- Default Value: 0x1

Bits	Name	Access	Description
[31:2]	MIPI2DMA_RESV43	RW	Reserved field Value After Reset: 0x0
[1]	FLAG_OF_CROSS_4K	W1C	Flag to indicate if there has cross 4K situation or not. Value After Reset: 0x0
[0]	CROSS_4K_EN	RW	Enable cross 4K function or not. 1: Enable (default) 0: Disable Value After Reset: 0x1

3 ISP

3.1 Overview

ISP supports simple CMOS sensors delivering RGB Bayer or RGBIR Bayer pattern without any integrated image process. ISP contains basic image processing, such as LSC, DPCC, Demosaic, 3A; as well as the advanced features, such as HDR, WDR, 3DNR, scaling, and compression functions.

3.2 Main Features

ISP basic features:

- DVP Camera Sensor Input Interface
- Test Pattern Generator (TPG)
- Black Level Compensation
- Sensor Linear Correction
- Defect Pixel Cluster Correction (DPCC)
- Green Equalization
- Lens Shade Correction (De-Vignetting)
- Digital Gain
- 2-Stage Adaptive Noise Filter (Noise reduction, Sharpness, Blurring)
- Enhanced Color Interpolation (Bayer De-mosaic filter)
- Chromatic Aberration Correction (CAC)
- Color Correction (Xtalk) Matrix (CCM)
- Color Space Conversion (CSC)
- Programmable Gamma correction for sensor adaptation and display correction
- Auto Focus (AF)measurement
- Auto White Balance (AWB) measurement
- Auto Exposure (AE) measurement
- Histogram Calculation
- Anti-flicker
- Cropping of the output picture (to crop interpolation artifacts), also used for windowing
- Color Processing: Contrast, Saturation, Brightness, Hue (CPROC)
- Sharpen/Blur Filter

ISP Advanced features:

- WDR in single wide dynamic frame
- Multi-exposure HDR (Native/Built-in HDR interface, 12~16-bit HDR input, Compand output)
- CPD, compand function to support native HDR sensor which performs HDR merging in sensor
- Variable sensor interface for RGB-Bayer sensors, DOL or stagger HDR sensors
- 20-bit HDR Processing, includes multi-exposure stitching and local tone mapping

- Advanced 2DNR spatial noise reduction
- Advanced 3DNR: spatial and temporal noise reduction
- Video Stabilization (VSM)
- RGB-IR 4x4 pattern

ISP performance or capability:

- Dual-ISP with Shared Memory Pool (SMP)
  - Dual ISP 4k@30fps->15fps HDR
  - One ISP 4k@60fps->30fps HDR, the other ISP no HDR
- 8bit to16bit Bayer RAW interface support
- Up to 12M (4096x3072)@30fps support
- Up to 3 output each ISP with different scaling factors and cropping

3.3 Function Description

3.3.1 ISP Overview

Figure & Table 3-1 shows the data process order of a single ISP. There are dual ISP inside the SoC. Inside a single ISP, RAW data from sensor interface or memory interface, will be processed by RAW pipeline, RGB pipeline and YUV pipeline, and then the final data will be stored into the external memory in YUV or RGB format. Meanwhile, there is also a RAW data path before Demosaic to store the RAW data into the external memory.

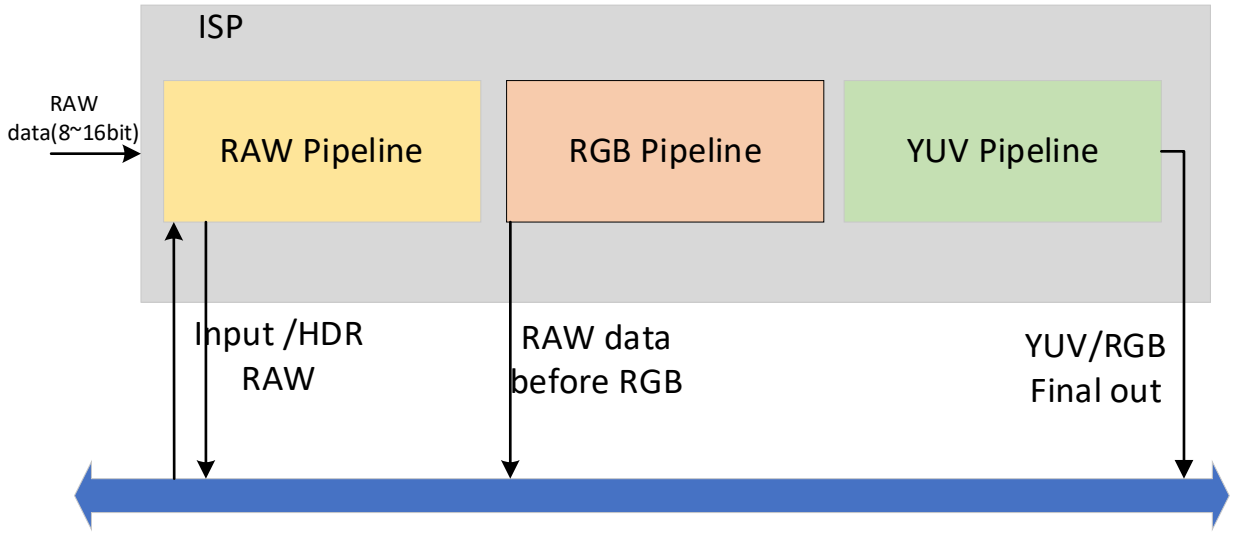


Figure & Table 3-1 ISP pipeline

3.3.2 Input Format Support

3.3.2.1 Sensor Inputs

The sensor interface is implemented with separated horizontal and vertical synchronization inputs. Supported video formats are:

- RGB bayer data

- RGB-IR 4x4 pattern
- Compand HDR data
- Multi-exposure HDR data with virtual channel information

3.3.2.2 DMA Inputs from System Memory

In DMA mode, data coming from the system memory can be read and processed by the ISP pipeline. Data should be RAW data, from 8-bit to 16-bit.

3.3.3 Output Format Support

3.3.3.1 Main Path Interface

Main path supports full resolution output, up to 4096*3072 resolution.
The following output data formats are supported:

- YUV422 or YUV420 either planar or semi-planar or interleaved
- RGB888 format either planar or interleaved
  Restriction: Only one path can output RGB888 for main/self path1/self path2
- 8 to 10 bit IR data
- Support data compression

3.3.3.2 Self Path 1/2 Interface

Self path1/2 supports downscaled resolution output, up to 1920*1080 resolution.

- YUV422 or YUV420 either planar or semi-planar or interleaved
- RGB888 format either planar or interleaved
  Restriction: only one path can be output RGB888 for main/self path1/self path2
- 8 to 10 bit IR data
- Support data compression

3.3.3.3 RAW Interface

There are 2 RAW data paths:

- When the RAW data comes from sensor, it can be stored into the external memory without any ISP process.
- RAW data after ISP RAW pipeline also can be stored into the external memory.

4 IVS

4.1 Overview

IVS is to realize the handshake interaction between ISP and VENC. The functional block diagram of IVS is given in Figure & Table 4-1.

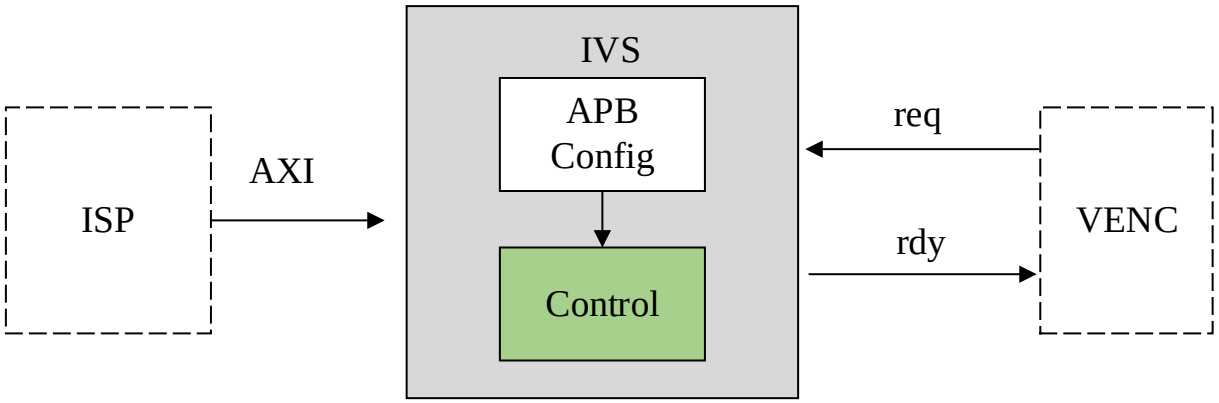


Figure & Table 4-1 IVS functional block diagram

4.2 Main Features

The main features of IVS are as follows:

- Configures parameters by APB.
- The range of encoding picture: 136x136-4096x4096.
- The number of encode lines can be configured, and the typical configuration is 16 or 64.
- Supports to detect overflow.

4.3 Function Description

4.3.1 Supported Picture Format

The module only supports the YUV420 semi-planar as Figure & Table 4-2, where Y and UV are stored separately, but U and V are cross-stored.

Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8
Y9	Y10	Y11	Y12	Y13	Y14	Y15	Y16
Y17	Y18	Y19	Y20	Y21	Y22	Y23	Y24
Y25	Y26	Y27	Y28	Y29	Y30	Y31	Y32
U1	V1	U2	V2	U3	V3	U4	V4
U5	V5	U6	V6	U7	V7	U8	V8

Figure & Table 4-2 YUV420 semi-planar

4.4 Usage

4.4.1 Flow Diagram

The basic operation flow of IVS is shown in Figure & Table 4-3:

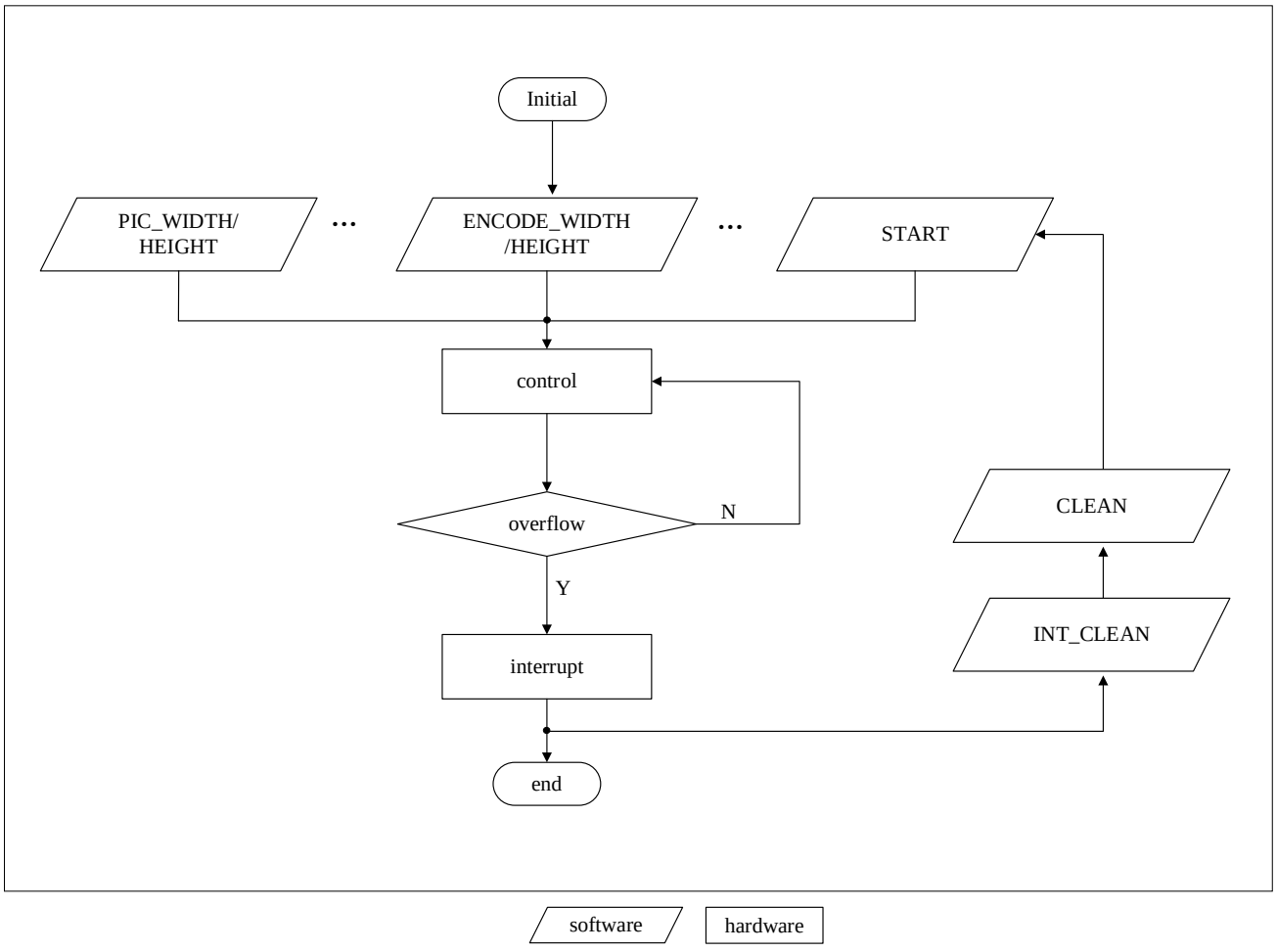


Figure & Table 4-3 Flow diagram

Initialize each basic configuration register of IVS, and finally configure the START register. Then the module starts to work. Once the SRAM overflows, it will trigger an interrupt, configure the INT_CLEAN and CLEAR registers. At the beginning of the next frame, configure the START register.

NOTE

- START must be the last configuration signal, and at the end of the current frame and the beginning of the next frame, configure the start signal.
- If you want to reconfigure the register before the second start, the right sequence is:
  AXI/APB rst -> Reconfigure register -> START.
- In the actual application, the interval between two frames of pictures is relatively large, so a cycle delay of switching between frames will not have an impact.

4.4.2 Specific Usage

1. Configure the following registers:
   - Configure the PIC_WIDTH/HEIGHT register to the value of the size of the picture.
   - Configure the ENCODE_WIDTH/HEIGHT register to the value of the size of the encoding area.
   - Configure the WID_Y/UV register to the value of the Y /UV write id number.
   - Configure the SRAM_SIZE register to the value of the actual size of SRAM.
   - Configure the ENCODE_N register to the value of the number of encode lines.
   - Configure the STRIDE_Y/UV register to the value of the size of Y/UV stride.
   - Configure the ENCODE_X/Y register to the value of the point of the start encoding.
   - Configure the INT_MASK register.
2. Configure the CLEAR register.
3. Configure the START register to start the module. Then you can successfully start the module.

If there is an overflow, you need to do:

4. Configure the INT_CLEAN register to clean the interrupt.
5. Configure the CLEAR register.
6. You need to reset AXI/APB, then repeat Steps1~3.

NOTE

STRIDE_Y and STRIDE_UV should be 16*n.