TH1520 Video CODEC
User Manual

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Revisions

Rev	Description	Author(s)	Date
V1.0.0	Initial version	T-Head	2023-08-26

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List of Abbreviations

Abbreviations	Full Spelling	Chinese Explanation
MMU	Memory Management Unit	内存管理单元
NAL	Network Abstract Layer	网络抽象层
PPS	Picture Parameter Set	图像参数集
SEI	Supplemental Enhancement Information	补充增强信息
SPS	Sequence Parameter Set	序列参数集
VPS	Video Parameter Set	视频参数集

1 VENC

1.1 Overview

VENC module uses a hardware single-core encoding scheme to achieve hardware encoding with a maximum throughput of 3840*2160@40fps for H.265 and H.264 under the premise of minimal host CPU interaction load.
VENC module also integrates JPEG encoding function, JPEG and H.26x can be encoded at the same time.

1.1.1 Block Diagram

The block diagram of the VENC module is as follows:

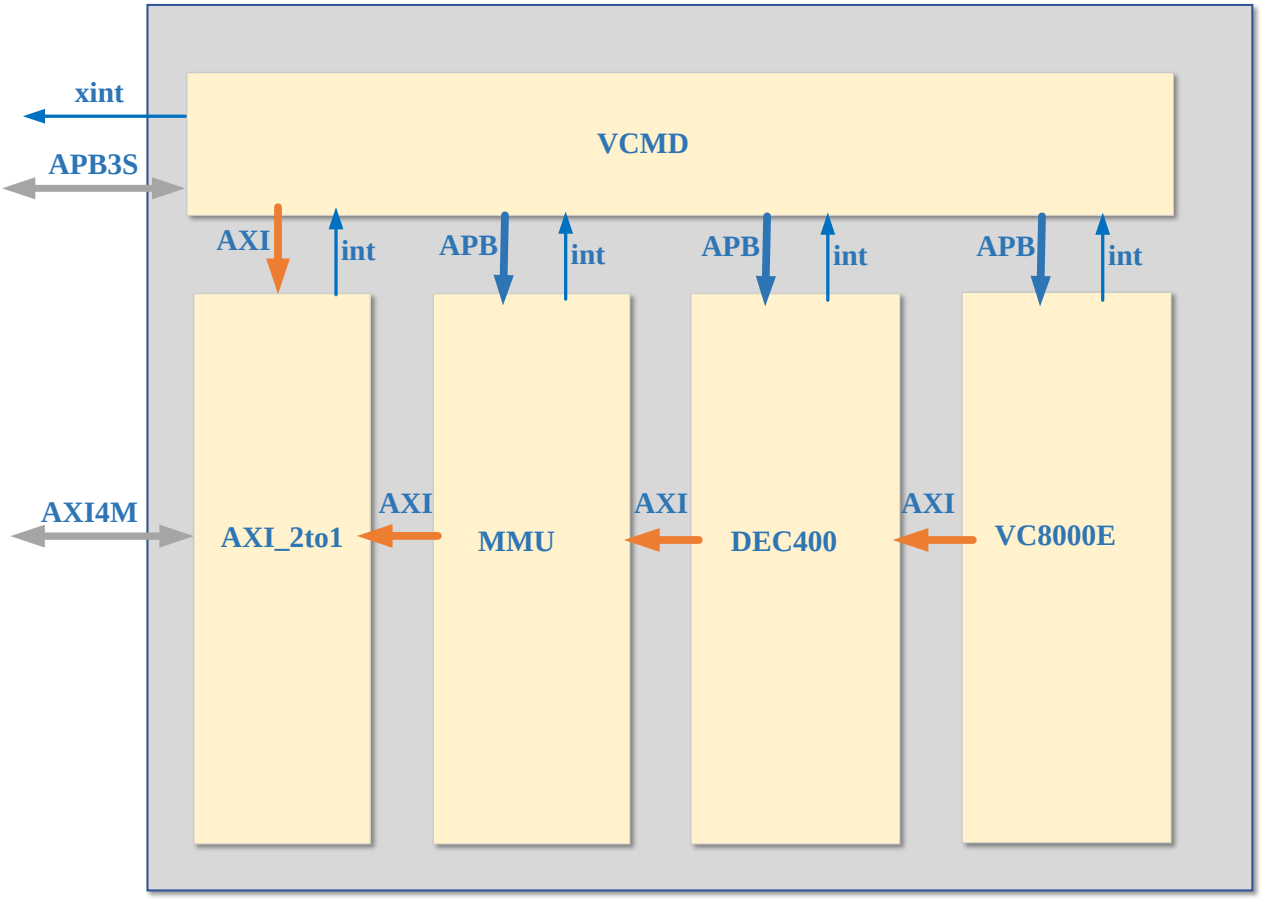

Figure & Table 1-1 VENC block diagram

1.2 Main Features

Main features of VENC:

- VENC module integrates the MMU sub-module to realize the memory management function.

- The VENC module integrates the engine VCMD sub-module for acceleration with register configuration. VCMD also completes the management of the interrupts of each sub-module inside the VENC module, and outputs an interrupt signal to the outside of the module.
- The integrated DEC400 sub-module of VENC module realizes the decompression function of input lossless compressed video data. When matched with the upstream module of VENC, the integrated DEC400 decompression function can achieve the purpose of saving bandwidth.
- The VC8000E sub-module integrated inside VENC is the main encoding hardware accelerator of VENC module. The overall function is: Under the premise of minimal host CPU interaction load, through the hardware single-core encoding scheme, the maximum hardware of 3840*2160@40fps is realized for H.26x coding.
- VC8000E sub-module also integrates JPEG encoding function, JPEG and H.26x can be encoded at the same time, supports simultaneous encoding of multiple video formats such as 4K, 1080P, VGA, etc.
- The VC8000E sub-module supports the maximum TU32*32 interframe conversion unit, supports CTB/MB level rate control, supports multi-region OSD overlay, region>=2.

1.3 Function Description

1.3.1 MMU Sub-module Function

VENC module integrates the MMU sub-module to realize the memory management function.

1.3.2 DEC400 Sub-module Function

The integrated DEC400 sub-module of VENC module realizes the decompression function of input lossless compressed video data. When matched with the upstream module of VENC, the integrated DEC400 decompression function can achieve the purpose of saving bandwidth.

1.3.3 VCMD Sub-module Function

The VENC module integrates the engine VCMD sub-module for acceleration with register configuration. VCMD also completes the management of the interrupts of each sub-module inside the VENC module, and outputs an interrupt signal to the outside of the module.

1.3.4 VC8000E Sub-module Function

The VC8000E sub-module integrated inside VENC is the main encoding hardware accelerator of VENC module. The overall function is: Under the premise of minimal host CPU interaction load, through the hardware single-core encoding scheme, the maximum hardware of 3840*2160@40fps is realized for H.26x coding.

VC8000E sub-module also integrates JPEG encoding function, JPEG and H.26x can be encoded at the same time, supports simultaneous encoding of multiple video formats such as 4K, 1080P, VGA, etc.

The VC8000E sub-module supports the maximum TU32*32 interframe conversion unit, supports CTB/MB level rate control, supports multi-region OSD overlay, region>=2.

1.4 Usage

The numbers presented in Figure & Table 1-2 represent the following transactions:

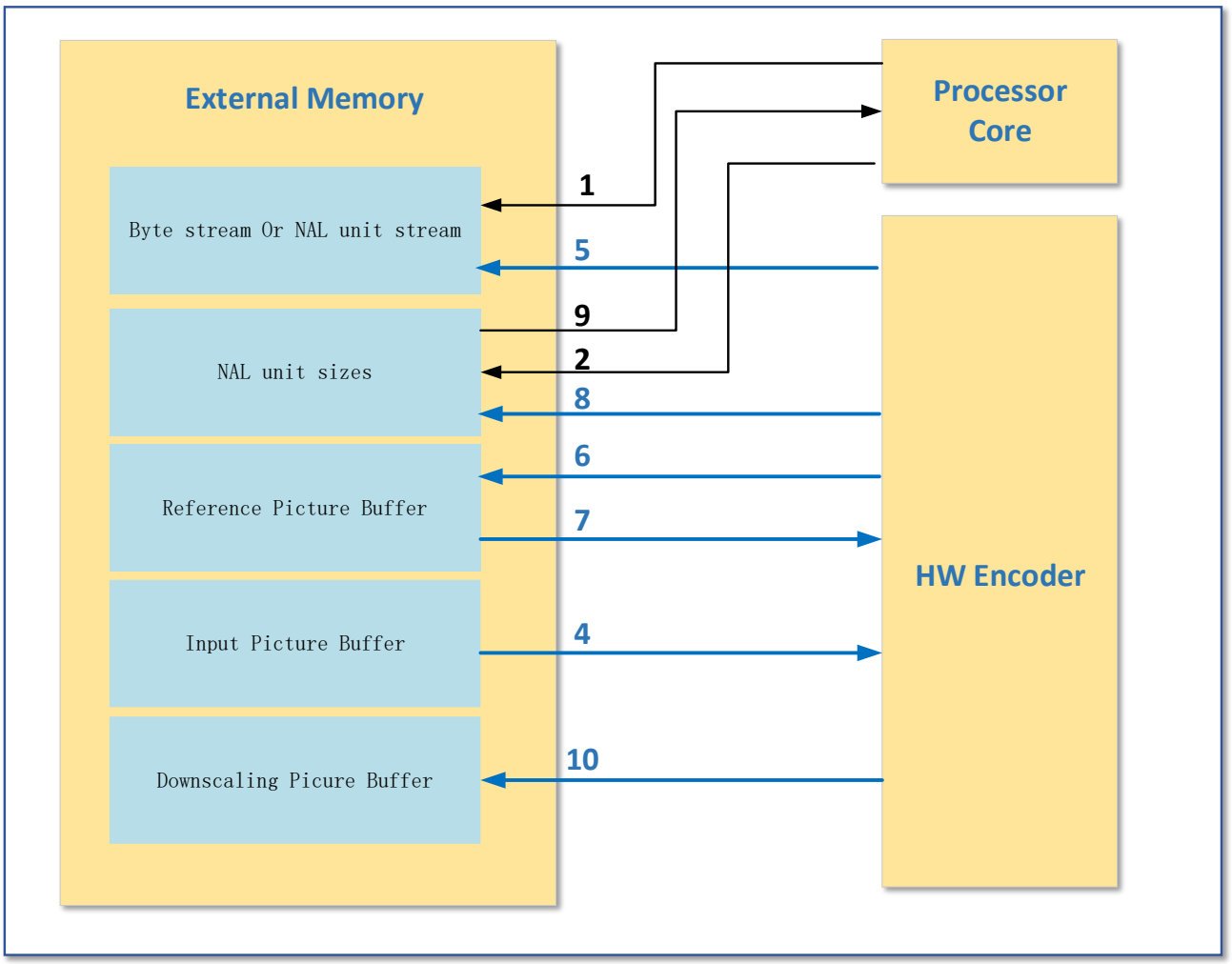

Figure & Table 1-2 H.265 data flow

1. Write Video Parameter Set (VPS), Sequence Parameter Set (SPS), Picture Parameter Set (PPS), and Supplemental Enhancement Information (SEI) (by SW).
2. Write VPS, SPS, PPS Network Abstraction Layer (NAL) unit size (by SW).
3. Initialize encoder HW via memory-mapped registers (by SW).
4. Read the input picture to be encoded.
5. Write encoded bit stream.
6. Write reference picture for next picture encoding.
7. Read reference picture for current picture encoding.
8. Write NAL unit size information.
9. Read NAL unit size information (by SW).
10. Write down scaled picture (optional).

2 VDEC

2.1 Overview

VDEC module is a single-core solution providing 4K decoding for HEVC, H.264, VP9, AVS and other formats. It is one of the smallest multi-format video decoder module solutions and offers low power consumption and negligible load on the host CPU.

2.1.1 Block Diagram

The block diagram of VDEC is as follow：

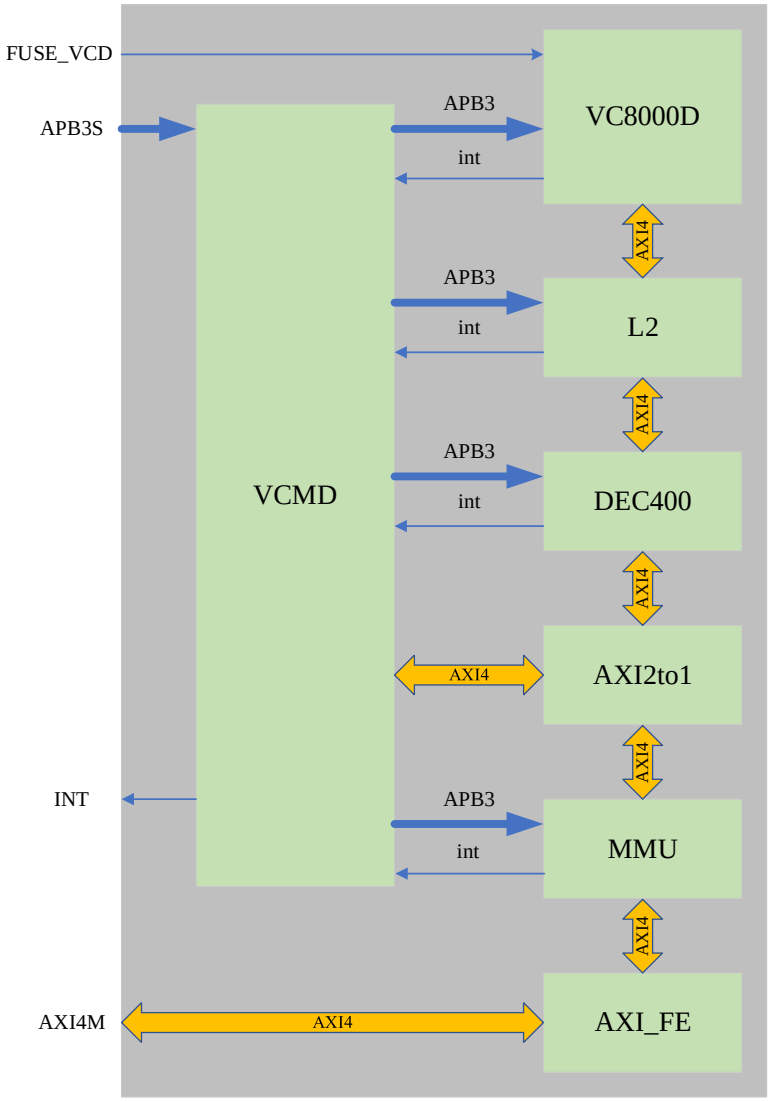

Figure & Table 2-1 VDEC block function diagram

2.2 Main Features

2.2.1 HEVC (H.265) Decoding Features

- Input stream format support
  - Byte stream
  - NAL unit stream
- Output picture format support
  - YCbCr420 semi-planar
  - DEC400 compatible compressed formats
- Up to main10 profile
- Level 5.1

2.2.2 VP9 Decoding Features

- Input stream format support
  - VP9 raw bit stream
  - IVF
- Output picture format support
  - YcbCr420 semi-planar
  - DEC400 compatible compressed formats
- Up to profile 2 (10-bit)

2.2.3 AVC (H.264) /MVC/SVC Decoding Features

- Input stream format support
  - AVC (H.264) stream
  - Byte stream
  - NAL unit stream
  - MVC stream
  - SVC stream
- Output picture format support
  - YCbCr4:2:0 semi-planar
  - Frames stored for progressive sequence
  - Fields stored for interlaced sequence
  - YCbCr4:0:0 monochrome
  - DEC400 compatible compressed formats
- Up to high profile
- H.264 HP level 5

2.2.4 MPEG-4/H.263 Decoding Features

- Input stream format support

  - MPEG-4 elementary video stream
  - H.263 elementary video stream
- Output picture format support
  - YCbCr4:2:0 semi-planar
  - Frame store for progressive sequence
  - Fields store for interlaced sequence
  - DEC400 compatible compressed formats
- MPEG-4 ASP level 5

2.2.5 VC-1 Decoding Features

- Input stream format support
  - VC-1 stream
- Output picture format support
  - YCbCr4:2:0 semi-planar
  - Frame store for progressive sequence
  - Fields store for interlaced sequence
  - DEC400 compatible compressed formats
- VC-1 AP Level 3(45 Mbits/s)

2.2.6 JPEG Decoding Features

- Input stream format support
  - JFIF file format 1.02
  - YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
- Output picture format support
  - YCbCr4:2:0 semi-planar raster scan
  - YCbCr4:0:0 semi-planar raster scan

2.2.7 VP8 Decoding Features

- Input stream format support
  - VP8 stream
- Output picture format support
  - YCbCr4:2:0 semi-planar
  - DEC400 compatible compressed format

2.2.8 VP7 Decoding Features

- Input stream format support
  - VP7 stream
- Output picture format support
  - YCbCr4:2:0 semi-planar
  - DEC400 compatible compressed formats

2.2.9 VP6 Decoding Features

- Input stream format support
  - VP6.0, 6.1, or 6.2 stream
- Output picture format support
  - YCbCr4:2:0 semi-planar
  - DEC400 compatible compressed formats

2.2.10 AVS/AVS+ Decoding Features

- Input stream format support
  - AVS or AVS+ stream
- Output picture format support
  - YCbCr4:2:0 semi-planar
  - DEC400 compatible compressed formats

2.2.11 AVS2

- Input stream format support
  - Byte stream
  - NAL unit stream
- Output picture format support
  - YCbCr4:2:0 semi-planar
  - DEC400 compatible compressed formats
- Main10 profile

2.2.12 Post Processing Output Frame Compression (DEC400)

- Crop
- Only down scaling

2.2.13 Maximum Picture Size

- HEVC/VP9/Progressive H.264/AVS2/VP8: 4096 x 4096
- JPEG: 32768 x 32768
- Other: 1920 x 1920

2.3 Function Description

2.3.1 MMU Sub-module Function

VDEC module integrates the Memory Management Unit (MMU) sub-module to realize the memory management function，the MMU implements virtual/physical address mapping to 40-bit address space as well as enforces memory access and security policies.

2.3.2 DEC400 Sub-module Function

The integrated DEC400 of VDEC module can provide a unified, lossless pixel compression and decompression infrastructure for the SoC. Working in conjunction with VC8000D, post-processor output can be compressed further to save bandwidth.

2.3.3 VCMD Sub-module Function

The VCMD integrated in VDEC module is a flexible command buffer execution engine. VCMD is designed to speed up VDEC swreg programming by fetching command buffer (stored in DDR) with AXI bus and reducing the number of interrupts with the command buffer queue. It also supports a group of command buffers which are linked together with the JMP command to reduce CPU loading.

2.3.4 L2Cache

The L2Cache integrated in VDEC module provides efficient additional bandwidth savings to VDEC, shapes the read and write AXI burst from VDEC with given alignment to maximize the DDR efficiency. L2Cache has two parts: a read-only cache and a write burst shaper. The read-only cache can cache read data in a specified address range to reduce DDR access. The write burst shaper can shape write AXI transactions in a specified address range to be aligned with a given alignment. The burst alignment is 128 Byte alignment.

2.3.5 VC8000D Sub-module Function

The VC8000D integrated in the VDEC module is the main decoding hardware accelerator. It supports decoding for HEVC, H.264, VP9, AVS2, VP8, VP7, VP6 and other formats.

2.3.6 AXI_FE

The AXI_FE integrated in the VDEC module provides the ability to allow an AXI port of a module (subsystem) to directly interface with the SoC system. AXI_FE capabilities include AXI burst split by a given alignment, generating unique AXI ID (support out-of-order/reorder) and generating AxUSER and AxPROT. For systems that need an AXI-unique ID, the AXI_FE block is recommended.