TH1520 System User Manual

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List of Abbreviations

Abbreviations	Full Spelling	Chinese Explanation
BMU	Bus Monitor Unit	总线监控单元
DMAC	Direct Memory Access Controller	直接内存访问控制器
DSP	Digital Signal Processor	数字信号处理器
ICU	Interrupt Control Unit	中断控制单元
ISR	Interrupt Service Routine	中断服务例程
POR	Power-On Reset	上电复位
QoS	Quality of Service	服务质量
REE	Rich Execution Environment	富执行环境
RTC	Real-Time Clock	实时时钟
SIMD	Single Instruction Multiple Data	单指令多数据
TAP	Test Access Port	测试接口
TEE	Trusted Execution Environment	可信执行环境
XIP	eXecute In Place	芯片内执行

1 Address Map

1.1 Address Map

An overview of address map is shown in Figure & Table 1-1.

- SYS_ TEE is TEE region, which can only be accessed by C910T.
- SYS_ REE is REE region.
- PLIC is REE region. PLIC is the local address space of C910 / C906 tightly coupled module. C910 PLIC can only be accessed by C910, and C906 PLIC can only be accessed by C906.
- Audio is in REE region.
- DDR is divided into multiple TEE and REE regions and configured according to specific applications.
- ROM is in TEE region, which can only be accessed by C910T.
- SRAM is in REE region and shared by Audio, NPU and CPU.

Generally, the configuration principle of PMP (IOPMP or PMP inside CPU) is that TEE region address space can only be accessed by C910T processor, and REE region address space can be accessed by all Masters. If access to a certain REE region needs to be restricted, for example, it can only be accessed by C910T, this function can be realized by modifying IOPMP configuration using software. For details, refer to the System Security chapter.

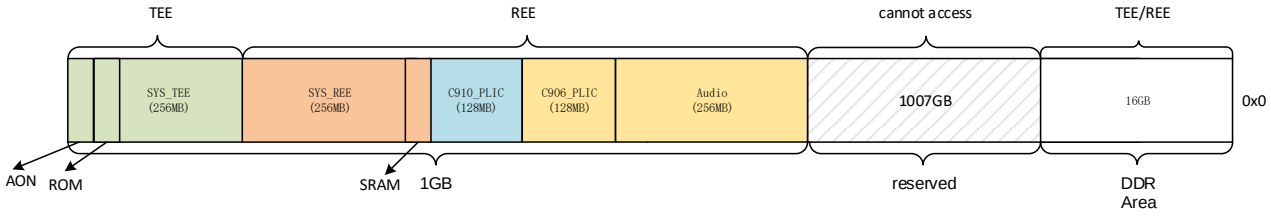


Figure & Table 1-1 Overview of memory map

The C910/C906 addresses are 40bit and the address assignment is shown in Figure & Table 1-2. The E902 addresses are 32bit, some addresses need to be remapped, and its address assignment is shown in Figure & Table 1-3.

NOTE

The address space assigned to DDR/SRAM/BROM is larger than the actual capacity. Please refer to the Features chapter for specific capacity.

Figure & Table 1-2 C910/C906 memory map

Start Address	End Address	Addressing Space	Description	Cache
0x00_0000_0000	0x03_FFFF_FFFF	16GB	DDR	Y
0xFF_D000_0000	0xFF_D7FF_FFFF	128MB	C906_PLIC	
0xFF_D800_0000	0xFF_DFFF_FFFF	128MB	C910_PLIC	

Start Address	End Address	Addressing Space	Description	Cache
0xFF_E000_0000	0xFF_E017_FFFF	1.5MB	SRAM	
0xFF_E018_0000	0xFF_E01B_FFFF	0.25MB	DSP00_TCM	
0xFF_E01C_0000	0xFF_E01F_FFFF	0.25MB	DSP01_TCM	
0xFF_E704_0000	0xFF_E704_FFFF	64KB	USB0	
0xFF_E706_0000	0xFF_E706_FFFF	64KB	GMAC1	
0xFF_E707_0000	0xFF_E707_FFFF	64KB	GMAC0	
0xFF_E708_0000	0xFF_E708_FFFF	64KB	EMMC	
0xFF_E709_0000	0xFF_E709_FFFF	64KB	SDIO0	
0xFF_E70A_0000	0xFF_E70A_FFFF	64KB	SDIO1	
0xFF_EA00_0000	0xFF_EBFF_FFFF	32MB	QSPI0	
0xFF_EC00_0000	0xFF_EC00_0FFF	4KB	GMAC_AXI_BUS_CFG	
0xFF_EC00_3000	0xFF_EC00_3FFF	4KB	GMAC0_APB	
0xFF_EC00_4000	0xFF_EC00_4FFF	4KB	GMAC1_APB	
0xFF_EC00_5000	0xFF_EC00_5FFF	4KB	GPIO0	
0xFF_EC00_6000	0xFF_EC00_6FFF	4KB	GPIO1	
0xFF_EC00_7000	0xFF_EC00_7FFF	4KB	PADCTRL0_APSYS	
0xFF_FC00_1000	0xFF_FC00_1FFF	4KB	IOPMP_GMAC0	
0xFF_FC00_2000	0xFF_FC00_2FFF	4KB	IOPMP_GMAC1	
0xFF_EC00_C000	0xFF_EC00_FFFF	16KB	I2C2	
0xFF_EC01_0000	0xFF_EC01_3FFF	16KB	UART2	
0xFF_EC01_4000	0xFF_EC01_7FFF	16KB	I2C3	
0xFF_EC01_C000	0xFF_EC01_FFFF	16KB	PWM	
0xFF_EC02_C000	0xFF_EC02_CFFF	4KB	MISC_SYSREG_R	
0xFF_EC03_0000	0xFF_EC03_FFFF	64KB	USB0_APB	
0xFF_FC02_8000	0xFF_FC02_8FFF	4KB	IOPMP_EMMC	
0xFF_FC02_9000	0xFF_FC02_9FFF	4KB	IOPMP_SDIO0	
0xFF_FC02_A000	0xFF_FC02_AFFF	4KB	IOPMP_SDIO1	
0xFF_FC02_B000	0xFF_FC02_BFFF	4KB	MISC_AXI_BUS_CFG	
0xFF_FC02_C000	0xFF_FC02_CFFF	4KB	MISC_SYSREG_T	

Start Address	End Address	Addressing Space	Description	Cache
0xFF_FC02_E000	0xFF_FC02_EFFF	4KB	IOPMP_USB0	
0xFF_E700_C000	0xFF_E700_FFFF	16KB	SPI0	
0xFF_E701_4000	0xFF_E701_7FFF	16KB	UART0	
0xFF_E703_4000	0xFF_E703_7FFF	16KB	I2S	
0xFF_E7F0_0000	0xFF_E7F0_3FFF	16KB	UART1	
0xFF_E7F0_4000	0xFF_E7F0_7FFF	16KB	UART3	
0xFF_E7F2_0000	0xFF_E7F2_3FFF	16KB	I2C0	
0xFF_E7F2_4000	0xFF_E7F2_7FFF	16KB	I2C1	
0xFF_E7F2_8000	0xFF_E7F2_BFFF	16KB	I2C4	
0xFF_E7F3_4000	0xFF_E7F3_7FFF	16KB	GPIO2	
0xFF_E7F3_8000	0xFF_E7F3_BFFF	16KB	GPIO3	
0xFF_E7F3_C000	0xFF_E7F3_CFFF	4KB	PADCTRL1_APSYS	
0xFF_F7F0_8000	0xFF_F7F0_BFFF	16KB	UART4	
0xFF_F7F0_C000	0xFF_F7F0_FFFF	16KB	UART5	
0xFF_F7F2_C000	0xFF_F7F2_FFFF	16KB	I2C5	
0xFF_F7F3_0000	0xFF_F7F3_3FFF	16KB	ISO7816	
0xFF_F800_0000	0xFF_F9FF_FFFF	32MB	QSPI1	
0xFF_FC80_0000	0xFF_FCBF_FFFF	4MB	NPU	
0xFF_E410_0000	0xFF_E410_FFFF	64KB	ISP0	
0xFF_E411_0000	0xFF_E411_FFFF	64KB	ISP1	
0xFF_E412_0000	0xFF_E412_FFFF	64KB	ISP_RY	
0xFF_E413_0000	0xFF_E413_FFFF	64KB	DW200	
0xFF_E400_0000	0xFF_E400_FFFF	64KB	MIPI_CSI2	
0xFF_E401_0000	0xFF_E401_FFFF	64KB	MIPI_CSI2X2_0	
0xFF_E402_0000	0xFF_E402_FFFF	64KB	MIPI_CSI2X2_1	
0xFF_E403_0000	0xFF_E403_FFFF	64KB	VIPRE	
0xFF_E404_0000	0xFF_E404_0FFF	4KB	VI_SYSREG_R	
0xFF_E406_0000	0xFF_E406_7FFF	32KB	DEC400_ISP0	
0xFF_E406_8000	0xFF_E406_FFFF	32KB	DEC400_ISP1	

Start Address	End Address	Addressing Space	Description	Cache
0xFF_E407_0000	0xFF_E407_7FFF	32KB	DEC400_DW	
0xFF_E407_8000	0xFF_E407_FFFF	32KB	ISP_VENC_SHAKE	
0xFF_F404_0000	0xFF_F404_0FFF	4KB	VI_SYSREG_T	
0xFF_F408_0000	0xFF_F408_0FFF	4KB	IOPMP_ISP0	
0xFF_F408_1000	0xFF_F408_1FFF	4KB	IOPMP_ISP1	
0xFF_F408_2000	0xFF_F408_2FFF	4KB	IOPMP_DW200	
0xFF_F408_3000	0xFF_F408_3FFF	4KB	IOPMP_VIPRE	
0xFF_F408_8000	0xFF_F408_8FFF	4KB	VI_AXI_BUS_CFG	
0xFF_F408_9000	0xFF_F408_9FFF	4KB	VI_AXI_BUS_CFG1	
0xFF_F408_A000	0xFF_F408_AFFF	4KB	VI_AXI_BUS_CFG2	
0xFF_F408_B000	0xFF_F408_BFFF	4KB	VI_AXI_BUS_CFG3	
0xFF_ECC0_0000	0xFF_ECC0_FFFF	64KB	VDEC	
0xFF_ECC1_0000	0xFF_ECC1_FFFF	64KB	VENC	
0xFF_ECC3_0000	0xFF_ECC3_0FFF	4KB	VP_SYSREG_R	
0xFF_ECC8_0000	0xFF_ECCB_FFFF	256KB	G2D	
0xFF_FCC3_0000	0xFF_FCC3_0FFF	4KB	VP_SYSREG_T	
0xFF_FCC5_0000	0xFF_FCC5_FFFF	64KB	FCE	
0xFF_FCC6_0000	0xFF_FCC6_0FFF	4KB	IOPMP_VENC	
0xFF_FCC6_1000	0xFF_FCC6_1FFF	4KB	IOPMP_VDEC	
0xFF_FCC6_2000	0xFF_FCC6_2FFF	4KB	IOPMP_G2D	
0xFF_FCC6_3000	0xFF_FCC6_3FFF	4KB	IOPMP_FCE	
0xFF_FCC6_4000	0xFF_FCC6_4FFF	4KB	VP_AXI_BUS_CFG	
0xFF_ED00_0000	0xFF_EF00_FFFF	32.0625MB	DDR_APB	
0xFF_EF01_0000	0xFF_EF01_0FFF	4KB	CLKGEN_R	
0xFF_EF01_4000	0xFF_EF01_4FFF	4KB	RSTGEN_R	
0xFF_EF01_8000	0xFF_EF01_8FFF	4KB	SYSREG_R	
0xFF_FD00_0000	0xFF_FF00_FFFF	32.0625MB	DDR_APB_T	
0xFF_FF01_0000	0xFF_FF01_0FFF	4KB	CLKGEN_T	
0xFF_FF01_4000	0xFF_FF01_4FFF	4KB	RSTGEN_T	

Start Address	End Address	Addressing Space	Description	Cache
0xFF_FF01_8000	0xFF_FF01_8FFF	4KB	SYSREG_T	
0xFF_FF01_C000	0xFF_FF01_CFFF	4KB	IOPMP_NPU	
0xFF_FF02_4400	0xFF_FF02_45FF	0.5KB	VO_AXI_BUS_CFG	
0xFF_FF02_4600	0xFF_FF02_47FF	0.5KB	NPU_AXI_BUS_CFG	
0xFF_EF04_0000	0xFF_EF04_0FFF	4KB	DSP_SYSREG	
0xFF_EF04_8000	0xFF_EF04_FFFF	32KB	DSP0_APB	
0xFF_EF05_0000	0xFF_EF05_7FFF	32KB	DSP1_APB	
0xFF_FF04_0000	0xFF_FF04_0FFF	4KB	DSP_SYSREG_T	
0xFF_FF05_8000	0xFF_FF05_8FFF	4KB	IOPMP_DSP0	
0xFF_FF05_9000	0xFF_FF05_9FFF	4KB	IOPMP_DSP1	
0xFF_FF05_A000	0xFF_FF05_AFFF	4KB	DSPSYS_AXI_BUS_CFG	
0xFF_FF05_B000	0xFF_FF05_BFFF	4KB	DSPSYS_AXI_SLV_BUS_CFG	
0xFF_FD00_0000	0xFF_FDFF_FFFF	16MB	DDR_PHY0	
0xFF_FE00_0000	0xFF_FEFF_FFFF	16MB	DDR_PHY1	
0xFF_FF00_0000	0xFF_FF00_3FFF	16KB	DDR_CTRL	
0xFF_FF00_4000	0xFF_FF00_4FFF	4KB	DDR_SCRAMBLER	
0xFF_FF00_5000	0xFF_FF00_5FFF	4KB	DDR_SYSREG	
0xFF_FF00_8000	0xFF_FF00_87FF	2KB	DDR_BMU0	
0xFF_FF00_8800	0xFF_FF00_8FFF	2KB	DDR_BMU1	
0xFF_FF00_9000	0xFF_FF00_97FF	2KB	DDR_BMU2	
0xFF_FF00_9800	0xFF_FF00_9FFF	2KB	DDR_BMU3	
0xFF_FF00_A000	0xFF_FF00_A7FF	2KB	DDR_BMU4	
0xFF_FF00_C000	0xFF_FF00_CFFF	4KB	DDR_PARITY	
0xFF_EF40_0000	0xFF_EF4F_FFFF	1MB	GPU	
0xFF_EF50_0000	0xFF_EF50_FFFF	64KB	MIPI_DSI0	
0xFF_EF51_0000	0xFF_EF51_FFFF	64KB	MIPI_DSI1	
0xFF_EF52_8000	0xFF_EF52_8FFF	4KB	VO_SYSREG_R	
0xFF_EF54_0000	0xFF_EF57_FFFF	256KB	HDMI	
0xFF_FF52_0000	0xFF_FF52_0FFF	4KB	IOPMP0_DPU	

Start Address	End Address	Addressing Space	Description	Cache
0xFF_FF52_1000	0xFF_FF52_1FFF	4KB	IOPMP1_DPU	
0xFF_FF52_2000	0xFF_FF52_2FFF	4KB	IOPMP_GPU	
0xFF_FF52_4000	0xFF_FF52_4FFF	4KB	VO_AXI_BUS_CFG	
0xFF_FF52_8000	0xFF_FF52_8FFF	4KB	VO_SYSREG_T	
0xFF_FF30_0000	0xFF_FF30_FFFF	64KB	EIP150B	
0xFF_FF31_0000	0xFF_FF31_FFFF	64KB	EIP120I	
0xFF_FF32_0000	0xFF_FF32_FFFF	64KB	EIP120II	
0xFF_FF33_0000	0xFF_FF33_FFFF	64KB	EIP120III	
0xFF_FF34_0000	0xFF_FF34_FFFF	64KB	TEE_DMAC	
0xFF_FF35_0000	0xFF_FF35_FFFF	64KB	OCRAM	
0xFF_FF20_0000	0xFF_FF20_FFFF	64KB	TEE_SYSREG	
0xFF_FF21_0000	0xFF_FF21_FFFF	64KB	EFUSE_CTL	
0xFF_FF22_0000	0xFF_FF22_FFFF	64KB	IOPMP_EIP120I	
0xFF_FF23_0000	0xFF_FF23_FFFF	64KB	IOPMP_EIP120II	
0xFF_FF24_0000	0xFF_FF24_FFFF	64KB	IOPMP_EIP120III	
0xFF_FF25_0000	0xFF_FF25_FFFF	64KB	IOPMP_TEE_DMAC	
0xFF_FF26_0000	0xFF_FF26_FFFF	64KB	KeyRAM	
0xFF_FF27_0000	0xFF_FF27_0FFF	4KB	Digital_Sensor3	
0xFF_FF27_1000	0xFF_FF27_1FFF	4KB	Digital_Sensor4	
0xFF_FF27_2000	0xFF_FF27_2FFF	4KB	Digital_Sensor5	
0xFF_FF27_3000	0xFF_FF27_3FFF	4KB	Digital_Sensor6	
0xFF_FF27_4000	0xFF_FF27_4FFF	4KB	Digital_Sensor7	
0xFF_EFC0_0000	0xFF_EFC0_FFFF	64KB	DMAC	
0xFF_EFC1_0000	0xFF_EFC1_FFFF	64KB	SPIN_LOCK	
0xFF_FFD0_0000	0xFF_FFDF_FFFF	1024KB	BROM	Y
0xFF_EFC3_0000	0xFF_EFC3_0FFF	4KB	WDT0	
0xFF_EFC3_1000	0xFF_EFC3_1FFF	4KB	WDT1	
0xFF_EFC3_2000	0xFF_EFC3_2FFF	4KB	TIMER0	
0xFF_EFC3_4000	0xFF_EFC3_4FFF	4KB	BMU_C910	

Start Address	End Address	Addressing Space	Description	Cache
0xFF_EFC3_E000	0xFF_EFC3_FFFF	8KB	MBOX0_R	
0xFF_EFC4_6000	0xFF_EFC4_7FFF	8KB	MBOX1_R	
0xFF_EFC4_8000	0xFF_EFC4_BFFF	16KB	MBOX2_R_0	
0xFF_EFC4_E000	0xFF_EFC4_FFFF	8KB	MBOX2_R_1	
0xFF_EFC5_0000	0xFF_EFC5_3FFF	16KB	MBOX3_R_0	
0xFF_EFC5_6000	0xFF_EFC5_7FFF	8KB	MBOX3_R_1	
0xFF_FFC2_0000	0xFF_FFC2_0FFF	4KB	IOPMP_DMAC	
0xFF_FFC2_1000	0xFF_FFC2_1FFF	4KB	IOPMP_AO	
0xFF_FFC2_2000	0xFF_FFC2_2FFF	4KB	IOPMP_AUD	
0xFF_FFC3_3000	0xFF_FFC3_3FFF	4KB	TIMER1	
0xFF_FFC3_5000	0xFF_FFC3_5FFF	4KB	CPU_AXI_BUS_CFG0	
0xFF_FFC3_6000	0xFF_FFC3_6FFF	4KB	CPU_AXI_BUS_CFG1	
0xFF_FFC3_7000	0xFF_FFC3_7FFF	4KB	IOPMP_CHIP_DBG	
0xFF_FFC3_8000	0xFF_FFC3_DFFF	24KB	MBOX0_T	
0xFF_FFC4_0000	0xFF_FFC4_5FFF	24KB	MBOX1_T	
0xFF_FFC4_C000	0xFF_FFC4_DFFF	8KB	MBOX2_T	
0xFF_FFC5_4000	0xFF_FFC5_5FFF	8KB	MBOX3_T	
0xFF_FFC5_7000	0xFF_FFC5_703F	64B	Digital_Sensor_C910_0	
0xFF_FFC5_7040	0xFF_FFC5_707F	64B	Digital_Sensor_C910_1	
0xFF_FFC5_7080	0xFF_FFC5_70BF	64B	Digital_Sensor_C910_2	
0xFF_FFC5_70C0	0xFF_FFC5_70FF	64B	Digital_Sensor_C910_3	
0xFF_FFEF_8000	0xFF_FFEF_FFFF	32KB	AO_SRAM	
0xFF_FFF0_0000	0xFF_FFF0_7FFF	32KB	STR_MEM	
0xFF_FFF4_0000	0xFF_FFF4_0FFF	4KB	RTC	
0xFF_FFF4_1000	0xFF_FFF4_1FFF	4KB	AO_GPIO	
0xFF_FFF4_2000	0xFF_FFF4_3FFF	8KB	AO_PMU	
0xFF_FFF4_4000	0xFF_FFF4_5FFF	8KB	AO_RSTGEN	
0xFF_FFF4_6000	0xFF_FFF4_7FFF	8KB	AO_CLKGEN	
0xFF_FFF4_8000	0xFF_FFF4_9FFF	8KB	AO_SYSREG	

Start Address	End Address	Addressing Space	Description	Cache
0xFF_FFF4_A000	0xFF_FFF4_BFFF	8KB	PADCTRL_AOSYS	
0xFF_FFF4_C000	0xFF_FFF4_CFFF	4KB	AO_IIC	
0xFF_FFF4_D000	0xFF_FFF4_DFFF	4KB	AO_TIMER	
0xFF_FFF4_E000	0xFF_FFF4_FFFF	8KB	PVT_CTRL	
0xFF_FFF5_0000	0xFF_FFF5_0FFF	4KB	AO_WDT	
0xFF_FFF5_1000	0xFF_FFF5_1FFF	4KB	AO_ADC	
0xFF_FFF5_2000	0xFF_FFF5_2FFF	4KB	AO_GPIO4	
0xFF_FFF5_3000	0xFF_FFF5_3FFF	4KB	AO_UART	
0xFF_C000_0000	0xFF_C001_FFFF	128KB	AUDIO_SRAM0	
0xFF_C002_0000	0xFF_C003_FFFF	128KB	AUDIO_SRAM1	
0xFF_C800_0000	0xFF_C800_FFFF	64KB	AUDIO_DMA	
0xFF_CB00_0000	0xFF_CB00_FFFF	64KB	AUDIO_CPR	
0xFF_CB01_0000	0xFF_CB01_FFFF	64KB	AUDIO_APB0	
0xFF_CB02_0000	0xFF_CB02_FFFF	64KB	AUDIO_APB1	
0xFF_CB01_0000	0xFF_CB01_0FFF	4KB	AUDIO_WDT	
0xFF_CB01_1000	0xFF_CB01_1FFF	4KB	AUDIO_TIMER	
0xFF_CB01_2000	0xFF_CB01_2FFF	4KB	AUDIO_TDM	
0xFF_CB01_3000	0xFF_CB01_3FFF	4KB	AUDIO_GPIO	
0xFF_CB01_4000	0xFF_CB01_4FFF	4KB	AUDIO_I2S0	
0xFF_CB01_5000	0xFF_CB01_5FFF	4KB	AUDIO_I2S1	
0xFF_CB01_6000	0xFF_CB01_6FFF	4KB	AUDIO_I2S2	
0xFF_CB01_7000	0xFF_CB01_7FFF	4KB	AUDIO_I2S_8CH	
0xFF_CB01_8000	0xFF_CB01_8FFF	4KB	AUDIO_SPDIF0	
0xFF_CB01_9000	0xFF_CB01_9FFF	4KB	AUDIO_SPDIF1	
0xFF_CB01_A000	0xFF_CB01_AFFF	4KB	AUDIO_I2C0	
0xFF_CB01_B000	0xFF_CB01_BFFF	4KB	AUDIO_I2C1	
0xFF_CB01_C000	0xFF_CB01_CFFF	4KB	AUDIO_UART	
0xFF_CB01_D000	0xFF_CB01_DFFF	4KB	AUDIO_IOCtrl	
0xFF_CB01_E000	0xFF_CB01_EFFF	4KB	AUDIO_VAD	

Start Address	End Address	Addressing Space	Description	Cache
0xFF_CB02_0000	0xFF_CB02_0FFF	4KB	AUDIO_BSM	
0xFF_CB02_E000	0xFF_CB02_EFFF	4KB	AUDIO_IOPMP0	
0xFF_CB02_F000	0xFF_CB02_FFFF	4KB	AUDIO_IOPMP1	

The E902 address bus is 32bit, so its address map is different from that of C910 and C906. The address map of E902 is shown in Figure & Table 1-3.

Figure & Table 1-3 E902 memory map

Start Address	End Address	Addressing Space	Description
0x0000_0000	0xAFFF_FFFF	16GB	DDR
0xE000_0000	0xE000_FFFF	64KB	E902_CLINT
0xE080_0000	0xE080_4FFF	20KB	E902_CLIC
0xB000_0000	0xB017_FFFF	1.5MB	SRAM
0xB018_0000	0xB01B_FFFF	0.25MB	DSP00_TCM
0xB01C_0000	0xB01F_FFFF	0.25MB	DSP01_TCM
0xB704_0000	0xB704_FFFF	64KB	USB0
0xB706_0000	0xB706_FFFF	64KB	GMAC1
0xB707_0000	0xB707_FFFF	64KB	GMAC0
0xB708_0000	0xB708_FFFF	64KB	EMMC
0xB709_0000	0xB709_FFFF	64KB	SDIO0
0xB70A_0000	0xB70A_FFFF	64KB	SDIO1
0xBA00_0000	0xBBFF_FFFF	32MB	QSPI0
0xBC00_0000	0xBC00_0FFF	4KB	GMAC_AXI_BUS_CFG
0xBC00_3000	0xBC00_3FFF	4KB	GMAC0_APB
0xBC00_4000	0xBC00_4FFF	4KB	GMAC1_APB
0xBC00_5000	0xBC00_5FFF	4KB	GPIO0
0xBC00_6000	0xBC00_6FFF	4KB	GPIO1
0xBC00_7000	0xBC00_7FFF	4KB	PADCTRL0_APSYS
0xFC00_1000	0xFC00_1FFF	4KB	IOPMP_GMAC0
0xFC00_2000	0xFC00_2FFF	4KB	IOPMP_GMAC1
0xBC00_C000	0xBC00_FFFF	16KB	I2C2

Start Address	End Address	Addressing Space	Description
0xBC01_0000	0xBC01_3FFF	16KB	UART2
0xBC01_4000	0xBC01_7FFF	16KB	I2C3
0xBC01_C000	0xBC01_FFFF	16KB	PWM
0xBC02_C000	0xBC02_CFFF	4KB	MISC_SYSREG_R
0xBC03_0000	0xBC03_FFFF	64KB	USB0_APB
0xFC02_8000	0xFC02_8FFF	4KB	IOPMP_EMMC
0xFC02_9000	0xFC02_9FFF	4KB	IOPMP_SDIO0
0xFC02_A000	0xFC02_AFFF	4KB	IOPMP_SDIO1
0xFC02_B000	0xFC02_BFFF	4KB	MISC_AXI_BUS_CFG
0xFC02_C000	0xFC02_CFFF	4KB	MISC_SYSREG_T
0xFC02_E000	0xFC02_EFFF	4KB	IOPMP_USB0
0xB700_C000	0xB700_FFFF	16KB	SPI0
0xB701_4000	0xB701_7FFF	16KB	UART0
0xB703_4000	0xB703_7FFF	16KB	I2S
0xB7F0_0000	0xB7F0_3FFF	16KB	UART1
0xB7F0_4000	0xB7F0_7FFF	16KB	UART3
0xB7F2_0000	0xB7F2_3FFF	16KB	I2C0
0xB7F2_4000	0xB7F2_7FFF	16KB	I2C1
0xB7F2_8000	0xB7F2_BFFF	16KB	I2C4
0xB7F3_4000	0xB7F3_7FFF	16KB	GPIO2
0xB7F3_8000	0xB7F3_BFFF	16KB	GPIO3
0xB7F3_C000	0xB7F3_CFFF	4KB	PADCTRL1_APSYS
0xF7F0_8000	0xF7F0_BFFF	16KB	UART4
0xF7F0_C000	0xF7F0_FFFF	16KB	UART5
0xF7F2_C000	0xF7F2_FFFF	16KB	I2C5
0xF7F3_0000	0xF7F3_3FFF	16KB	ISO7816
0xF800_0000	0xF9FF_FFFF	32MB	QSPI1
0xFC80_0000	0xFCBF_FFFF	4MB	NPU
0xB410_0000	0xB410_FFFF	64KB	ISP0

Start Address	End Address	Addressing Space	Description
0xB411_0000	0xB411_FFFF	64KB	ISP1
0xB412_0000	0xB412_FFFF	64KB	ISP_RY
0xB413_0000	0xB413_FFFF	64KB	DW200
0xB400_0000	0xB400_FFFF	64KB	MIPI_CSI2
0xB401_0000	0xB401_FFFF	64KB	MIPI_CSI2X2_0
0xB402_0000	0xB402_FFFF	64KB	MIPI_CSI2X2_1
0xB403_0000	0xB403_FFFF	64KB	VIPRE
0xB404_0000	0xB404_0FFF	4KB	VI_SYSREG_R
0xB406_0000	0xB406_7FFF	32KB	DEC400_ISP0
0xB406_8000	0xB406_FFFF	32KB	DEC400_ISP1
0xB407_0000	0xB407_7FFF	32KB	DEC400_DW
0xB407_8000	0xB407_FFFF	32KB	ISP_VENC_SHAKE
0xF404_0000	0xF404_0FFF	4KB	VI_SYSREG_T
0xF408_0000	0xF408_0FFF	4KB	IOPMP_ISP0
0xF408_1000	0xF408_1FFF	4KB	IOPMP_ISP1
0xF408_2000	0xF408_2FFF	4KB	IOPMP_DW200
0xF408_3000	0xF408_3FFF	4KB	IOPMP_VIPRE
0xF408_8000	0xF408_8FFF	4KB	VI_AXI_BUS_CFG
0xF408_9000	0xF408_9FFF	4KB	VI_AXI_BUS_CFG1
0xF408_A000	0xF408_AFFF	4KB	VI_AXI_BUS_CFG2
0xF408_B000	0xF408_BFFF	4KB	VI_AXI_BUS_CFG3
0xBCC0_0000	0xBCC0_FFFF	64KB	VDEC
0xBCC1_0000	0xBCC1_FFFF	64KB	VENC
0xBCC3_0000	0xBCC3_0FFF	4KB	VP_SYSREG_R
0xBCC8_0000	0xBCCB_FFFF	256KB	G2D
0xFCC3_0000	0xFCC3_0FFF	4KB	VP_SYSREG_T
0xFCC5_0000	0xFCC5_FFFF	64KB	FCE
0xFCC6_0000	0xFCC6_0FFF	4KB	IOPMP_VENC
0xFCC6_1000	0xFCC6_1FFF	4KB	IOPMP_VDEC

Start Address	End Address	Addressing Space	Description
0xFCC6_2000	0xFCC6_2FFF	4KB	IOPMP_G2D
0xFCC6_3000	0xFCC6_3FFF	4KB	IOPMP_FCE
0xFCC6_4000	0xFCC6_4FFF	4KB	VP_AXI_BUS_CFG
0xBD00_0000	0xBF00_FFFF	32.0625MB	DDR_APB
0xBF01_0000	0xBF01_0FFF	4KB	CLKGEN_R
0xBF01_4000	0xBF01_4FFF	4KB	RSTGEN_R
0xBF01_8000	0xBF01_8FFF	4KB	SYSREG_R
0xFD00_0000	0xFF00_FFFF	32.0625MB	DDR_APB_T
0xFF01_0000	0xFF01_0FFF	4KB	CLKGEN_T
0xFF01_4000	0xFF01_4FFF	4KB	RSTGEN_T
0xFF01_8000	0xFF01_8FFF	4KB	SYSREG_T
0xFF01_C000	0xFF01_CFFF	4KB	IOPMP_NPU
0xFF02_4400	0xFF02_45FF	0.5KB	VO_AXI_BUS_CFG
0xFF02_4600	0xFF02_47FF	0.5KB	NPU_AXI_BUS_CFG
0xBF04_0000	0xBF04_0FFF	4KB	DSP_SYSREG
0xBF04_8000	0xBF04_FFFF	32KB	DSP0_APB
0xBF05_0000	0xBF05_7FFF	32KB	DSP1_APB
0xFF04_0000	0xFF04_0FFF	4KB	DSP_SYSREG_T
0xFF05_8000	0xFF05_8FFF	4KB	IOPMP_DSP0
0xFF05_9000	0xFF05_9FFF	4KB	IOPMP_DSP1
0xFF05_A000	0xFF05_AFFF	4KB	DSPSYS_AXI_BUS_CFG
0xFF05_B000	0xFF05_BFFF	4KB	DSPSYS_AXI_SLV_BUS_CFG
0xFD00_0000	0xFDFF_FFFF	16MB	DDR_PHY0
0xFE00_0000	0xFEFF_FFFF	16MB	DDR_PHY1
0xFF00_0000	0xFF00_3FFF	16KB	DDR_CTRL
0xFF00_4000	0xFF00_4FFF	4KB	DDR_SCRAMBLER
0xFF00_5000	0xFF00_5FFF	4KB	DDR_SYSREG
0xFF00_8000	0xFF00_87FF	2KB	DDR_BMU0
0xFF00_8800	0xFF00_8FFF	2KB	DDR_BMU1

Start Address	End Address	Addressing Space	Description
0xFF00_9000	0xFF00_97FF	2KB	DDR_BMU2
0xFF00_9800	0xFF00_9FFF	2KB	DDR_BMU3
0xFF00_A000	0xFF00_A7FF	2KB	DDR_BMU4
0xFF00_C000	0xFF00_CFFF	4KB	DDR_PARITY
0xBF40_0000	0xBF4F_FFFF	1MB	GPU
0xBF50_0000	0xBF50_FFFF	64KB	MIPI_DSI0
0xBF51_0000	0xBF51_FFFF	64KB	MIPI_DSI1
0xBF52_8000	0xBF52_8FFF	4KB	VO_SYSREG_R
0xBF54_0000	0xBF57_FFFF	256KB	HDMI
0xFF52_0000	0xFF52_0FFF	4KB	IOPMP0_DPU
0xFF52_1000	0xFF52_1FFF	4KB	IOPMP1_DPU
0xFF52_2000	0xFF52_2FFF	4KB	IOPMP_GPU
0xFF52_4000	0xFF52_4FFF	4KB	VO_AXI_BUS_CFG
0xFF52_8000	0xFF52_8FFF	4KB	VO_SYSREG_T
0xFF30_0000	0xFF30_FFFF	64KB	EIP150B
0xFF31_0000	0xFF31_FFFF	64KB	EIP120I
0xFF32_0000	0xFF32_FFFF	64KB	EIP120II
0xFF33_0000	0xFF33_FFFF	64KB	EIP120III
0xFF34_0000	0xFF34_FFFF	64KB	TEE_DMAC
0xFF35_0000	0xFF35_FFFF	64KB	OCRAM
0xFF20_0000	0xFF20_FFFF	64KB	TEE_SYSREG
0xFF21_0000	0xFF21_FFFF	64KB	EFUSE_CTL
0xFF22_0000	0xFF22_FFFF	64KB	IOPMP_EIP120I
0xFF23_0000	0xFF23_FFFF	64KB	IOPMP_EIP120II
0xFF24_0000	0xFF24_FFFF	64KB	IOPMP_EIP120III
0xFF25_0000	0xFF25_FFFF	64KB	IOPMP_TEE_DMAC
0xFF26_0000	0xFF26_FFFF	64KB	KeyRAM
0xFF27_0000	0xFF27_0FFF	4KB	Digital_Sensor3
0xFF27_1000	0xFF27_1FFF	4KB	Digital_Sensor4

Start Address	End Address	Addressing Space	Description
0xFF27_2000	0xFF27_2FFF	4KB	Digital_Sensor5
0xFF27_3000	0xFF27_3FFF	4KB	Digital_Sensor6
0xFF27_4000	0xFF27_4FFF	4KB	Digital_Sensor7
0xBFC0_0000	0xBFC0_FFFF	64KB	DMAC
0xBFC1_0000	0xBFC1_FFFF	64KB	SPIN_LOCK
0xFFD0_0000	0xFFDF_FFFF	1024KB	BROM
0xBFC3_0000	0xBFC3_0FFF	4KB	WDT0
0xBFC3_1000	0xBFC3_1FFF	4KB	WDT1
0xBFC3_2000	0xBFC3_2FFF	4KB	TIMER0
0xBFC3_4000	0xBFC3_4FFF	4KB	BMU_C910
0xBFC3_E000	0xBFC3_FFFF	8KB	MBOX0_R
0xBFC4_6000	0xBFC4_7FFF	8KB	MBOX1_R
0xBFC4_8000	0xBFC4_BFFF	16KB	MBOX2_R_0
0xBFC4_E000	0xBFC4_FFFF	8KB	MBOX2_R_1
0xBFC5_0000	0xBFC5_3FFF	16KB	MBOX3_R_0
0xBFC5_6000	0xBFC5_7FFF	8KB	MBOX3_R_1
0xFFC2_0000	0xFFC2_0FFF	4KB	IOPMP_DMAC
0xFFC2_1000	0xFFC2_1FFF	4KB	IOPMP_AO
0xFFC2_2000	0xFFC2_2FFF	4KB	IOPMP_AUD
0xFFC3_3000	0xFFC3_3FFF	4KB	TIMER1
0xFFC3_5000	0xFFC3_5FFF	4KB	CPU_AXI_BUS_CFG0
0xFFC3_6000	0xFFC3_6FFF	4KB	CPU_AXI_BUS_CFG1
0xFFC3_7000	0xFFC3_7FFF	4KB	IOPMP_CHIP_DBG
0xFFC3_8000	0xFFC3_DFFF	24KB	MBOX0_T
0xFFC4_0000	0xFFC4_5FFF	24KB	MBOX1_T
0xFFC4_C000	0xFFC4_DFFF	8KB	MBOX2_T
0xFFC5_4000	0xFFC5_5FFF	8KB	MBOX3_T
0xFFC5_7000	0xFFC5_703F	64B	Digital_Sensor_C910_0
0xFFC5_7040	0xFFC5_707F	64B	Digital_Sensor_C910_1

Start Address	End Address	Addressing Space	Description
0xFFC5_7080	0xFFC5_70BF	64B	Digital_Sensor_C910_2
0xFFC5_70C0	0xFFC5_70FF	64B	Digital_Sensor_C910_3
0xFFEF_8000	0xFFEF_FFFF	32KB	AO_SRAM
0xFFF0_0000	0xFFF0_7FFF	32KB	STR_MEM
0xFFF4_0000	0xFFF4_0FFF	4KB	RTC
0xFFF4_1000	0xFFF4_1FFF	4KB	AO_GPIO
0xFFF4_2000	0xFFF4_3FFF	8KB	AO_PMU
0xFFF4_4000	0xFFF4_5FFF	8KB	AO_RSTGEN
0xFFF4_6000	0xFFF4_7FFF	8KB	AO_CLKGEN
0xFFF4_8000	0xFFF4_9FFF	8KB	AO_SYSREG
0xFFF4_A000	0xFFF4_BFFF	8KB	PADCTRL_AOSYS
0xFFF4_C000	0xFFF4_CFFF	4KB	AO_IIC
0xFFF4_D000	0xFFF4_DFFF	4KB	AO_TIMER
0xFFF4_E000	0xFFF4_FFFF	8KB	PVT_CTRL
0xFFF5_0000	0xFFF5_0FFF	4KB	AO_WDT
0xFFF5_1000	0xFFF5_1FFF	4KB	AO_ADC
0xFFF5_2000	0xFFF5_2FFF	4KB	AO_GPIO4
0xFFF5_3000	0xFFF5_3FFF	4KB	AO_UART
0xC000_0000	0xC001_FFFF	128KB	AUDIO_SRAM0
0xC002_0000	0xC003_FFFF	128KB	AUDIO_SRAM1
0xC800_0000	0xC800_FFFF	64KB	AUDIO_DMA
0xCB00_0000	0xCB00_FFFF	64KB	AUDIO_CPR
0xCB01_0000	0xCB01_FFFF	64KB	AUDIO_APB0
0xCB02_0000	0xCB02_FFFF	64KB	AUDIO_APB1
0xCB01_0000	0xCB01_0FFF	4KB	AUDIO_WDT
0xCB01_1000	0xCB01_1FFF	4KB	AUDIO_TIMER
0xCB01_2000	0xCB01_2FFF	4KB	AUDIO_TDM
0xCB01_3000	0xCB01_3FFF	4KB	AUDIO_GPIO
0xCB01_4000	0xCB01_4FFF	4KB	AUDIO_I2S0

Start Address	End Address	Addressing Space	Description
0xCB01_5000	0xCB01_5FFF	4KB	AUDIO_I2S1
0xCB01_6000	0xCB01_6FFF	4KB	AUDIO_I2S2
0xCB01_7000	0xCB01_7FFF	4KB	AUDIO_I2S_8CH
0xCB01_8000	0xCB01_8FFF	4KB	AUDIO_SPDIF0
0xCB01_9000	0xCB01_9FFF	4KB	AUDIO_SPDIF1
0xCB01_A000	0xCB01_AFFF	4KB	AUDIO_I2C0
0xCB01_B000	0xCB01_BFFF	4KB	AUDIO_I2C1
0xCB01_C000	0xCB01_CFFF	4KB	AUDIO_UART
0xCB01_D000	0xCB01_DFFF	4KB	AUDIO_IOCtrl
0xCB01_E000	0xCB01_EFFF	4KB	AUDIO_VAD
0xCB02_0000	0xCB02_0FFF	4KB	AUDIO_BSM
0xCB02_E000	0xCB02_EFFF	4KB	AUDIO_IOPMP0
0xCB02_F000	0xCB02_FFFF	4KB	AUDIO_IOPMP1

1.2 E902 Address Remap

The E902 address bus is 32bit and cannot directly access the 40-bit address space, so address remap is required. The address map relationship is shown in Figure & Table 1-4. The 32-bit address space of E902 is 4GB. 0-3GB is mapped to the DDR area of the 40-bit address space by default, that is, 0-3GB. The E902 3-4GB address space is fixedly mapped to the IO area of the 40-bit address space, that is, 1023-1024GB.

To enable E902 to access the full 40-bit address space, 0-1GB address space of E902 can be remapped to any consecutive 1GB area in the 40-bit address space by configuring the system register E902_ADDR_remap. To avoid overlap, 0-1GB address space can only be mapped to 5-16GB DDR space, that is, e902_addr_remap[9:0] can only be set to 0x0 or 0x4~0xf.

Figure & Table 1-4 Map relationship between E902 address and system address

E902 addr[31:30]	System Bus addr[39:30]	Area
0x0	e902_addr_remap[9:0]	DDR
0x1	0x1	DDR
0x2	0x2	DDR
0x3	0x3FF	IO

NOTE

The default value of e902_addr_remap[9:0] is 0.

2 Interrupt

2.1 Interrupt Mechanism

Three CPU cores are integrated in the chip, and each CPU core has its own interrupt controller. C902/C906 CPU is integrated with RISC-V standard compliant core local interrupt controller: CLIC. C910 is integrated with a platform-level interrupt controller compatible with the RIISC-V standard: PLIC. All interrupts are level triggered and active high.

2.2 Interrupt Map

Interrupt mapping of each CPU is shown below.

NOTE

0-15 interrupts of E902/C906/C910 are reserved for internal use, so the actual interrupt number is the interrupt number plus 16 in the following tables.

2.2.1 E902 Interrupt Map Table

Figure & Table 2-1 E902 interrupt map

No.	Interrupt Source	Description
0	audio_pd_intr	AudioSYS Power Down Interrupt
1	vdec_pd_intr	Video Decoder Power Down Interrupt
2	npu_pd_intr	NPU Power Down Interrupt
3	venc_pd_intr	Video Encoder Power Down Interrupt
4	gpu_pd_intr	GPU Power Down Interrupt
5	dsp0_pd_intr	DSP0 Power Down Interrupt
6	dsp1_pd_intr	DSP1 Power Down Interrupt
7	c910_core0_pd_intr	C910 Core0 Power Down Interrupt
8	c910_core1_pd_intr	C910 Core1 Power Down Interrupt
9	c910_core2_pd_intr	C910 Core2 Power Down Interrupt
10	c910_core3_pd_intr	C910 Core3 Power Down Interrupt
11	Reserved	Reserved
12	int_aogpio	AONSYS GPIO Interrupt
13	int_rtc	AONSYS RTC Interrupt

No.	Interrupt Source	Description
14	int_aonsys_cpr	AONSYS PMU Interrupt
15	int_pvtc	PVT Controller Interrupt
16	int_aoi2c	AONSYS I2C Interrupt
17	int_aotimer[0]	AONSYS Timer Interrupt 0
18	int_aotimer[1]	AONSYS Timer Interrupt 1
19	int_aotimer[2]	AONSYS Timer Interrupt 2
20	int_aotimer[3]	AONSYS Timer Interrupt 3
21	int_audio_pmu	AudioSYS ->AONSYS PMU Request Interrupt
22	int_mbox1	Mailbox1 Interrupt
23	int_uart1	UART1 Interrupt
24	int_aowdt	AONSYS Watchdog Interrupt
25	int_ao_sram1_err	AONSYS SRAM1 Check Error Interrupt
26	int_ao_sram2_err	AONSYS SRAM2 Check Error Interrupt
27	int_adc	ADC Interrupt
28	int_aouart	AONSYS UART Interrupt
29	int_hdmi_wakeup	HDMI Wakeup Interrupt
[31:30]	Reserved	Reserved

2.2.2 C906 Interrupt Map Table

Figure & Table 2-2 C906 interrupt map

No.	Interrupt Source	Description
0	Reserved	Reserved
1	int_audio_subsys_wdt	AudioSYS Watchdog Interrupt
2	int_mbox2	Mailbox2 Interrupt
3	int_audio_subsys_dmac	AudioSYS DMA Interrupt
4	int_audio_subsys_timer[0]	AudioSYS Timer Interrupt 0
5	int_audio_subsys_timer[1]	AudioSYS Timer Interrupt 1
6	int_audio_subsys_timer[2]	AudioSYS Timer Interrupt 2
7	int_audio_subsys_timer[3]	AudioSYS Timer Interrupt 3

No.	Interrupt Source	Description
8	int_audio_subsys_vad_fifo	AudioSYS VAD FIFO Interrupt
9	int_audio_subsys_vad_wakeup	AudioSYS VAD Wakeup Interrupt
10	int_audio_subsys_i2s0	AudioSYS I2S0 Interrupt
11	int_audio_subsys_i2s1	AudioSYS I2S1 Interrupt
12	int_audio_subsys_i2s2	AudioSYS I2S2 Interrupt
13	int_audio_subsys_i2s8ch	AudioSYS 8 Channel I2S Interrupt
14	int_audio_subsys_tdm	AudioSYS TDM Interrupt
15	int_audio_subsys_spdif0	AudioSYS SPDIF0 Interrupt
16	int_audio_subsys_spdif1	AudioSYS SPDIF1 Interrupt
17	int_audio_subsys_gpio	AudioSYS GPIO Interrupt
18	int_audio_subsys_i2c0	AudioSYS I2C0 Interrupt
19	int_audio_subsys_i2c1	AudioSYS I2C1 Interrupt
20	int_audio_subsys_uart	AudioSYS UART Interrupt
21	int_audio_subsys_bmu	AudioSYS BMU Interrupt
22	Reserved	Reserved
23	int_img_nna[0]	NPU Interrupt 0
24	int_img_nna[1]	NPU Interrupt 1
25	int_img_nna[2]	NPU Interrupt 2
26	pmu_cp_req_intr	AONSYS PMU Request Interrupt

2.2.3 C910 Interrupt Map Table

Figure & Table 2-3 C910 interrupt map

No.	Interrupt Source	Description
0	int_timer0[0]	Timer0 Interrupt 0
1	int_timer0[1]	Timer0 Interrupt 1
2	int_timer0[2]	Timer0 Interrupt 2
3	int_timer0[3]	Timer0 Interrupt 3
4	int_timer1[0]	Timer1 Interrupt 0
5	int_timer1[1]	Timer1 Interrupt 1

No.	Interrupt Source	Description
6	int_timer1[2]	Timer1 Interrupt 2
7	int_timer1[3]	Timer1 Interrupt 3
8	int_wdt0	Watchdog0 Interrupt
9	int_wdt1	Watchdog1 Interrupt
10	int_bmu_c910	C910 BMU Interrupt
11	int_dmac_cpusys	REE DMA Interrupt
12	int_mbox0	Mailbox0 Interrupt (C910 TEE)
13	int_mbox1	Mailbox1 Interrupt (E902)
14	int_mbox2	Mailbox2 Interrupt (C906)
15	int_mbox3	Mailbox3 Interrupt (C910 REE)
16	Reserved	Reserved
17	Reserved	Reserved
18	Reserved	Reserved
19	Reserved	Reserved
20	int_uart0	UART0 Interrupt
21	int_uart1	UART1 Interrupt
22	int_uart2	UART2 Interrupt
23	int_uart3	UART3 Interrupt
24	int_uart4	UART4 Interrupt
25	int_uart5	UART5 Interrupt
26	Reserved	Reserved
27	Reserved	Reserved
28	int_i2c0	I2C0 Interrupt
29	int_i2c1	I2C1 Interrupt
30	int_i2c2	I2C2 Interrupt
31	int_i2c3	I2C3 Interrupt
32	int_i2c4	I2C4 Interrupt
33	int_i2c5	I2C5 Interrupt
34	Reserved	Reserved

No.	Interrupt Source	Description
35	Reserved	Reserved
36	int_qspi0	QSPI0 Interrupt
37	int_qspi1	QSPI1 Interrupt
38	int_spi	SPI Interrupt
39	int_gpio4	GPIO4 Interrupt
40	int_gpio0	GPIO0 Interrupt
41	int_gpio1	GPIO1 Interrupt
42	int_gpio2	GPIO2 Interrupt
43	int_gpio3	GPIO3 Interrupt
44	int_pwm	PWM Interrupt
45	int_adc	ADC Interrupt
46	int_emmc_normal	eMMC Interrupt
47	int_emmc_wakeup	eMMC Wakeup Interrupt
48	int_sdio0_normal	SDIO0 Interrupt
49	int_sdio0_wakeup	SDIO0 Wakeup Interrupt
50	int_gmac0	GMAC0 Interrupt
51	int_gmac1	GMAC1 Interrupt
52	int_usb3_drd	USB Interrupt
53	int_dsmart	Smart Card Interrupt
54	int_i2s	I2S Interrupt
55	int_sdio1_normal	SDIO1 Interrupt
56	int_sdio1_wakeup	SDIO1 Wakeup Interrupt
57	Reserved	Reserved
58	int_rtc	RTC Interrupt
59	int_pvtc	PVT Controller Interrupt
60	int_aogpio	AONSYS GPIO Interrupt
61	int_aowdt	AONSYS Watchdog Interrupt
62	int_aouart	AONSYS UATR Interrupt
63	int_aoi2c	AONSYS I2C Interrupt

No.	Interrupt Source	Description
64	int_efuse	eFuse Interrupt
65	Reserved	Reserved
66	int_aotimer[0]	AONSYS Timer Interrupt 0
67	int_aotimer[1]	AONSYS Timer Interrupt 1
68	int_aotimer[2]	AONSYS Timer Interrupt 2
69	int_aotimer[3]	AONSYS Timer Interrupt 3
70	int_mpjtag	MPJTAG Interrupt
71	int_ddr_subsys_bmu	DDR BMU Interrupt
72	int_ddr_subsys_axiscr	AXI Scramble Interrupt
73	int_ddr_subsys_ddrphy[0]	DDR PHY Interrupt 0
74	int_ddr_subsys_ddrphy[1]	DDR PHY Interrupt 1
75	int_security_err	Security Summary Interrupt. Refer to the Security Interrupt table for details.
76	int_iopmp	IOPMP Summary Interrupt. Refer to the IOPMP Interrupt table for details.
77	int_dpu	DPU (Display Processing Unit) Interrupt
78	int_dpu_mmu	DPU MMU Interrupt
79	int_dpu_se	DPU Security Interrupt
80	int_dsp0	DSP0 Interrupt
81	int_dsp1	DSP1 Interrupt
82	int_dw200_dwe	DW200 DWE Module Interrupt
83	int_dw200_vse	DW200 VSE Module Interrupt
84	int_fce	FCE Interrupt
85	int_g2d	G2D Interrupt
86	int_gpu	GPU Interrupt
87	int_gpu_os_irq[0]	GPU OS0 Interrupt
88	int_gpu_os_irq[1]	GPU OS1 Interrupt
89	int_gpu_os_irq[2]	GPU OS2 Interrupt
90	int_gpu_os_irq[3]	GPU OS3 Interrupt

No.	Interrupt Source	Description
91	int_gpu_os_irq[4]	GPU OS4 Interrupt
92	int_gpu_os_irq[5]	GPU OS5 Interrupt
93	int_gpu_os_irq[6]	GPU OS6 Interrupt
94	int_gpu_os_irq[7]	GPU OS7 Interrupt
95	int_hdmi	HDMI Interrupt
96	int_hdmi_wakeup	HDMI Wakeup Interrupt
97	int_img_nna[0]	NPU Interrupt 0
98	int_img_nna[1]	NPU Interrupt 1
99	int_img_nna[2]	NPU Interrupt 3
100	int_isp_fe0_irq	ISP0 Fast Register Configuration Interrupt
101	int_isp_isp0_irq	ISP0 Interrupt
102	int_isp_mi0_irq	ISP0 Memory Interface Interrupt
103	int_isp_fe1_irq	ISP1 Fast Register Configuration Interrupt
104	int_isp_isp1_irq	ISP1 Interrupt
105	int_isp_mi1_irq	ISP1 Memory Interface Interrupt
106	int_isp_ry_fe_int	Post ISP Fast Register Configuration Interrupt
107	int_isp_ry_isp_int	Post ISP Interrupt
108	int_isp_ry_mi_int	Post ISP Memory Interface Interrupt
109	int_dw200_fe	DW200 Fast Register Configuration Interrupt
110	int_mipi_csi2x2_int0	MIPI CSI2X2_B Interrupt
111	int_mipi_csi2x2_int1	MIPI CSI2X2_A Interrupt
112	int_mipi_csi2	MIPI CSI2 Interrupt
113	int_mipi_dsi0	MIPI DSI0 Interrupt
114	int_mipi_dsi1	MIPI DSI1 Interrupt
115	int_vdec	Video Decoder Interrupt
116	Reserved	Reserved
117	int_venc	Video Encoder Interrupt
118	int_vipre	VIPRE Interrupt
119	int_eip120si_dma_done	EIP120SI DMA Completion Interrupt

No.	Interrupt Source	Description
120	int_eip120si_out	EIP120SI Interrupt
121	int_eip120si_result_av	EIP120SI Result Interrupt
122	int_eip120sii_dma_done	EIP120SII DMA Completion Interrupt
123	int_eip120sii_out	EIP120SII Interrupt
124	int_eip120sii_result_av	EIP120SII Result Interrupt
125	int_eip120siii_dma_done	EIP120SIII DMA Completion Interrupt
126	int_eip120siii_out	EIP120SIII Interrupt
127	int_eip120siii_result_av	EIP120SIII Result Interrupt
128	int_eip150b_int_eip150b_aic	EIP150B AIC Interrupt
129	int_eip150b_int_eip150b_pka[0]	EIP150B PKA Interrupt 0
130	int_eip150b_int_eip150b_pka[1]	EIP150B PKA Interrupt 1
131	int_eip150b_int_eip150b_pka[2]	EIP150B PKA Interrupt 2
132	int_eip150b_int_eip150b_slverr	EIP150B Slave Error Interrupt
133	int_eip150b_int_eip150b_trng	EIP150B TRNG Interrupt
134	int_tee_dmac	TEE DMA Interrupt
135	int_dec400_dw	DEC400 Interrupt Shared by DW200 and POST ISP
136	int_dec400_isp0	ISP0 DEC400 Interrupt
137	int_dec400_isp1	ISP1 DEC400 Interrupt
138	int_mipi_dsi0_halt	MIPI DSI0 Halt Interrupt
139	int_mipi_dsi1_halt	MIPI DSI1 Halt Interrupt
140	int_dsp0_cpu	Soft Interrupt of DSP0 and C910
141	int_dsp1_cpu	Soft Interrupt of DSP1 and C910
142	int_isp_venc_shake	ISP and VENC Handshake Interrupt
143	int_kram	KeyRAM Interrupt
147:144	Reserved	Reserved
148	Reserved	Reserved
149	int_audio_subsys_wdt	AudioSYS Watchdog Interrupt
150	Reserved	Reserved

No.	Interrupt Source	Description
151	int_audio_subsys_dmac	AudioSYS DMA Interrupt
152	int_audio_subsys_timer[0]	AudioSYS Timer Interrupt 0
153	int_audio_subsys_timer[1]	AudioSYS Timer Interrupt 1
154	int_audio_subsys_timer[2]	AudioSYS Timer Interrupt 2
155	int_audio_subsys_timer[3]	AudioSYS Timer Interrupt 3
156	int_audio_subsys_vad_fifo	AudioSYS VAD FIFO Interrupt
157	int_audio_subsys_vad_wakeup	AudioSYS VAD Wakeup Interrupt
158	int_audio_subsys_i2s0	AudioSYS I2S0 Interrupt
159	int_audio_subsys_i2s1	AudioSYS I2S1 Interrupt
160	int_audio_subsys_i2s2	AudioSYS I2S2 Interrupt
161	int_audio_subsys_i2s8ch	AudioSYS 8 Channel I2S Interrupt
162	int_audio_subsys_tdm	AudioSYS TDM Interrupt
163	int_audio_subsys_spdif0	AudioSYS SPDIF0 Interrupt
164	int_audio_subsys_spdif1	AudioSYS SPDIF1 Interrupt
165	int_audio_subsys_gpio	AudioSYS GPIO Interrupt
166	int_audio_subsys_i2c0	AudioSYS I2C0 Interrupt
167	int_audio_subsys_i2c1	AudioSYS I2C1 Interrupt
168	int_audio_subsys_uart	AudioSYS UART Interrupt
169	int_audio_subsys_bmu	AudioSYS BMU Interrupt
170	audio_pd_intr	AudioSYS Power Down Interrupt
171	c910_core0_pd_intr	C910 Core0 Power Down Interrupt
172	c910_core1_pd_intr	C910 Core1 Power Down Interrupt
173	c910_core2_pd_intr	C910 Core2 Power Down Interrupt
174	c910_core3_pd_intr	C910 Core3 Power Down Interrupt
175	dsp0_pd_intr	DSP0 Power Down Interrupt
176	dsp1_pd_intr	DSP1 Power Down Interrupt
177	gpu_pd_intr	GPU Power Down Interrupt
178	Reserved	Reserved

No.	Interrupt Source	Description
179	Reserved	Reserved
180	npu_pd_intr	NPU Power Down Interrupt
181	vdec_pd_intr	Video Decoder Power Down Interrupt
182	venc_pd_intr	Video Encoder Power Down Interrupt
[191:183]	Reserved	Reserved
192	int_c910_tee_sw[0]	C910 TEE Soft Interrupt 0
193	int_c910_tee_sw[1]	C910 TEE Soft Interrupt 1
194	int_c910_tee_sw[2]	C910 TEE Soft Interrupt 2
195	int_c910_tee_sw[3]	C910 TEE Soft Interrupt 3
196	int_c910_tee_sw[4]	C910 TEE Soft Interrupt 4
197	int_c910_tee_sw[5]	C910 TEE Soft Interrupt 5
198	int_c910_tee_sw[6]	C910 TEE Soft Interrupt 6
199	int_c910_tee_sw[7]	C910 TEE Soft Interrupt 7
200	int_c910_ree_sw[0]	C910 REE Soft Interrupt 0
201	int_c910_ree_sw[1]	C910 REE Soft Interrupt 1
202	int_c910_ree_sw[2]	C910 REE Soft Interrupt 2
203	int_c910_ree_sw[3]	C910 REE Soft Interrupt 3
204	int_c910_ree_sw[4]	C910 REE Soft Interrupt 4
205	int_c910_ree_sw[5]	C910 REE Soft Interrupt 5
206	int_c910_ree_sw[6]	C910 REE Soft Interrupt 6
207	int_c910_ree_sw[7]	C910 REE Soft Interrupt 7

2.2.4 DSP0 Interrupt Map Table

Figure & Table 2-4 DSP0 interrupt map

No.	Interrupt Source	Description
0	int_vipre	VIPRE Interrupt
1	int_mipi_csi2x2_int1	MIPI CSI2X2 Interrupt 0
2	int_mipi_csi2x2_int0	MIPI CSI2X2 Interrupt 1
3	int_mipi_csi2	MIPI CSI2 Interrupt

No.	Interrupt Source	Description
4	int_isp_ry_mi_int	ISP0 Memory Interface Interrupt
5	int_isp_ry_isp_int	ISP0 Interrupt
6	int_isp_ry_fe_int	ISP0 Fast Register Configuration Interrupt
7	int_isp_mi1_irq	ISP1 Memory Interface Interrupt
8	int_isp_mi0_irq	ISP0 Memory Interface Interrupt
9	int_isp_isp1_irq	ISP1 Interrupt
10	int_isp_isp0_irq	ISP0 Interrupt
11	int_isp_fe1_irq	ISP1 Fast Register Configuration Interrupt
12	int_isp_fe0_irq	ISP0 Fast Register Configuration Interrupt
13	int_iopmp_vi4	VIPRE IOPMP Interrupt
14	int_iopmp_vi3	POST ISP and DW200 IOPMP Interrupt
15	int_iopmp_vi2	ISP1 IOPMP Interrupt
16	int_iopmp_vi1	ISP0 IOPMP Interrupt
17	int_dw200_vse	DW200 VSE Module Interrupt
18	int_dw200_fe	DW200 Fast Register Configuration Interrupt
19	int_dw200_dwe	DW200 DWE Module Interrupt
20	int_dec400_isp0	ISP0 DEC400 Interrupt
21	int_dec400_isp1	ISP1 DEC400 Interrupt
22	int_dec400_dw	DW200 DEC400 Interrupt
23	Reserved	Reserved
24	int_dsp1_dsp0	DSP1->DSP0 Soft Interrupt
25	int_gpio0	GPIO0 Interrupt
26	int_gpio1	GPIO1 Interrupt
27	int_gpio2	GPIO2 Interrupt
28	int_gpio3	GPIO3 Interrupt
29	int_gpio4	GPIO4 Interrupt
30	int_aogpio	AONSYS GPIO Interrupt
31	int_iopmp_dsp0	DSP0 IOPMP Interrupt

2.2.5 DSP1 Interrupt Map Table

Figure & Table 2-5 DSP1 interrupt map

No.	Interrupt Source	Description
0	int_vipre	VIPRE Interrupt
1	int_mipi_csi2x2_int1	MIPI CSI2X2 Interrupt 0
2	int_mipi_csi2x2_int0	MIPI CSI2X2 Interrupt 1
3	int_mipi_csi2	MIPI CSI2 Interrupt
4	int_isp_ry_mi_int	ISP0 Memory Interface Interrupt
5	int_isp_ry_isp_int	ISP0 Interrupt
6	int_isp_ry_fe_int	ISP0 Fast Register Config Interrupt
7	int_isp_mi1_irq	ISP1 Memory Interface Interrupt
8	int_isp_mi0_irq	ISP0 Memory Interface Interrupt
9	int_isp_isp1_irq	ISP1 Interrupt
10	int_isp_isp0_irq	ISP0 Interrupt
11	int_isp_fe1_irq	ISP1 Fast Register Config Interrupt
12	int_isp_fe0_irq	ISP0 Fast Register Config Interrupt
13	int_iopmp_vi4	VIPRE IOPMP Interrupt
14	int_iopmp_vi3	POST ISP and DW200 IOPMP Interrupt
15	int_iopmp_vi2	ISP1 IOPMP Interrupt
16	int_iopmp_vi1	ISP0 IOPMP Interrupt
17	int_dw200_vse	DW200 VSE Module Interrupt
18	int_dw200_fe	DW200 Fast Register Config Interrupt
19	int_dw200_dwe	DW200 DWE Module Interrupt
20	int_dec400_isp0	ISP0 DEC400 Interrupt
21	int_dec400_isp1	ISP1 DEC400 Interrupt
22	int_dec400_dw	DW200 DEC400 Interrupt
23	Reserved	Reserved
24	int_dsp0_dsp1	DSP0->DSP1 Soft Interrupt
25	int_gpio0	GPIO0 Interrupt

No.	Interrupt Source	Description
26	int_gpio1	GPIO1 Interrupt
27	int_gpio2	GPIO2 Interrupt
28	int_gpio3	GPIO3 Interrupt
29	int_gpio4	GPIO4 Interrupt
30	int_aogpio	AONSYS GPIO Interrupt
31	int_iopmp_dsp1	DSP1 IOPMP Interrupt

3 Pinmux

3.1 Overview

All the PADs on the chip are divided into three groups. MUX and registers of each group are independent. The base Addresses of related registers in each PAD group are also different. This chapter mainly introduces configuration and MUX of digital PADs. Other PADs on the chip, such as analog PADs, PHY PADs and power PADs, are not covered in this chapter.

Except for some special PADs, most PADs correspond to two registers: PADCFG register and PADMUX register. The PADCFG register can mainly be used to configure the pull- up/pull-down state of the internal resistor of the PAD, the slew rate control of the PAD output signal, the Schmitt control of the PAD input signal, and the PAD driver strength. The PADMUX register is used to select the PAD working mode.

Due to the internal physical implementation on the chip, the internal pull-up/pull-down resistor value of the PAD is not accurate. Generally, the internal pull-up resistor value is about 48KΩ and the internal pull-down resistor value is about 44KΩ. In addition, you can enable the internal strong pull-up resistor of the PAD through the PADCFG register. When the internal pull-up function is enabled, enabling the internal strong pull-up resistor will give the PAD a pull-up of about 2.1kΩ on the chip. The pull-up/pull-down resistor value range is as follows:

Figure & Table 3-1 Pull-up/Pull-down resistor value

Parameter	Min.	Typ. (25℃)	Max.	Units	Description
RSPU	1.6k	2.1k	3k	Ω	Strong Pull-up Resistor
RPU	32k	48k	79k	Ω	Pull-up Resistor
RPD	30k	44k	65k	Ω	Pull-down Resistor

Driver strength of digital PADs can be configured through PADCFG registers to 16 levels. Driver strength of PAD high level is slightly different from that of PAD low level. The output current corresponding to driver strength at each level is as follows:

PAD low level output current:

Figure & Table 3-2 PAD low level output current

Configuration	Min.	Typ. (25℃)	Max.	Units
(DS3,DS2,DS1,DS0) = '0000'	0.8	1.1	1.5	mA
(DS3,DS2,DS1,DS0) = '0001'	1.1	1.6	2.2	mA
(DS3,DS2,DS1,DS0) = '0010'	2.3	3.3	4.3	mA
(DS3,DS2,DS1,DS0) = '0011'	3.4	4.9	6.5	mA

Configuration	Min.	Typ. (25℃)	Max.	Units
(DS3,DS2,DS1,DS0) = '0100'	4.5	6.6	8.6	mA
(DS3,DS2,DS1,DS0) = '0101'	5.7	8.2	10.8	mA
(DS3,DS2,DS1,DS0) = '0110'	6.8	9.9	13.0	mA
(DS3,DS2,DS1,DS0) = '0111'	7.9	11.5	15.1	mA
(DS3,DS2,DS1,DS0) = '1000'	9.0	13.1	17.2	mA
(DS3,DS2,DS1,DS0) = '1001'	10.2	14.8	19.4	mA
(DS3,DS2,DS1,DS0) = '1010'	11.3	16.4	21.6	mA
(DS3,DS2,DS1,DS0) = '1011'	12.4	18.1	32.7	mA
(DS3,DS2,DS1,DS0) = '1100'	13.5	19.6	25.8	mA
(DS3,DS2,DS1,DS0) = '1101'	14.7	21.3	28.0	mA
(DS3,DS2,DS1,DS0) = '1110'	15.8	22.9	30.1	mA
(DS3,DS2,DS1,DS0) = '1111'	16.9	24.6	32.3	mA

PAD high level output current:

Figure & Table 3-3 PAD high level output current

Configuration	Min.	Typ. (25℃)	Max.	Units
(DS3,DS2,DS1,DS0) = '0000'	0.7	1.1	1.6	mA
(DS3,DS2,DS1,DS0) = '0001'	1.1	1.7	2.3	mA
(DS3,DS2,DS1,DS0) = '0010'	2.1	3.3	4.7	mA
(DS3,DS2,DS1,DS0) = '0011'	3.2	5.0	7.0	mA
(DS3,DS2,DS1,DS0) = '0100'	4.2	6.6	9.3	mA
(DS3,DS2,DS1,DS0) = '0101'	5.3	8.3	11.7	mA
(DS3,DS2,DS1,DS0) = '0110'	6.3	9.9	13.9	mA
(DS3,DS2,DS1,DS0) = '0111'	7.4	11.6	16.2	mA
(DS3,DS2,DS1,DS0) = '1000'	8.4	13.2	18.5	mA
(DS3,DS2,DS1,DS0) = '1001'	9.4	14.8	20.8	mA
(DS3,DS2,DS1,DS0) = '1010'	10.5	16.5	23.1	mA
(DS3,DS2,DS1,DS0) = '1011'	11.5	18.1	25.4	mA
(DS3,DS2,DS1,DS0) = '1100'	12.6	19.7	27.6	mA

Configuration	Min.	Typ. (25℃)	Max.	Units
(DS3,DS2,DS1,DS0) = '1101'	13.6	21.4	29.9	mA
(DS3,DS2,DS1,DS0) = '1110'	14.6	23.0	32.1	mA
(DS3,DS2,DS1,DS0) = '1111'	15.7	24.6	34.4	mA

3.2 Function Description

3.2.1 PADMUX in Function Mode

MUX and default pull-up/pull-down of all digital PADs are shown in the following table:

Figure & Table 3-4 PAD MUX table

PAD Name	PU/PD	Default	Function Select 1	Function Select 2	Function Select 3	Function Select 4	Function Select 5
PAD Group 1							
OSC_CLK_IN	N.A.	OSC_CLK_IN					
OSC_CLK_OUT	N.A.	OSC_CLK_OUT					
SYS_RST_N	PU	SYS_RST_N					
RTC_CLK_IN	N.A.	RTC_CLK_IN					
RTC_CLK_OUT	N.A.	RTC_CLK_OUT					
TEST_MODE	PD	TEST_MODE					
DEBUG_MODE	PD	DEBUG_MODE			GPIO4_22		
POR_SEL	PU	POR_SEL					
I2C_AON_SCL	PU	I2C_AON_SCL			AOGPIO_0		
I2C_AON_SDA	PU	I2C_AON_SDA			AOGPIO_1		
CPU_JTG_TCLK	none	CPU_JTG_TCLK			AOGPIO_2		
CPU_JTG_TMS	PU	CPU_JTG_TMS			AOGPIO_3		
CPU_JTG_TDI	none	CPU_JTG_TDI			AOGPIO_4		
CPU_JTG_TDO	none	CPU_JTG_TDO			AOGPIO_5		
CPU_JTG_TRST	PU	CPU_JTG_TRST			AOGPIO_6		
AOGPIO_7	PD	PLL_DSKEW_BYPASS	AUDIO_PA18		AOGPIO_7		

PAD Name	PU/PD	Default	Function Select 1	Function Select 2	Function Select 3	Function Select 4	Function Select 5
AOGPIO_8	none	AOUART_TXD	AUDIO_PA19	AOUART_IR_OUT	AOGPIO_8		
AOGPIO_9	none	AOUART_RXD	AUDIO_PA20	AOUART_IR_IN	AOGPIO_9		
AOGPIO_10	PD	BISR_BYPASS	AUDIO_PA21		AOGPIO_10		
AOGPIO_11	none	AOGPIO_11	AUDIO_PA22				
AOGPIO_12	none	AOGPIO_12	AUDIO_PA23				
AOGPIO_13	none	AOGPIO_13	AUDIO_PA24				
AOGPIO_14	none	AOGPIO_14	AUDIO_PA25				
AOGPIO_15	none	AOGPIO_15	AUDIO_PA26				
AUDIO_PA0	none	AUDIO_PA0			GPIO4_0		
AUDIO_PA1	none	AUDIO_PA1			GPIO4_1		
AUDIO_PA2	none	AUDIO_PA2			GPIO4_2		
AUDIO_PA3	none	AUDIO_PA3			GPIO4_3		
AUDIO_PA4	none	AUDIO_PA4			GPIO4_4		
AUDIO_PA5	none	AUDIO_PA5			GPIO4_5		
AUDIO_PA6	none	AUDIO_PA6			GPIO4_6		
AUDIO_PA7	none	AUDIO_PA7			GPIO4_7		
AUDIO_PA8	none	AUDIO_PA8			GPIO4_8		
AUDIO_PA9	none	AUDIO_PA9			GPIO4_9		
AUDIO_PA10	none	AUDIO_PA10			GPIO4_10		
AUDIO_PA11	none	AUDIO_PA11			GPIO4_11		
AUDIO_PA12	none	AUDIO_PA12			GPIO4_12		
AUDIO_PA13	none	AUDIO_PA13			GPIO4_13		
AUDIO_PA14	none	AUDIO_PA14			GPIO4_14		
AUDIO_PA15	none	AUDIO_PA15			GPIO4_15		
AUDIO_PA16	none	AUDIO_PA16			GPIO4_16		

PAD Name	PU/PD	Default	Function Select 1	Function Select 2	Function Select 3	Function Select 4	Function Select 5
AUDIO_PA17	none	AUDIO_PA17			GPIO4_17		
AUDIO_PA27	none	AUDIO_PA27			GPIO4_18		
AUDIO_PA28	none	AUDIO_PA28			GPIO4_19		
AUDIO_PA29	none	AUDIO_PA29			GPIO4_20		
AUDIO_PA30	none	AUDIO_PA30	SE_RSTN		GPIO4_21		
PAD Group 2							
QSPI1_SCLK	none	QSPI1_SCLK	ISO7816_DET		GPIO0_0	EFUSE_SPI_CLK	
QSPI1_CSN0	none	QSPI1_SSN0		I2C5_SCL	GPIO0_1	EFUSE_SPI_NSS	
QSPI1_D0_MOSI	none	QSPI1_M0_MOSI	ISO7816_CVCC_EN	I2C5_SDA	GPIO0_2	EFUSE_SPI_SI	
QSPI1_D1_MISO	none	QSPI1_M1_MISO	ISO7816_CLK		GPIO0_3	EFUSE_SPI_SO	
QSPI1_D2_WP	none	QSPI1_M2_WP	ISO7816_RST	UART5_TXD	GPIO0_4	EFUSE_BUSY	
QSPI1_D3_HOLD	none	QSPI1_M3_HOLD	ISO7816_DAT	UART5_RXD	GPIO0_5		
I2C0_SCL	PU	I2C0_SCL			GPIO0_6		
I2C0_SDA	PU	I2C0_SDA			GPIO0_7		
I2C1_SCL	PU	I2C1_SCL			GPIO0_8		
I2C1_SDA	PU	I2C1_SDA			GPIO0_9		
UART1_TXD	none	UART1_TXD			GPIO0_10		
UART1_RXD	none	UART1_RXD			GPIO0_11		
UART4_TXD	none	UART4_TXD			GPIO0_12		
UART4_RXD	none	UART4_RXD			GPIO0_13		
UART4_CTSN	none	UART4_CTSN			GPIO0_14		
UART4_RTSN	none	UART4_RTSN			GPIO0_15		
UART3_TXD	none	CHIP_DBG_TXD	UART3_TXD		GPIO0_16		
UART3_RXD	none	CHIP_DBG_RXD	UART3_RXD		GPIO0_17		
GPIO0_18	none	GPIO0_18	I2C4_SCL				
GPIO0_19	none	GPIO0_19	I2C4_SDA				

PAD Name	PU/PD	Default	Function Select 1	Function Select 2	Function Select 3	Function Select 4	Function Select 5
GPIO0_20	none	GPIO0_20	UART3_TXD	UART3_IR_OUT			
GPIO0_21	none	GPIO0_21	UART3_RXD	UART3_IR_IN		DPU_COLOR_0	DPU1_COLOR_0
GPIO0_22	none	GPIO0_22	DSP0_JTG_TRST	I2C4_SCL		DPU_COLOR_1	DPU1_COLOR_1
GPIO0_23	none	GPIO0_23	DSP0_JTG_TMS	I2C4_SDA		DPU_COLOR_2	DPU1_COLOR_2
GPIO0_24	none	GPIO0_24	DSP0_JTG_TDI	QSPI1_SSN1		DPU_COLOR_3	DPU1_COLOR_3
GPIO0_25	none	GPIO0_25	DSP0_JTG_TDO			DPU_COLOR_4	DPU1_COLOR_4
GPIO0_26	none	GPIO0_26	DSP0_JTG_TCLK			DPU_COLOR_5	DPU1_COLOR_5
GPIO0_27	none	GPIO0_27		I2C1_SCL		DPU_COLOR_6	DPU1_COLOR_6
GPIO0_28	none	GPIO0_28		I2C1_SDA		DPU_COLOR_7	DPU1_COLOR_7
GPIO0_29	none	GPIO0_29				DPU_COLOR_8	DPU1_COLOR_8
GPIO0_30	none	GPIO0_30				DPU_COLOR_9	DPU1_COLOR_9
GPIO0_31	none	GPIO0_31				DPU_COLOR_10	DPU1_COLOR_10
GPIO1_0	none	GPIO1_0	DSP1_JTG_TRST			DPU_COLOR_11	DPU1_COLOR_11
GPIO1_1	none	GPIO1_1	DSP1_JTG_TMS			DPU_COLOR_12	DPU1_COLOR_12
GPIO1_2	none	GPIO1_2	DSP1_JTG_TDI			DPU_COLOR_13	DPU1_COLOR_13
GPIO1_3	none	GPIO1_3	DSP1_JTG_TDO			DPU_COLOR_14	DPU1_COLOR_14
GPIO1_4	none	GPIO1_4	DSP1_JTG_TCLK			DPU_COLOR_15	DPU1_COLOR_15
GPIO1_5	none	GPIO1_5				DPU_COLOR_16	DPU1_COLOR_16
GPIO1_6	none	GPIO1_6				DPU_COLOR_17	DPU1_COLO

PAD Name	PU/PD	Default	Function Select 1	Function Select 2	Function Select 3	Function Select 4	Function Select 5
							R_17
GPIO1_7	none	GPIO1_7	QSPI1_SCLK			DPU_COLOR_18	DPU1_COLOR_18
GPIO1_8	none	GPIO1_8	QSPI1_SSN0			DPU_COLOR_19	DPU1_COLOR_19
GPIO1_9	none	GPIO1_9	QSPI1_M0_MOSI			DPU_COLOR_20	DPU1_COLOR_20
GPIO1_10	none	GPIO1_10	QSPI1_M1_MISO			DPU_COLOR_21	DPU1_COLOR_21
GPIO1_11	none	GPIO1_11	QSPI1_M2_WP			DPU_COLOR_22	DPU1_COLOR_22
GPIO1_12	none	GPIO1_12	QSPI1_M3_HOLD			DPU_COLOR_23	DPU1_COLOR_23
GPIO1_13	none	GPIO1_13	UART4_TXD			DPU_COLOR_EN	DPU1_COLOR_EN
GPIO1_14	none	GPIO1_14	UART4_RXD			DPU_HSYNC	DPU1_HSYNC
GPIO1_15	none	GPIO1_15	UART4_CTSN			DPU_VSYNC	DPU1_VSYNC
GPIO1_16	none	GPIO1_16	UART4_RTSN			DPU_PIXELCLK	DPU1_PIXELCLK
CLK_OUT_0	none	BOOT_SEL0	CLK_OUT_0		GPIO1_17		
CLK_OUT_1	none	BOOT_SEL1	CLK_OUT_1		GPIO1_18		
CLK_OUT_2	none	BOOT_SEL2	CLK_OUT_2		GPIO1_19		
CLK_OUT_3	none	BOOT_SEL3	CLK_OUT_3		GPIO1_20		
GPIO1_21	none	GPIO1_21		ISP0_FL_TRIG	GPIO1_21		
GPIO1_22	none	GPIO1_22		ISP0_FLASH_TRIG	GPIO1_22		
GPIO1_23	none	GPIO1_23		ISP0_PRELIGHT_TRIG	GPIO1_23		
GPIO1_24	none	GPIO1_24		ISP0_SHUTTER_TRIG	GPIO1_24		
GPIO1_25	none	GPIO1_25		ISP0_SHUTTER_OPEN	GPIO1_25		
GPIO1_26	none	GPIO1_26		ISP1_FL_TRIG			
GPIO1_27	none	GPIO1_27		ISP1_FLASH_TRIG			

PAD Name	PU/PD	Default	Function Select 1	Function Select 2	Function Select 3	Function Select 4	Function Select 5
GPIO1_28	none	GPIO1_28		ISP1_PRELIGHT_TRIG			
GPIO1_29	none	GPIO1_29		ISP1_SHUTTER_TRIG			
GPIO1_30	none	GPIO1_30		ISP1_SHUTTER_OPEN			
PAD Group 3							
UART0_TXD	none	UART0_TXD			GPIO2_0		
UART0_RXD	none	UART0_RXD			GPIO2_1		
QSPI0_SCLK	none	QSPI0_SCLK	PWM0	I2S_SDA0	GPIO2_2		
QSPI0_CSN0	none	QSPI0_SSN0	PWM1	I2S_SDA1	GPIO2_3		
QSPI0_CSN1	none	QSPI0_SSN1	PWM2	I2S_SDA2	GPIO2_4		
QSPI0_D0_MOSI	none	QSPI0_M0_MOSI	PWM3	I2S_SDA3	GPIO2_5		
QSPI0_D1_MISO	none	QSPI0_M1_MISO	PWM4	I2S_MCLK	GPIO2_6		
QSPI0_D2_WP	none	QSPI0_M2_WP	PWM5	I2S_SCLK	GPIO2_7		
QSPI0_D3_HOLD	none	QSPI0_M3_HOLD		I2S_WS	GPIO2_8		
I2C2_SCL	none	I2C2_SCL	UART2_TXD		GPIO2_9		
I2C2_SDA	none	I2C2_SDA	UART2_RXD		GPIO2_10		
I2C3_SCL	none	I2C3_SCL			GPIO2_11		
I2C3_SDA	none	I2C3_SDA			GPIO2_12		
GPIO2_13	none	GPIO2_13	SPI_SSN1				
SPI_SCLK	none	SPI_SCLK	UART2_TXD	UART2_IR_OUT	GPIO2_14		
SPI_CSN	none	SPI_SSN0	UART2_RXD	UART2_IR_IN	GPIO2_15		
SPI_MOSI	none	SPI_MOSI			GPIO2_16		
SPI_MISO	none	SPI_MISO			GPIO2_17		
GPIO2_18	none	GPIO2_18	GMAC1_TX_CLK				
GPIO2_19	none	GPIO2_19	GMAC1_RX_CLK				
GPIO2_20	none	GPIO2_20	GMAC1_TXEN				
GPIO2_21	none	GPIO2_21	GMAC1_TXD0				

PAD Name	PU/PD	Default	Function Select 1	Function Select 2	Function Select 3	Function Select 4	Function Select 5
GPIO2_22	none	GPIO2_22	GMAC1_TXD1				
GPIO2_23	none	GPIO2_23	GMAC1_TXD2				
GPIO2_24	none	GPIO2_24	GMAC1_TXD3				
GPIO2_25	none	GPIO2_25	GMAC1_RXDV				
SDIO0_WPRTN	none	SDIO0_WPRTN			GPIO2_26		
SDIO0_DETN	none	SDIO0_DETN			GPIO2_27		
SDIO1_WPRTN	none	SDIO1_WPRTN			GPIO2_28		
SDIO1_DETN	none	SDIO1_DETN			GPIO2_29		
GPIO2_30	none	GPIO2_30	GMAC1_RXD0				
GPIO2_31	none	GPIO2_31	GMAC1_RXD1				
GPIO3_0	none	GPIO3_0	GMAC1_RXD2				
GPIO3_1	none	GPIO3_1	GMAC1_RXD3				
GPIO3_2	none	GPIO3_2	PWM0				
GPIO3_3	none	GPIO3_3	PWM1				
HDMI_SCL	PU	HDMI_SCL	PWM2		GPIO3_4		
HDMI_SDA	PU	HDMI_SDA	PWM3		GPIO3_5		
HDMI_CEC	PU	HDMI_CEC			GPIO3_6		
GMAC0_TX_CLK	none	GMAC0_TX_CLK			GPIO3_7		
GMAC0_RX_CLK	none	GMAC0_RX_CLK			GPIO3_8		
GMAC0_TXEN	none	GMAC0_TXEN	UART2_TXD		GPIO3_9		
GMAC0_TXD0	none	GMAC0_TXD0	UART2_RXD		GPIO3_10		
GMAC0_TXD1	none	GMAC0_TXD1	UART0_TXD		GPIO3_11		
GMAC0_TXD2	none	GMAC0_TXD2	UART0_RXD		GPIO3_12		
GMAC0_TXD3	none	GMAC0_TXD3	I2C2_SCL		GPIO3_13		
GMAC0_RXDV	none	GMAC0_RXDV	I2C2_SDA		GPIO3_14		
GMAC0_RXD0	none	GMAC0_RXD0	I2C3_SCL		GPIO3_15		

PAD Name	PU/PD	Default	Function Select 1	Function Select 2	Function Select 3	Function Select 4	Function Select 5
GMAC0_RXD1	none	GMAC0_RXD1	I2C3_SDA		GPIO3_16		
GMAC0_RXD2	none	GMAC0_RXD2	SPI_SCLK		GPIO3_17		
GMAC0_RXD3	none	GMAC0_RXD3	SPI_SSN0		GPIO3_18		
GMAC0_MDC	none	GMAC0_MDC	SPI_MOSI	GMAC1_MDC	GPIO3_19		
GMAC0_MDIO	none	GMAC0_MDIO	SPI_MISO	GMAC1_MDIO	GPIO3_20		
GMAC0_COL	none	GMAC0_COL	PWM4		GPIO3_21		
GMAC0_CRS	none	GMAC0_CRS	PWM5		GPIO3_22		

Each PAD corresponds to a 4-bit MUX register, which is used to select the PAD working mode. The 31 PADs AUDIO_PA0-AUDIO_PAD30 have another MUX relationship in AUDIO_SUBSYS, which is controlled by the MUX register in AUDIO_SUBSYS. The specific MUX relationship is as follows:

Figure & Table 3-5 PAD MUX table-AUDIO_SUBSYS

PAD Name	Default	Function Select 1	Function Select 2	Function Select 3	Function Select 4
AUDIO_PA18	AUDIO_PA18	I2S2_WSCLK	TDM_DAT	VAD_DIN2	UART_CTS
AUDIO_PA19	AUDIO_PA19	I2S2_BCLK	TDM_BCLK	VAD_DIN3	UART_RTS
AUDIO_PA20	AUDIO_PA20	I2S2_MCLK	TDM_WSCLK	I2C1_CLK	I2C1_DATA
AUDIO_PA21	AUDIO_PA21	I2S2_DIN	SPDIF0_DIN	I2C1_DATA	I2C1_CLK
AUDIO_PA22	AUDIO_PA22	I2S2_DOUT	SPDIF0_DOUT	CLK_12M	
AUDIO_PA23	AUDIO_PA23	UART_TX	SPDIF1_DOUT	SPDIF0_DOUT	
AUDIO_PA24	AUDIO_PA24	UART_RX	SPDIF1_DIN	SPDIF0_DIN	I2S_8CH_MCLK
AUDIO_PA25	AUDIO_PA25	I2S_8CH_SDA2	UART_RTS	SPDIF0_DIN	I2C1_DATA
AUDIO_PA26	AUDIO_PA26	I2S_8CH_SDA3	UART_CTS	SPDIF0_DOUT	I2C1_CLK
AUDIO_PA0	AUDIO_PA0	VAD_DIN0	VAD_PDM_DIN0	SPDIF0_DOUT	I2S_8CH_SDA2
AUDIO_PA1	AUDIO_PA1	VAD_DIN1	VAD_PDM_DIN1	SPDIF0_DIN	I2S_8CH_SDA3
AUDIO_PA2	AUDIO_PA2	VAD_WS		SPDIF1_DOUT	I2S_8CH_WSCLK
AUDIO_PA3	AUDIO_PA3	VAD_SCLK	VAD_PDM_CLK	SPDIF1_DIN	I2S_8CH_BCLK
AUDIO_PA4	AUDIO_PA4	VAD_DIN2	VAD_PDM_DIN2	UART_RX	I2S_8CH_SDA0
AUDIO_PA5	AUDIO_PA5	VAD_DIN3	VAD_PDM_DIN3	UART_TX	I2S_8CH_SDA1
AUDIO_PA6	AUDIO_PA6	I2C0_CLK	T_CPU_CLK	I2C1_CLK	UART_RX
AUDIO_PA7	AUDIO_PA7	I2C0_DATA	T_AXI_CLK	I2C1_DATA	UART_TX
AUDIO_PA8	AUDIO_PA8	CLK_12M	T_AHB_CLK	VAD_MCLK	I2S_8CH_MCLK
AUDIO_PA9	AUDIO_PA9	I2S0_WSCLK	T_APB_CLK	TDM_DAT	I2S1_WSCLK
AUDIO_PA10	AUDIO_PA10	I2S0_BCLK	T_UART_CLK	TDM_BCLK	I2S1_BCLK

PAD Name	Default	Function Select 1	Function Select 2	Function Select 3	Function Select 4
AUDIO_PA11	AUDIO_PA11	I2S0_SDA	T_AUDIO_CLK	TDM_WSCLK	I2S1_DIN
AUDIO_PA12	AUDIO_PA12	I2S0_MCLK	I2C1_CLK	UART_TX	I2S1_DOUT
AUDIO_PA13	AUDIO_PA13	I2S1_MCLK	I2C1_DATA	VAD_MCLK	UART_RX
AUDIO_PA14	AUDIO_PA14	I2S1_WSCLK	VAD_PDM_DIN0	VAD_DIN0	I2S0_WSCLK
AUDIO_PA15	AUDIO_PA15	I2S1_BCLK	VAD_PDM_DIN1	VAD_DIN1	CLK_12M
AUDIO_PA16	AUDIO_PA16	I2S1_DIN	VAD_PDM_CLK	VAD_WS	I2C1_CLK
AUDIO_PA17	AUDIO_PA17	I2S1_DOUT	VAD_PDM_DIN2	VAD_SCLK	I2C1_DATA
AUDIO_PA27	AUDIO_PA27	I2S_8CH_WSCLK	TDM_WSCLK	SPDIF1_DIN	I2S0_WSCLK
AUDIO_PA28	AUDIO_PA28	I2S_8CH_BCLK	TDM_BCLK	SPDIF1_DOUT	I2S0_BCLK
AUDIO_PA29	AUDIO_PA29	I2S_8CH_SDA0	TDM_DAT	I2C0_CLK	I2S0_SDA
AUDIO_PA30	AUDIO_PA30	I2S_8CH_SDA1		I2C0_DATA	I2S0_MCLK

3.2.2 PADMUX in Debug Mode

The debug mode is used to multiplex observation and control signals of some modules on the chip to the PADs. Pulling up the DEBUG_MODE PAD enables the chip PAD configurationuration to enter the debug mode. There is also MUX in debug mode. AUDIO_PA0 is used to control whether other PADs have debug mode function or Alt1 function. The MUX relationship in debug mode is as follows:

Figure & Table 3-6 PAD MUX table-debug mode

PAD Name	Default	Function Select 1	Description
AOGPIO_8	PMU_FSM_ST0	ADC_CLK	PMU FSM observation signal
AOGPIO_9	PMU_FSM_ST1	ADC_EOC	
AOGPIO_10	PMU_FSM_ST2	ADC_SOB	
AOGPIO_11	PMU_FSM_ST3	ADC_SOC	
AOGPIO_12	POR_RST_N		POR reset output observation signal
AOGPIO_7	BISR_L2_CDE		BISR observation signal
AOGPIO_13	BISR_L2_DONE		
AOGPIO_14	BISR_SRAM_CDE		
AOGPIO_15	BISR_SRAM_DONE		
AUDIO_PA0	DEBUG_ALT1_SEL		RC test control signal
AUDIO_PA1	RC_ATESTSEL0		
AUDIO_PA2	RC_ATESTSEL1		
AUDIO_PA3	RC_ATESTSEL2		

PAD Name	Default	Function Select 1	Description
AUDIO_PA4	RC_CLK		
AUDIO_PA6	RC_ATESTEN		
AUDIO_PA5	RC_READY		
AUDIO_PA8	RC_EN		
AUDIO_PA9	RC_MODE		
AUDIO_PA10	RC_FCAL_0		
AUDIO_PA11	RC_FCAL_1		
AUDIO_PA12	RC_FCAL_2		
AUDIO_PA13	RC_FCAL_3		
AUDIO_PA14	RC_FCAL_4		
AUDIO_PA15	RC_FCAL_5		
AUDIO_PA16	RC_FCAL_6		
AUDIO_PA17	RC_FCAL_7		
AUDIO_PA27	RC_FCAL_8		
AUDIO_PA28	RC_FCAL_9		
AUDIO_PA29	RC_FCAL_10		
AUDIO_PA30	RC_FCAL_11		
AUDIO_PA7	EFUSE_PRELOAD_DONE		eFuse programming interface
QSPI1_SCLK	EFUSE_SPI_CLK		
QSPI1_CSN0	EFUSE_SPI_NSS		
QSPI1_D0_MOSI	EFUSE_SPI_SI		
QSPI1_D1_MISO	EFUSE_SPI_SO		
QSPI1_D2_WP	EFUSE_BUSY		
I2C0_SCL	USB3_DRD_JTG_TCLK		USB3 PHY JTAG interface
I2C0_SDA	USB3_DRD_JTG_TRST		
I2C1_SCL	USB3_DRD_JTG_TDI		
I2C1_SDA	USB3_DRD_JTG_TMS		
UART1_TXD	USB3_DRD_JTG_TDO		
UART3_TXD	CHIP_DBG_TXD		CHIP_DBG UART and SPI interface

PAD Name	Default	Function Select 1	Description
UART3_RXD	CHIP_DBG_RXD		
GPIO0_22	CHIP_DBG_SEL		
GPIO0_23	CHIP_DBG_SCLK		
GPIO0_24	CHIP_DBG_CSN		
GPIO0_25	CHIP_DBG_MOSI		
GPIO0_26	CHIP_DBG_MISO		
GPIO0_30	TRNG_CLK_OUT		TRNG observation signal
GPIO0_31	TRNG_TST_IDDQ		
GPIO1_0	DDRPHY_DTO_0		DDR PHY digital test output signal
GPIO1_1	DDRPHY_DTO_1		
GPIO1_2	CSI2X2_ALIGN		MIPI CSI DSI PHY function test control signal
GPIO1_3	CSI2X2_PHASE_0		
GPIO1_4	CSI2X2_PHASE_1		
GPIO1_5	MIPI_CSI2_CONT_AND		
GPIO1_6	MIPI_CSI2_CONT_OR		
GPIO1_7	MIPI_CSI2_CONT_EN		
GPIO1_8	MIPI_CSI2_TEST_OR		
GPIO1_9	MIPI_CSI2X2_A_CONT_AND		
GPIO1_10	MIPI_CSI2X2_A_CONT_OR		
GPIO1_11	MIPI_CSI2X2_A_CONT_EN		
GPIO1_12	MIPI_CSI2X2_A_TEST_OR		
GPIO1_13	MIPI_CSI2X2_B_CONT_AND		
GPIO1_14	MIPI_CSI2X2_B_CONT_OR		
GPIO1_15	MIPI_CSI2X2_B_CONT_EN		
GPIO1_16	MIPI_CSI2X2_B_TEST_OR		
GPIO1_21	MIPI_DSI0_BISTON		
GPIO1_22	MIPI_DSI1_CONT_AND		
GPIO1_23	MIPI_DSI1_CONT_OR		
GPIO1_24	MIPI_DSI1_CONT_EN		

PAD Name	Default	Function Select 1	Description
GPIO1_25	MIPI_DSI1_TEST_OR		
GPIO1_26	MIPI_DSI1_BISTON		
GPIO1_27	MIPI_DSI0_CONT_AND		
GPIO1_28	MIPI_DSI0_CONT_OR		
GPIO1_29	MIPI_DSI0_TEST_OR		
GPIO1_30	MIPI_DSI0_CONT_EN		
I2C2_SCL	C910_RSTN		C910 reset control signal
QSPI0_D0_MOSI	PLL_TEST_SEL_0		PLL function test control signal
QSPI0_D1_MISO	PLL_TEST_SEL_1		
QSPI0_D2_WP	PLL_TEST_SEL_2		
QSPI0_D3_HOLD	PLL_TEST_SEL_3		
I2C2_SDA	PLL_TEST_CLK		
I2C3_SCL	PLL_TEST_EN		
I2C3_SDA	PLL_ALLDSKEW_LOCK		
GPIO2_13	PLL_ALL_DSKEW_RDY		
SPI_SCLK	PLL_ALL_DSKEW_PASS		
SPI_CSN	PLL_DSKEW_CAL_OUT_0		
SPI_MOSI	PLL_DSKEW_CAL_OUT_1		
SPI_MISO	PLL_DSKEW_CAL_OUT_2		
GPIO2_18	PLL_DSKEW_CAL_OUT_3		
GPIO2_19	PLL_DSKEW_CAL_OUT_4		
GPIO2_20	PLL_DSKEW_CAL_OUT_5		
GPIO2_21	PLL_DSKEW_CAL_OUT_6		
GPIO2_22	PLL_DSKEW_CAL_OUT_7		
GPIO2_23	PLL_DSKEW_CAL_OUT_8		
GPIO2_24	PLL_DSKEW_CAL_OUT_9		
GPIO2_25	PLL_DSKEW_CAL_OUT_10		
SDIO0_WPRTN	PLL_DSKEW_CAL_OUT_11		
SDIO0_DETN	PLL_ALL_PASS		

PAD Name	Default	Function Select 1	Description
SDIO1_WPRTN	PLL_ALL_FREQ_PASS		
SDIO1_DETN	PLL_ALL_LOCK		
GPIO2_30	PLL_DSKEW_LOCK		
GPIO2_31	PLL_DSKEW_RDY		
GPIO3_0	PLL_FREQ_PASS		
GPIO3_1	PLL_LOCK		
GPIO3_2	HDMI_DTB0		HDMI PHY digital output observation signal
GPIO3_3	HDMI_DTB1		

3.2.3 Special PADs Description

Special PADs mainly refer to PADs related to system configurationuration, chip working mode, and chip startup. The detailed descriptions are as follows:

Figure & Table 3-7 System PADs description

PAD Name	Description
TEST_MODE	DFT test mode select 0: Function mode 1: DFT test mode
DEBUG_MODE	Debug mode select 0: Function mode. DEBUG_MODE can be multiplexed to GPIO function in function mode; 1: Debug mode. Chip works normally in debug mode and PADMUX is different.
POR_SEL	0: On chip POR is disabled. 1: On chip POR is enabled.
AOGPIO_7	PLL_DSKEW_BYPASS is enabled by default after power on. 0: PLL DSKEW calibration is enabled after power on. 1: PLL DSKEW calibration is disabled after power on.
AOGPIO_10	BISR_BYPASS is enabled by default after power on. 0: MEM BISR is enabled after power on. 1: MEM BISR is disabled after power on.
CLK_OUT_0	BOOT_SEL[2:0] is enabled by default after power on. 0XX: USB 100: eMMC
CLK_OUT_1	

PAD Name	Description
CLK_OUT_2	101: SD/TF card 110: SPI NAND (QSPI0) 111: SPI NOR (QSPI0)

3.3 PADMUX Register

3.3.1 Base Addresses of PADMUX Register

Figure & Table 3-8 Register the base Addresses of all registers

PAD Group	E902 Base Addresses	C906 Base Addresses	C910 Base Addresses
PAD Group 1 Registers	0xFFF4A000	0xFFFFF4A000	0xFFFFF4A000
PAD Group 2 Registers	0xB7F3C000	0xFFE7F3C000	0xFFE7F3C000
PAD Group 3 Registers	0xBC007000	0xFFEC007000	0xFFEC007000
MUX Registers in AUDIO_SUBSYS	0xCB01D000	0xFFCB01D000	0xFFCB01D000

3.3.2 Find Register by PAD Name

Figure & Table 3-9 PAD name and configuration register name map table

PAD Group	PAD Name	PADCFG Reg Name	PADCFG Offset	PADCFG Bits	MUXCFG Reg Name	MUXCFG Offset	MUXCFG Bits
1	OSC_CLK_IN	G1_PADCFG_001	0x0	[7:0]			
1	OSC_CLK_OUT						
1	SYS_RST_N						
1	RTC_CLK_IN	G1_PADCFG_002	0x4	[20:16]			
1	RTC_CLK_OUT						
1	TEST_MODE						
1	DEBUG_MODE			[25:16]	G1_MUXCFG_001	0x400	[31:28]
1	POR_SEL						
1	I2C_AON_SCL	G1_PADCFG_005	0x10	[25:16]	G1_MUXCFG_002	0x404	[7:4]
1	I2C_AON_SDA	G1_PADCFG_006	0x14	[9:0]	G1_MUXCFG_002	0x404	[11:8]
1	CPU_JTG_TCLK	G1_PADCFG_006	0x14	[25:16]	G1_MUXCFG_002	0x404	[15:12]
1	CPU_JTG_TMS	G1_PADCFG_007	0x18	[9:0]	G1_MUXCFG_002	0x404	[19:16]
1	CPU_JTG_TDI	G1_PADCFG_007	0x18	[25:16]	G1_MUXCFG_002	0x404	[23:20]
1	CPU_JTG_TDO	G1_PADCFG_008	0x1C	[9:0]	G1_MUXCFG_002	0x404	[27:24]
1	CPU_JTG_TRST	G1_PADCFG_008	0x1C	[25:16]	G1_MUXCFG_002	0x404	[31:28]

PAD Group	PAD Name	PADCFG Reg Name	PADCFG Offset	PADCFG Bits	MUXCFG Reg Name	MUXCFG Offset	MUXCFG Bits
1	AOGPIO_7	G1_PADCFG_009	0x20	[9:0]	G1_MUXCFG_003	0x408	[3:0]
1	AOGPIO_8	G1_PADCFG_009	0x20	[25:16]	G1_MUXCFG_003	0x408	[7:4]
1	AOGPIO_9	G1_PADCFG_010	0x24	[9:0]	G1_MUXCFG_003	0x408	[11:8]
1	AOGPIO_10	G1_PADCFG_010	0x24	[25:16]	G1_MUXCFG_003	0x408	[15:12]
1	AOGPIO_11	G1_PADCFG_011	0x28	[9:0]	G1_MUXCFG_003	0x408	[19:16]
1	AOGPIO_12	G1_PADCFG_011	0x28	[25:16]	G1_MUXCFG_003	0x408	[23:20]
1	AOGPIO_13	G1_PADCFG_012	0x2C	[9:0]	G1_MUXCFG_003	0x408	[27:24]
1	AOGPIO_14	G1_PADCFG_012	0x2C	[25:16]	G1_MUXCFG_003	0x408	[31:28]
1	AOGPIO_15	G1_PADCFG_013	0x30	[9:0]	G1_MUXCFG_004	0x40C	[3:0]
1	AUDIO_PA0	G1_PADCFG_013	0x30	[25:16]	G1_MUXCFG_004	0x40C	[7:4]
1	AUDIO_PA1	G1_PADCFG_014	0x34	[9:0]	G1_MUXCFG_004	0x40C	[11:8]
1	AUDIO_PA2	G1_PADCFG_014	0x34	[25:16]	G1_MUXCFG_004	0x40C	[15:12]
1	AUDIO_PA3	G1_PADCFG_015	0x38	[9:0]	G1_MUXCFG_004	0x40C	[19:16]
1	AUDIO_PA4	G1_PADCFG_015	0x38	[25:16]	G1_MUXCFG_004	0x40C	[23:20]
1	AUDIO_PA5	G1_PADCFG_016	0x3C	[9:0]	G1_MUXCFG_004	0x40C	[27:24]
1	AUDIO_PA6	G1_PADCFG_016	0x3C	[25:16]	G1_MUXCFG_004	0x40C	[31:28]
1	AUDIO_PA7	G1_PADCFG_017	0x40	[9:0]	G1_MUXCFG_005	0x410	[3:0]
1	AUDIO_PA8	G1_PADCFG_017	0x40	[25:16]	G1_MUXCFG_005	0x410	[7:4]
1	AUDIO_PA9	G1_PADCFG_018	0x44	[9:0]	G1_MUXCFG_005	0x410	[11:8]
1	AUDIO_PA10	G1_PADCFG_018	0x44	[25:16]	G1_MUXCFG_005	0x410	[15:12]
1	AUDIO_PA11	G1_PADCFG_019	0x48	[9:0]	G1_MUXCFG_005	0x410	[19:16]
1	AUDIO_PA12	G1_PADCFG_019	0x48	[25:16]	G1_MUXCFG_005	0x410	[23:20]
1	AUDIO_PA13	G1_PADCFG_020	0x4C	[9:0]	G1_MUXCFG_005	0x410	[27:24]
1	AUDIO_PA14	G1_PADCFG_020	0x4C	[25:16]	G1_MUXCFG_005	0x410	[31:28]
1	AUDIO_PA15	G1_PADCFG_021	0x50	[9:0]	G1_MUXCFG_006	0x414	[3:0]
1	AUDIO_PA16	G1_PADCFG_021	0x50	[25:16]	G1_MUXCFG_006	0x414	[7:4]
1	AUDIO_PA17	G1_PADCFG_022	0x54	[9:0]	G1_MUXCFG_006	0x414	[11:8]
1	AUDIO_PA27	G1_PADCFG_022	0x54	[25:16]	G1_MUXCFG_006	0x414	[15:12]
1	AUDIO_PA28	G1_PADCFG_023	0x58	[9:0]	G1_MUXCFG_006	0x414	[19:16]
1	AUDIO_PA29	G1_PADCFG_023	0x58	[25:16]	G1_MUXCFG_006	0x414	[23:20]
1	AUDIO_PA30	G1_PADCFG_024	0x5C	[9:0]	G1_MUXCFG_006	0x414	[27:24]
2	QSPI1_SCLK	G2_PADCFG_001	0x0	[9:0]	G2_MUXCFG_001	0x400	[3:0]
2	QSPI1_CSN0	G2_PADCFG_001	0x0	[25:16]	G2_MUXCFG_001	0x400	[7:4]
2	QSPI1_D0_MOSI	G2_PADCFG_002	0x4	[9:0]	G2_MUXCFG_001	0x400	[11:8]

PAD Group	PAD Name	PADCFG Reg Name	PADCFG Offset	PADCFG Bits	MUXCFG Reg Name	MUXCFG Offset	MUXCFG Bits
2	QSPI1_D1_MISO	G2_PADCFG_002	0x4	[25:16]	G2_MUXCFG_001	0x400	[15:12]
2	QSPI1_D2_WP	G2_PADCFG_003	0x8	[9:0]	G2_MUXCFG_001	0x400	[19:16]
2	QSPI1_D3_HOLD	G2_PADCFG_003	0x8	[25:16]	G2_MUXCFG_001	0x400	[23:20]
2	I2C0_SCL	G2_PADCFG_004	0xC	[9:0]	G2_MUXCFG_001	0x400	[27:24]
2	I2C0_SDA	G2_PADCFG_004	0xC	[25:16]	G2_MUXCFG_001	0x400	[31:28]
2	I2C1_SCL	G2_PADCFG_005	0x10	[9:0]	G2_MUXCFG_002	0x404	[3:0]
2	I2C1_SDA	G2_PADCFG_005	0x10	[25:16]	G2_MUXCFG_002	0x404	[7:4]
2	UART1_TXD	G2_PADCFG_006	0x14	[9:0]	G2_MUXCFG_002	0x404	[11:8]
2	UART1_RXD	G2_PADCFG_006	0x14	[25:16]	G2_MUXCFG_002	0x404	[15:12]
2	UART4_TXD	G2_PADCFG_007	0x18	[9:0]	G2_MUXCFG_002	0x404	[19:16]
2	UART4_RXD	G2_PADCFG_007	0x18	[25:16]	G2_MUXCFG_002	0x404	[23:20]
2	UART4_CTSN	G2_PADCFG_008	0x1C	[9:0]	G2_MUXCFG_002	0x404	[27:24]
2	UART4_RTSN	G2_PADCFG_008	0x1C	[25:16]	G2_MUXCFG_002	0x404	[31:28]
2	UART3_TXD	G2_PADCFG_009	0x20	[9:0]	G2_MUXCFG_003	0x408	[3:0]
2	UART3_RXD	G2_PADCFG_009	0x20	[25:16]	G2_MUXCFG_003	0x408	[7:4]
2	GPIO0_18	G2_PADCFG_010	0x24	[9:0]	G2_MUXCFG_003	0x408	[11:8]
2	GPIO0_19	G2_PADCFG_010	0x24	[25:16]	G2_MUXCFG_003	0x408	[15:12]
2	GPIO0_20	G2_PADCFG_011	0x28	[9:0]	G2_MUXCFG_003	0x408	[19:16]
2	GPIO0_21	G2_PADCFG_011	0x28	[25:16]	G2_MUXCFG_003	0x408	[23:20]
2	GPIO0_22	G2_PADCFG_012	0x2C	[9:0]	G2_MUXCFG_003	0x408	[27:24]
2	GPIO0_23	G2_PADCFG_012	0x2C	[25:16]	G2_MUXCFG_003	0x408	[31:28]
2	GPIO0_24	G2_PADCFG_013	0x30	[9:0]	G2_MUXCFG_004	0x40C	[3:0]
2	GPIO0_25	G2_PADCFG_013	0x30	[25:16]	G2_MUXCFG_004	0x40C	[7:4]
2	GPIO0_26	G2_PADCFG_014	0x34	[9:0]	G2_MUXCFG_004	0x40C	[11:8]
2	GPIO0_27	G2_PADCFG_014	0x34	[25:16]	G2_MUXCFG_004	0x40C	[15:12]
2	GPIO0_28	G2_PADCFG_015	0x38	[9:0]	G2_MUXCFG_004	0x40C	[19:16]
2	GPIO0_29	G2_PADCFG_015	0x38	[25:16]	G2_MUXCFG_004	0x40C	[23:20]
2	GPIO0_30	G2_PADCFG_016	0x3C	[9:0]	G2_MUXCFG_004	0x40C	[27:24]
2	GPIO0_31	G2_PADCFG_016	0x3C	[25:16]	G2_MUXCFG_004	0x40C	[31:28]
2	GPIO1_0	G2_PADCFG_017	0x40	[9:0]	G2_MUXCFG_005	0x410	[3:0]
2	GPIO1_1	G2_PADCFG_017	0x40	[25:16]	G2_MUXCFG_005	0x410	[7:4]
2	GPIO1_2	G2_PADCFG_018	0x44	[9:0]	G2_MUXCFG_005	0x410	[11:8]
2	GPIO1_3	G2_PADCFG_018	0x44	[25:16]	G2_MUXCFG_005	0x410	[15:12]
2	GPIO1_4	G2_PADCFG_019	0x48	[9:0]	G2_MUXCFG_005	0x410	[19:16]

PAD Group	PAD Name	PADCFG Reg Name	PADCFG Offset	PADCFG Bits	MUXCFG Reg Name	MUXCFG Offset	MUXCFG Bits
2	GPIO1_5	G2_PADCFG_019	0x48	[25:16]	G2_MUXCFG_005	0x410	[23:20]
2	GPIO1_6	G2_PADCFG_020	0x4C	[9:0]	G2_MUXCFG_005	0x410	[27:24]
2	GPIO1_7	G2_PADCFG_020	0x4C	[25:16]	G2_MUXCFG_005	0x410	[31:28]
2	GPIO1_8	G2_PADCFG_021	0x50	[9:0]	G2_MUXCFG_006	0x414	[3:0]
2	GPIO1_9	G2_PADCFG_021	0x50	[25:16]	G2_MUXCFG_006	0x414	[7:4]
2	GPIO1_10	G2_PADCFG_022	0x54	[9:0]	G2_MUXCFG_006	0x414	[11:8]
2	GPIO1_11	G2_PADCFG_022	0x54	[25:16]	G2_MUXCFG_006	0x414	[15:12]
2	GPIO1_12	G2_PADCFG_023	0x58	[9:0]	G2_MUXCFG_006	0x414	[19:16]
2	GPIO1_13	G2_PADCFG_023	0x58	[25:16]	G2_MUXCFG_006	0x414	[23:20]
2	GPIO1_14	G2_PADCFG_024	0x5C	[9:0]	G2_MUXCFG_006	0x414	[27:24]
2	GPIO1_15	G2_PADCFG_024	0x5C	[25:16]	G2_MUXCFG_006	0x414	[31:28]
2	GPIO1_16	G2_PADCFG_025	0x60	[9:0]	G2_MUXCFG_007	0x418	[3:0]
2	CLK_OUT_0	G2_PADCFG_025	0x60	[25:16]	G2_MUXCFG_007	0x418	[7:4]
2	CLK_OUT_1	G2_PADCFG_026	0x64	[9:0]	G2_MUXCFG_007	0x418	[11:8]
2	CLK_OUT_2	G2_PADCFG_026	0x64	[25:16]	G2_MUXCFG_007	0x418	[15:12]
2	CLK_OUT_3	G2_PADCFG_027	0x68	[9:0]	G2_MUXCFG_007	0x418	[19:16]
2	GPIO1_21	G2_PADCFG_027	0x68	[25:16]	G2_MUXCFG_007	0x418	[23:20]
2	GPIO1_22	G2_PADCFG_028	0x6C	[9:0]	G2_MUXCFG_007	0x418	[27:24]
2	GPIO1_23	G2_PADCFG_028	0x6C	[25:16]	G2_MUXCFG_007	0x418	[31:28]
2	GPIO1_24	G2_PADCFG_029	0x70	[9:0]	G2_MUXCFG_008	0x41C	[3:0]
2	GPIO1_25	G2_PADCFG_029	0x70	[25:16]	G2_MUXCFG_008	0x41C	[7:4]
2	GPIO1_26	G2_PADCFG_030	0x74	[9:0]	G2_MUXCFG_008	0x41C	[11:8]
2	GPIO1_27	G2_PADCFG_030	0x74	[25:16]	G2_MUXCFG_008	0x41C	[15:12]
2	GPIO1_28	G2_PADCFG_031	0x78	[9:0]	G2_MUXCFG_008	0x41C	[19:16]
2	GPIO1_29	G2_PADCFG_031	0x78	[25:16]	G2_MUXCFG_008	0x41C	[23:20]
2	GPIO1_30	G2_PADCFG_032	0x7C	[9:0]	G2_MUXCFG_008	0x41C	[27:24]
3	UART0_TXD	G3_PADCFG_001	0x0	[9:0]	G3_MUXCFG_001	0x400	[3:0]
3	UART0_RXD	G3_PADCFG_001	0x0	[25:16]	G3_MUXCFG_001	0x400	[7:4]
3	QSPI0_SCLK	G3_PADCFG_002	0x4	[9:0]	G3_MUXCFG_001	0x400	[11:8]
3	QSPI0_CSN0	G3_PADCFG_002	0x4	[25:16]	G3_MUXCFG_001	0x400	[15:12]
3	QSPI0_CSN1	G3_PADCFG_003	0x8	[9:0]	G3_MUXCFG_001	0x400	[19:16]
3	QSPI0_D0_MOSI	G3_PADCFG_003	0x8	[25:16]	G3_MUXCFG_001	0x400	[23:20]
3	QSPI0_D1_MISO	G3_PADCFG_004	0xC	[9:0]	G3_MUXCFG_001	0x400	[27:24]
3	QSPI0_D2_WP	G3_PADCFG_004	0xC	[25:16]	G3_MUXCFG_001	0x400	[31:28]

PAD Group	PAD Name	PADCFG Reg Name	PADCFG Offset	PADCFG Bits	MUXCFG Reg Name	MUXCFG Offset	MUXCFG Bits
3	QSPI0_D3_HOLD	G3_PADCFG_005	0x10	[9:0]	G3_MUXCFG_002	0x404	[3:0]
3	I2C2_SCL	G3_PADCFG_005	0x10	[25:16]	G3_MUXCFG_002	0x404	[7:4]
3	I2C2_SDA	G3_PADCFG_006	0x14	[9:0]	G3_MUXCFG_002	0x404	[11:8]
3	I2C3_SCL	G3_PADCFG_006	0x14	[25:16]	G3_MUXCFG_002	0x404	[15:12]
3	I2C3_SDA	G3_PADCFG_007	0x18	[9:0]	G3_MUXCFG_002	0x404	[19:16]
3	GPIO2_13	G3_PADCFG_007	0x18	[25:16]	G3_MUXCFG_002	0x404	[23:20]
3	SPI_SCLK	G3_PADCFG_008	0x1C	[9:0]	G3_MUXCFG_002	0x404	[27:24]
3	SPI_CSN	G3_PADCFG_008	0x1C	[25:16]	G3_MUXCFG_002	0x404	[31:28]
3	SPI_MOSI	G3_PADCFG_009	0x20	[9:0]	G3_MUXCFG_003	0x408	[3:0]
3	SPI_MISO	G3_PADCFG_009	0x20	[25:16]	G3_MUXCFG_003	0x408	[7:4]
3	GPIO2_18	G3_PADCFG_010	0x24	[9:0]	G3_MUXCFG_003	0x408	[11:8]
3	GPIO2_19	G3_PADCFG_010	0x24	[25:16]	G3_MUXCFG_003	0x408	[15:12]
3	GPIO2_20	G3_PADCFG_011	0x28	[9:0]	G3_MUXCFG_003	0x408	[19:16]
3	GPIO2_21	G3_PADCFG_011	0x28	[25:16]	G3_MUXCFG_003	0x408	[23:20]
3	GPIO2_22	G3_PADCFG_012	0x2C	[9:0]	G3_MUXCFG_003	0x408	[27:24]
3	GPIO2_23	G3_PADCFG_012	0x2C	[25:16]	G3_MUXCFG_003	0x408	[31:28]
3	GPIO2_24	G3_PADCFG_013	0x30	[9:0]	G3_MUXCFG_004	0x40C	[3:0]
3	GPIO2_25	G3_PADCFG_013	0x30	[25:16]	G3_MUXCFG_004	0x40C	[7:4]
3	SDIO0_WPRTN	G3_PADCFG_014	0x34	[9:0]	G3_MUXCFG_004	0x40C	[11:8]
3	SDIO0_DETN	G3_PADCFG_014	0x34	[25:16]	G3_MUXCFG_004	0x40C	[15:12]
3	SDIO1_WPRTN	G3_PADCFG_015	0x38	[9:0]	G3_MUXCFG_004	0x40C	[19:16]
3	SDIO1_DETN	G3_PADCFG_015	0x38	[25:16]	G3_MUXCFG_004	0x40C	[23:20]
3	GPIO2_30	G3_PADCFG_016	0x3C	[9:0]	G3_MUXCFG_004	0x40C	[27:24]
3	GPIO2_31	G3_PADCFG_016	0x3C	[25:16]	G3_MUXCFG_004	0x40C	[31:28]
3	GPIO3_0	G3_PADCFG_017	0x40	[9:0]	G3_MUXCFG_005	0x410	[3:0]
3	GPIO3_1	G3_PADCFG_017	0x40	[25:16]	G3_MUXCFG_005	0x410	[7:4]
3	GPIO3_2	G3_PADCFG_018	0x44	[9:0]	G3_MUXCFG_005	0x410	[11:8]
3	GPIO3_3	G3_PADCFG_018	0x44	[25:16]	G3_MUXCFG_005	0x410	[15:12]
3	HDMI_SCL	G3_PADCFG_019	0x48	[9:0]	G3_MUXCFG_005	0x410	[19:16]
3	HDMI_SDA	G3_PADCFG_019	0x48	[25:16]	G3_MUXCFG_005	0x410	[23:20]
3	HDMI_CEC	G3_PADCFG_020	0x4C	[9:0]	G3_MUXCFG_005	0x410	[27:24]
3	GMAC0_TX_CLK	G3_PADCFG_020	0x4C	[25:16]	G3_MUXCFG_005	0x410	[31:28]
3	GMAC0_RX_CLK	G3_PADCFG_021	0x50	[9:0]	G3_MUXCFG_006	0x414	[3:0]
3	GMAC0_TXEN	G3_PADCFG_021	0x50	[25:16]	G3_MUXCFG_006	0x414	[7:4]

PAD Group	PAD Name	PADCFG Reg Name	PADCFG Offset	PADCFG Bits	MUXCFG Reg Name	MUXCFG Offset	MUXCFG Bits
3	GMAC0_TXD0	G3_PADCFG_022	0x54	[9:0]	G3_MUXCFG_006	0x414	[11:8]
3	GMAC0_TXD1	G3_PADCFG_022	0x54	[25:16]	G3_MUXCFG_006	0x414	[15:12]
3	GMAC0_TXD2	G3_PADCFG_023	0x58	[9:0]	G3_MUXCFG_006	0x414	[19:16]
3	GMAC0_TXD3	G3_PADCFG_023	0x58	[25:16]	G3_MUXCFG_006	0x414	[23:20]
3	GMAC0_RXDV	G3_PADCFG_024	0x5C	[9:0]	G3_MUXCFG_006	0x414	[27:24]
3	GMAC0_RXD0	G3_PADCFG_024	0x5C	[25:16]	G3_MUXCFG_006	0x414	[31:28]
3	GMAC0_RXD1	G3_PADCFG_025	0x60	[9:0]	G3_MUXCFG_007	0x418	[3:0]
3	GMAC0_RXD2	G3_PADCFG_025	0x60	[25:16]	G3_MUXCFG_007	0x418	[7:4]
3	GMAC0_RXD3	G3_PADCFG_026	0x64	[9:0]	G3_MUXCFG_007	0x418	[11:8]
3	GMAC0_MDC	G3_PADCFG_026	0x64	[25:16]	G3_MUXCFG_007	0x418	[15:12]
3	GMAC0_MDIO	G3_PADCFG_027	0x68	[9:0]	G3_MUXCFG_007	0x418	[19:16]
3	GMAC0_COL	G3_PADCFG_027	0x68	[25:16]	G3_MUXCFG_007	0x418	[23:20]
3	GMAC0_CRS	G3_PADCFG_028	0x6C	[9:0]	G3_MUXCFG_007	0x418	[27:24]

3.3.3 Register Memory Map

Figure & Table 3-10 Register memory map

Register	Offset	Description	Section/Page
G1_PADCFG_001	0x0	Pad cell configuration register for pad: OSC_CLK_IN	3.3.4.1/59
G1_PADCFG_002	0x4	Pad cell configuration register for pad: RTC_CLK_IN	3.3.4.2/60
G1_PADCFG_005	0x10	Pad cell configuration register for pad: I2C_AON_SCL	3.3.4.3/60
G1_PADCFG_006	0x14	Pad cell configuration register for pad: I2C_AON_SDA, CPU_JTG_TCLK	3.3.4.4/61
G1_PADCFG_007	0x18	Pad cell configuration register for pad: CPU_JTG_TMS, CPU_JTG_TDI	3.3.4.5/62
G1_PADCFG_008	0x1C	Pad cell configuration register for pad: CPU_JTG_TDO, CPU_JTG_TRST	3.3.4.6/63
G1_PADCFG_009	0x20	Pad cell configuration register for pad: AOGPIO_7, AOGPIO_8	3.3.4.7/64
G1_PADCFG_010	0x24	Pad cell configuration register for pad: AOGPIO_9, AOGPIO_10	3.3.4.8/65
G1_PADCFG_011	0x28	Pad cell configuration register for pad:	3.3.4.9/66

Register	Offset	Description	Section/Page
		AOGPIO_11, AOGPIO_12	
G1_PADCFG_012	0x2C	Pad cell configuration register for pad: AOGPIO_13, AOGPIO_14	3.3.4.10/67
G1_PADCFG_013	0x30	Pad cell configuration register for pad: AOGPIO_15, AUDIO_PA0	3.3.4.11/68
G1_PADCFG_014	0x34	Pad cell configuration register for pad: AUDIO_PA1, AUDIO_PA2	3.3.4.12/69
G1_PADCFG_015	0x38	Pad cell configuration register for pad: AUDIO_PA3, AUDIO_PA4	3.3.4.13/70
G1_PADCFG_016	0x3C	Pad cell configuration register for pad: AUDIO_PA5, AUDIO_PA6	3.3.4.14/71
G1_PADCFG_017	0x40	Pad cell configuration register for pad: AUDIO_PA7, AUDIO_PA8	3.3.4.15/72
G1_PADCFG_018	0x44	Pad cell configuration register for pad: AUDIO_PA9, AUDIO_PA10	3.3.4.16/73
G1_PADCFG_019	0x48	Pad cell configuration register for pad: AUDIO_PA11, AUDIO_PA12	3.3.4.17/74
G1_PADCFG_020	0x4C	Pad cell configuration register for pad: AUDIO_PA13, AUDIO_PA14	3.3.4.18/75
G1_PADCFG_021	0x50	Pad cell configuration register for pad: AUDIO_PA15, AUDIO_PA16	3.3.4.19/76
G1_PADCFG_022	0x54	Pad cell configuration register for pad: AUDIO_PA17, AUDIO_PA27	3.3.4.20/77
G1_PADCFG_023	0x58	Pad cell configuration register for pad: AUDIO_PA28, AUDIO_PA29	3.3.4.21/78
G1_PADCFG_024	0x5C	Pad cell configuration register for pad: AUDIO_PA30	3.3.4.22/79
G1_MUXCFG_001	0x400	MUX configuration register for pad: DEBUG_MODE	3.3.4.23/80
G1_MUXCFG_002	0x404	MUX configuration register for pad: I2C_SON_SCL, I2C_AON_SDA, CPU_JTG_TCLK, CPU_JTG_TMS, CPU_JTG_TDI, CPU_JTG_TDO, CPU_JTG_TRST	3.3.4.24/80
G1_MUXCFG_003	0x408	MUX configuration register for pad: AOGPIO_7, AOGPIO_8, AOGPIO_9, AOGPIO_10, AOGPIO_11, AOGPIO_12,	3.3.4.25/81

Register	Offset	Description	Section/Page
		AOGPIO_13, AOGPIO_14	
G1_MUXCFG_004	0x40C	MUX configuration register for pad: AOGPIO_15, AUDIO_PA0, AUDIO_PA1, AUDIO_PA2, AUDIO_PA3, AUDIO_PA4, AUDIO_PA5, AUDIO_PA6	3.3.4.26/83
G1_MUXCFG_005	0x410	MUX configuration register for pad: AUDIO_PA7, AUDIO_PA8, AUDIO_PA9, AUDIO_PA10, AUDIO_PA11, AUDIO_PA12, AUDIO_PA13, AUDIO_PA14	3.3.4.27/84
G1_MUXCFG_006	0x414	MUX configuration register for pad: AUDIO_PA15, AUDIO_PA16, AUDIO_PA17, AUDIO_PA27, AUDIO_PA28, AUDIO_PA29, AUDIO_PA30	3.3.4.28/85
G2_PADCFG_001	0x0	Pad cell configuration register for pad: QSPI1_SCLK, QSPI1_CSN0	3.3.4.29/86
G2_PADCFG_002	0x4	Pad cell configuration register for pad: QSPI1_D0_MOSI, QSPI1_D1_MISO	3.3.4.30/87
G2_PADCFG_003	0x8	Pad cell configuration register for pad: QSPI1_D2_WP, QSPI1_D3_HOLD	3.3.4.31/88
G2_PADCFG_004	0xC	Pad cell configuration register for pad: I2C0_SCL, I2C0_SDA	3.3.4.32/89
G2_PADCFG_005	0x10	Pad cell configuration register for pad: I2C1_SCL, I2C1_SDA	3.3.4.33/90
G2_PADCFG_006	0x14	Pad cell configuration register for pad: UART1_TXD, UART1_RXD	3.3.4.34/91
G2_PADCFG_007	0x18	Pad cell configuration register for pad: UART4_TXD, UART4_RXD	3.3.4.35/92
G2_PADCFG_008	0x1C	Pad cell configuration register for pad: UART4_CTSN, UART4_RTSN	3.3.4.36/93
G2_PADCFG_009	0x20	Pad cell configuration register for pad: UART3_TXD, UART3_RXD	3.3.4.37/94
G2_PADCFG_010	0x24	Pad cell configuration register for pad: GPIO0_18, GPIO0_19	3.3.4.38/95
G2_PADCFG_011	0x28	Pad cell configuration register for pad: GPIO0_20, GPIO0_21	3.3.4.39/96
G2_PADCFG_012	0x2C	Pad cell configuration register for pad: GPIO0_22, GPIO0_23	3.3.4.40/97

Register	Offset	Description	Section/Page
G2_PADCFG_013	0x30	Pad cell configuration register for pad: GPIO0_24, GPIO0_25	3.3.4.41/98
G2_PADCFG_014	0x34	Pad cell configuration register for pad: GPIO0_26, GPIO0_27	3.3.4.42/99
G2_PADCFG_015	0x38	Pad cell configuration register for pad: GPIO0_28, GPIO0_29	3.3.4.43/100
G2_PADCFG_016	0x3C	Pad cell configuration register for pad: GPIO0_30, GPIO0_31	3.3.4.44/101
G2_PADCFG_017	0x40	Pad cell configuration register for pad: GPIO1_0, GPIO1_1	3.3.4.45/102
G2_PADCFG_018	0x44	Pad cell configuration register for pad: GPIO1_2, GPIO1_3	3.3.4.46/103
G2_PADCFG_019	0x48	Pad cell configuration register for pad: GPIO1_4, GPIO1_5	3.3.4.47/104
G2_PADCFG_020	0x4C	Pad cell configuration register for pad: GPIO1_6, GPIO1_7	3.3.4.48/105
G2_PADCFG_021	0x50	Pad cell configuration register for pad: GPIO1_8, GPIO1_9	3.3.4.49/106
G2_PADCFG_022	0x54	Pad cell configuration register for pad: GPIO1_10, GPIO1_11	3.3.4.50/107
G2_PADCFG_023	0x58	Pad cell configuration register for pad: GPIO1_12, GPIO1_13	3.3.4.51/108
G2_PADCFG_024	0x5C	Pad cell configuration register for pad: GPIO1_14, GPIO1_15	3.3.4.52/109
G2_PADCFG_025	0x60	Pad cell configuration register for pad: GPIO1_16, CLK_OUT_0	3.3.4.53/110
G2_PADCFG_026	0x64	Pad cell configuration register for pad: CLK_OUT_1, CLK_OUT_2	3.3.4.54/111
G2_PADCFG_027	0x68	Pad cell configuration register for pad: CLK_OUT_3, GPIO1_21	3.3.4.55/112
G2_PADCFG_028	0x6C	Pad cell configuration register for pad: GPIO1_22, GPIO1_23	3.3.4.56/113
G2_PADCFG_029	0x70	Pad cell configuration register for pad: GPIO1_24, GPIO1_25	3.3.4.57/114
G2_PADCFG_030	0x74	Pad cell configuration register for pad:	3.3.4.58/115

Register	Offset	Description	Section/Page
		GPIO1_26, GPIO1_27	
G2_PADCFG_031	0x78	Pad cell configuration register for pad: GPIO1_28, GPIO1_29	3.3.4.59/116
G2_PADCFG_032	0x7C	Pad cell configuration register for pad: GPIO1_30	3.3.4.60/117
G2_MUXCFG_001	0x400	MUX configuration register for pad: QSPI1_SCLK, QSPI1_CSN0, QSPI1_D0_MOSI, QSPI1_D1_MISO, QSPI1_D2_WP, QSPI1_D3_HOLD, I2C0_SCL, I2C0_SDA	3.3.4.61/118
G2_MUXCFG_002	0x404	MUX configuration register for pad: I2C1_SCL, I2C1_SDA, UART1_TXD, UART1_RXD, UART4_TXD, UART4_RXD, UART4_CTSN, UART4_RTSN	3.3.4.62/120
G2_MUXCFG_003	0x408	MUX configuration register for pad: UART3_TXD, UART3_RXD, GPIO0_18, GPIO0_19, GPIO0_20, GPIO0_21, GPIO0_22, GPIO0_23	3.3.4.63/121
G2_MUXCFG_004	0x40C	MUX configuration register for pad: GPIO0_24, GPIO0_25, GPIO0_26, GPIO0_27, GPIO0_28, GPIO0_29, GPIO0_30, GPIO0_31	3.3.4.64/122
G2_MUXCFG_005	0x410	MUX configuration register for pad: GPIO1_0, GPIO1_1, GPIO1_2, GPIO1_3, GPIO1_4, GPIO1_5, GPIO1_6, GPIO1_7	3.3.4.65/124
G2_MUXCFG_006	0x414	MUX configuration register for pad: GPIO1_8, GPIO1_9, GPIO1_10, GPIO1_11, GPIO1_12, GPIO1_13, GPIO1_14, GPIO1_15	3.3.4.66/126
G2_MUXCFG_007	0x418	MUX configuration register for pad: GPIO1_16, CLK_OUT_0, CLK_OUT_1, CLK_OUT_2, CLK_OUT_3, GPIO1_21, GPIO1_22, GPIO1_23	3.3.4.67/127
G2_MUXCFG_008	0x41C	MUX configuration register for pad: GPIO1_24, GPIO1_25, GPIO1_26, GPIO1_27, GPIO1_28, GPIO1_29, GPIO1_30	3.3.4.68/129
G3_PADCFG_001	0x0	Pad cell configuration register for pad: UART0_TXD, UART0_RXD	3.3.4.69/130
G3_PADCFG_002	0x4	Pad cell configuration register for pad: QSPI0_SCLK, QSPI0_CSN0	3.3.4.70/131
G3_PADCFG_003	0x8	Pad cell configuration register for pad:	3.3.4.71/132

Register	Offset	Description	Section/Page
		QSPI0_CSN1, QSPI0_D0_MOSI	
G3_PADCFG_004	0xC	Pad cell configuration register for pad: QSPI0_D1_MISO, QSPI0_D2_WP	3.3.4.72/133
G3_PADCFG_005	0x10	Pad cell configuration register for pad: QSPI0_D3_HOLD, I2C2_SCL	3.3.4.73/134
G3_PADCFG_006	0x14	Pad cell configuration register for pad: I2C2_SDA, I2C3_SCL	3.3.4.74/135
G3_PADCFG_007	0x18	Pad cell configuration register for pad: I2C3_SDA, GPIO2_13	3.3.4.75/136
G3_PADCFG_008	0x1C	Pad cell configuration register for pad: SPI_SCLK, SPI_CSN	3.3.4.76/137
G3_PADCFG_009	0x20	Pad cell configuration register for pad: SPI_MOSI, SPI_MISO	3.3.4.77/138
G3_PADCFG_010	0x24	Pad cell configuration register for pad: GPIO2_18, GPIO2_19	3.3.4.78/139
G3_PADCFG_011	0x28	Pad cell configuration register for pad: GPIO2_20, GPIO2_21	3.3.4.79/140
G3_PADCFG_012	0x2C	Pad cell configuration register for pad: GPIO2_22, GPIO2_23	3.3.4.80/141
G3_PADCFG_013	0x30	Pad cell configuration register for pad: GPIO2_24, GPIO2_25	3.3.4.81/142
G3_PADCFG_014	0x34	Pad cell configuration register for pad: SDIO0_WPRTN, SDIO0_DETN	3.3.4.82/143
G3_PADCFG_015	0x38	Pad cell configuration register for pad: SDIO1_WPRTN, SDIO1_DETN	3.3.4.83/144
G3_PADCFG_016	0x3C	Pad cell configuration register for pad: GPIO2_30, GPIO2_31	3.3.4.84/145
G3_PADCFG_017	0x40	Pad cell configuration register for pad: GPIO3_0, GPIO3_1	3.3.4.85/146
G3_PADCFG_018	0x44	Pad cell configuration register for pad: GPIO3_2, GPIO3_3	3.3.4.86/147
G3_PADCFG_019	0x48	Pad cell configuration register for pad: HDMI_SCL, HDMI_SDA	3.3.4.87/148
G3_PADCFG_020	0x4C	Pad cell configuration register for pad: HDMI_CEC, GMAC0_TX_CLK	3.3.4.88/149

Register	Offset	Description	Section/Page
G3_PADCFG_021	0x50	Pad cell configuration register for pad: GMAC0_RX_CLK, GMAC0_TXEN	3.3.4.89/150
G3_PADCFG_022	0x54	Pad cell configuration register for pad: GMAC0_TXD0, GMAC0_TXD1	3.3.4.90/151
G3_PADCFG_023	0x58	Pad cell configuration register for pad: GMAC0_TXD2, GMAC0_TXD3	3.3.4.91/152
G3_PADCFG_024	0x5C	Pad cell configuration register for pad: GMAC0_RXDV, GMAC0_RXD0	3.3.4.92/153
G3_PADCFG_025	0x60	Pad cell configuration register for pad: GMAC0_RXD1, GMAC0_RXD2	3.3.4.93/154
G3_PADCFG_026	0x64	Pad cell configuration register for pad: GMAC0_RXD3, GMAC0_MDC	3.3.4.94/155
G3_PADCFG_027	0x68	Pad cell configuration register for pad: GMAC0_MDIO, GMAC0_COL	3.3.4.95/156
G3_PADCFG_028	0x6C	Pad cell configuration register for pad: GMAC0_CRS	3.3.4.96/157
G3_MUXCFG_001	0x400	MUX configuration register for pad: UART0_TXD, UART0_RXD, QSPI0_SCLK, QSPI0_CSN0, QSPI0_CSN1, QSPI0_D0_MOSI, QSPI0_D1_MISO, QSPI0_D2_WP	3.3.4.97/158
G3_MUXCFG_002	0x404	MUX configuration register for pad: QSPI0_D3_HOLD, I2C2_SCL, I2C2_SDA, I2C3_SCL, I2C3_SDA, GPIO2_13, SPI_SCLK, SPI_CSN	3.3.4.98/160
G3_MUXCFG_003	0x408	MUX configuration register for pad: SPI_MOSI, SPI_MISO, GPIO2_18, GPIO2_19, GPIO2_20, GPIO2_21, GPIO2_22, GPIO2_23	3.3.4.99/161
G3_MUXCFG_004	0x40C	MUX configuration register for pad: GPIO2_24, GPIO2_25, SDIO0_WPRTN, SDIO0_DETN, SDIO1_WPRTN, SDIO1_DETN, GPIO2_30, GPIO2_31	3.3.4.100/162
G3_MUXCFG_005	0x410	MUX configuration register for pad: GPIO3_0, GPIO3_1, GPIO3_2, GPIO3_3, HDMI_SCL, HDMI_SDA, HDMI_CEC, GMAC0_TX_CLK	3.3.4.101/163
G3_MUXCFG_006	0x414	MUX configuration register for pad: GMAC0_RX_CLK, GMAC0_TXEN, GMAC0_TXD0, GMAC0_TXD1, GMAC0_TXD2,	3.3.4.102/165

Register	Offset	Description	Section/Page
		GMAC0_TXD3, GMAC0_RXDV, GMAC0_RXD0	
G3_MUXCFG_007	0x418	MUX configuration register for pad: GMAC0_RXD1, GMAC0_RXD2, GMAC0_RXD3, GMAC0_MDC, GMAC0_MDIO, GMAC0_COL, GMAC0_CRS	3.3.4.103/166
AUDIO_IO_GPIO_SEL	0x00	AUDIO PAD mode configuration register	3.3.4.104/167
AUDIO_IO_MUXCFG_001	0x04	AUDIO PAD Alternative function mode selection register	3.3.4.105/172
AUDIO_IO_MUXCFG_002	0x08	AUDIO PAD Alternative function mode selection register	3.3.4.106/175
AUDIO_IO_PADCFG_001	0x0C	PAD cell configuration register for AUDIO_PA0 and AUDIO_PA1. Only valid when PAD in AUDIO_SUBSYS function mode.	3.3.4.107/178
AUDIO_IO_PADCFG_002	0x10	PAD cell configuration register for AUDIO_PA2 and AUDIO_PA3. Only valid when PAD in AUDIO_SUBSYS function mode.	3.3.4.108/179
AUDIO_IO_PADCFG_003	0x14	PAD cell configuration register for AUDIO_PA4 and AUDIO_PA5. Only valid when PAD in AUDIO_SUBSYS function mode.	3.3.4.109/180
AUDIO_IO_PADCFG_004	0x18	PAD cell configuration register for AUDIO_PA6 and AUDIO_PA7. Only valid when PAD in AUDIO_SUBSYS function mode.	3.3.4.110/181
AUDIO_IO_PADCFG_005	0x1C	PAD cell configuration register for AUDIO_PA8 and AUDIO_PA9. Only valid when PAD in AUDIO_SUBSYS function mode.	3.3.4.111/182
AUDIO_IO_PADCFG_006	0x20	PAD cell configuration register for AUDIO_PA10 and AUDIO_PA11. Only valid when PAD in AUDIO_SUBSYS function mode.	3.3.4.112/184
AUDIO_IO_PADCFG_007	0x24	PAD cell configuration register for AUDIO_PA12 and AUDIO_PA13. Only valid when PAD in AUDIO_SUBSYS function mode.	3.3.4.113/185
AUDIO_IO_PADCFG_008	0x28	PAD cell configuration register for	3.3.4.114/186

Register	Offset	Description	Section/Page
		AUDIO_PA14 and AUDIO_PA15. Only valid when PAD in AUDIO_SUBSYS function mode.	
AUDIO_IO_PADCFG_009	0x2C	PAD cell configuration register for AUDIO_PA16 and AUDIO_PA17. Only valid when PAD in AUDIO_SUBSYS function mode.	3.3.4.115/187
AUDIO_IO_PADCFG_010	0x30	PAD cell configuration register for AUDIO_PA18 and AUDIO_PA19. Only valid when PAD in AUDIO_SUBSYS function mode.	3.3.4.116/188
AUDIO_IO_PADCFG_011	0x34	PAD cell configuration register for AUDIO_PA20 and AUDIO_PA21. Only valid when PAD in AUDIO_SUBSYS function mode.	3.3.4.117/189
AUDIO_IO_PADCFG_012	0x38	PAD cell configuration register for AUDIO_PA22 and AUDIO_PA23. Only valid when PAD in AUDIO_SUBSYS function mode.	3.3.4.118/190
AUDIO_IO_PADCFG_013	0x3C	PAD cell configuration register for AUDIO_PA24 and AUDIO_PA25. Only valid when PAD in AUDIO_SUBSYS function mode.	3.3.4.119/191
AUDIO_IO_PADCFG_014	0x40	PAD cell configuration register for AUDIO_PA26 and AUDIO_PA27. Only valid when PAD in AUDIO_SUBSYS function mode.	3.3.4.120/192
AUDIO_IO_PADCFG_015	0x44	PAD cell configuration register for AUDIO_PA28 and AUDIO_PA29. Only valid when PAD in AUDIO_SUBSYS function mode.	3.3.4.121/193
AUDIO_IO_PADCFG_016	0x48	PAD cell configuration register for AUDIO_PA30. Only valid when PAD in AUDIO_SUBSYS function mode.	3.3.4.122/194

3.3.4 Register and Field Description

3.3.4.1 G1_PADCFG_001

- Description: Pad cell configuration register for pad: OSC_CLK_IN
- Offset: 0x0; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910

- Default Value: 0x125

Bits	Field Name	Access	Description
[31:9]	RESERVED_1	-	
[8:0]	OSC_CLK_IN_PAD_CFG	RW	Pad cell configuration: {RD1, RD0, REF1, REF0, DS3, DS2, DS1, DS0} [RD1:RD0]: Build-in damping resistance RD 00: ~200R 01: ~500R 10: ~1K 11: ~1.5K [REF1,REF0]: Feedback resistance RF 00: Disable (open) 01: ~0.75M 10: ~1M 11: ~1.5M [DS3,DS2,DS1,DS0]: Driving strength Value After Reset: 0x125

3.3.4.2 G1_PADCFG_002

- Description: Pad cell configuration register for pad: RTC_CLK_IN
- Offset: 0x4; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x1a0000

Bits	Field Name	Access	Description
[31:21]	RESERVED_2	-	
[20:16]	RTC_CLK_IN_PAD_CFG	RW	{REF, XE, DS2, DS1, DS0} REF: Feedback resistance RF 0: Disable (open) 1: ~10M [DS2,DS1,DS0]: Driving strength Value After Reset: 0x1A
[15:0]	RESERVED_1	-	

3.3.4.3 G1_PADCFG_005

- Description: Pad cell configuration register for pad: I2C_AON_SCL
- Offset: 0x10; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910

- Default Value: 0x2380000

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	I2C_AON_SCL_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x238
[15:0]	RESERVED_1	-	

3.3.4.4 G1_PADCFG_006

- Description: Pad cell configuration register for pad: I2C_AON_SDA, CPU_JTG_TCLK
- Offset: 0x14; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080238

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	CPU_JTG_TCLK_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull

Bits	Field Name	Access	Description
			up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	I2C_AON_SDA_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x238

3.3.4.5 G1_PADCFG_007

- Description: Pad cell configuration register for pad: CPU_JTG_TMS, CPU_JTG_TDI
- Offset: 0x18; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080238

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	CPU_JTG_TDI_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down.

Bits	Field Name	Access	Description
			PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	CPU_JTG_TMS_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x238

3.3.4.6 G1_PADCFG_008

- Description: Pad cell configuration register for pad: CPU_JTG_TDO, CPU_JTG_TRST
- Offset: 0x1C; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2380208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	CPU_JTG_TRST_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-

Bits	Field Name	Access	Description
			down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x238
[15:10]	RESERVED_1	-	
[9:0]	CPU_JTG_TDO_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.7 G1_PADCFG_009

- Description: Pad cell configuration register for pad: AOGPIO_7, AOGPIO_8
- Offset: 0x20; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080218

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	AOGPIO_8_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor.

Bits	Field Name	Access	Description
			PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	AOGPIO_7_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x218

3.3.4.8 G1_PADCFG_010

- Description: Pad cell configuration register for pad: AOGPIO_9, AOGPIO_10
- Offset: 0x24; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2180208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	AOGPIO_10_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular.

Bits	Field Name	Access	Description
			SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x218
[15:10]	RESERVED_1	-	
[9:0]	AOGPIO_9_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.9 G1_PADCFG_011

- Description: Pad cell configuration register for pad: AOGPIO_11, AOGPIO_12
- Offset: 0x28; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	AOGPIO_12_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal

Bits	Field Name	Access	Description
			more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	AOGPIO_11_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.10 G1_PADCFG_012

- Description: Pad cell configuration register for pad: AOGPIO_13, AOGPIO_14
- Offset: 0x2C; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	AOGPIO_14_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad.

Bits	Field Name	Access	Description
			ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	AOGPIO_13_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.11 G1_PADCFG_013

- Description: Pad cell configuration register for pad: AOGPIO_15, AUDIO_PA0
- Offset: 0x30; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	AUDIO_PA0_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster

Bits	Field Name	Access	Description
			transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	AOGPIO_15_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.12 G1_PADCFG_014

- Description: Pad cell configuration register for pad: AUDIO_PA1, AUDIO_PA2
- Offset: 0x34; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	AUDIO_PA2_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core.

Bits	Field Name	Access	Description
			SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	AUDIO_PA1_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.13 G1_PADCFG_015

- Description: Pad cell configuration register for pad: AUDIO_PA3, AUDIO_PA4
- Offset: 0x38; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	AUDIO_PA4_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to

Bits	Field Name	Access	Description
			enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	AUDIO_PA3_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.14 G1_PADCFG_016

- Description: Pad cell configuration register for pad: AUDIO_PA5, AUDIO_PA6
- Offset: 0x3C; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	AUDIO_PA6_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0}

Bits	Field Name	Access	Description
			IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	AUDIO_PA5_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.15 G1_PADCFG_017

- Description: Pad cell configuration register for pad: AUDIO_PA7, AUDIO_PA8
- Offset: 0x40; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	

Bits	Field Name	Access	Description
[25:16]	AUDIO_PA8_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	AUDIO_PA7_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.16 G1_PADCFG_018

- Description: Pad cell configuration register for pad: AUDIO_PA9, AUDIO_PA10
- Offset: 0x44; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	AUDIO_PA10_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	AUDIO_PA9_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.17 G1_PADCFG_019

- Description: Pad cell configuration register for pad: AUDIO_PA11, AUDIO_PA12
- Offset: 0x48; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	AUDIO_PA12_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	AUDIO_PA11_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.18 G1_PADCFG_020

- Description: Pad cell configuration register for pad: AUDIO_PA13, AUDIO_PA14
- Offset: 0x4C; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	AUDIO_PA14_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	AUDIO_PA13_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.19 G1_PADCFG_021

- Description: Pad cell configuration register for pad: AUDIO_PA15, AUDIO_PA16
- Offset: 0x50; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	AUDIO_PA16_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	AUDIO_PA15_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.20 G1_PADCFG_022

- Description: Pad cell configuration register for pad: AUDIO_PA17, AUDIO_PA27
- Offset: 0x54; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	AUDIO_PA27_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	AUDIO_PA17_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.21 G1_PADCFG_023

- Description: Pad cell configuration register for pad: AUDIO_PA28, AUDIO_PA29
- Offset: 0x58; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	AUDIO_PA29_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	AUDIO_PA28_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.22 G1_PADCFG_024

- Description: Pad cell configuration register for pad: AUDIO_PA30
- Offset: 0x5C; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x208

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9:0]	AUDIO_PA30_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.23 G1_MUXCFG_001

- Description: MUX configuration register for pad: DEBUG_MODE
- Offset: 0x400; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	DEBUG_MODE_MUX_CFG	RW	MUX configuration for pad: DEBUG_MODE 0000: DEBUG_MODE 0011: GPIO4_22 Value After Reset: 0x0
[27:0]	RESERVED_1	-	

3.3.4.24 G1_MUXCFG_002

- Description: MUX configuration register for pad: I2C_SON_SCL, I2C_AON_SDA, CPU_JTG_TCLK, CPU_JTG_TMS, CPU_JTG_TDI, CPU_JTG_TDO, CPU_JTG_TRST
- Offset: 0x404; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	CPU_JTG_TRST_MUX_CFG	RW	MUX configuration for pad: CPU_JTG_TRST

Bits	Field Name	Access	Description
			0000: CPU_JTG_TRST 0011: AOGPIO_6 Value After Reset: 0x0
[27:24]	CPU_JTG_TDO_MUX_CFG	RW	MUX configuration for pad: CPU_JTG_TDO 0000: CPU_JTG_TDO 0011: AOGPIO_5 Value After Reset: 0x0
[23:20]	CPU_JTG_TDI_MUX_CFG	RW	MUX configuration for pad: CPU_JTG_TDI 0000: CPU_JTG_TDI 0011: AOGPIO_4 Value After Reset: 0x0
[19:16]	CPU_JTG_TMS_MUX_CFG	RW	MUX configuration for pad: CPU_JTG_TMS 0000: CPU_JTG_TMS 0011: AOGPIO_3 Value After Reset: 0x0
[15:12]	CPU_JTG_TCLK_MUX_CFG	RW	MUX configuration for pad: CPU_JTG_TCLK 0000: CPU_JTG_TCLK 0011: AOGPIO_2 Value After Reset: 0x0
[11:8]	I2C_AON_SDA_MUX_CFG	RW	MUX configuration for pad: I2C_AON_SDA 0000: I2C_AON_SDA 0011: AOGPIO_1 Value After Reset: 0x0
[7:4]	I2C_AON_SCL_MUX_CFG	RW	MUX configuration for pad: I2C_AON_SCL 0000: I2C_AON_SCL 0011: AOGPIO_0 Value After Reset: 0x0
[3:0]	RESERVED_1	-	

3.3.4.25 G1_MUXCFG_003

- Description: MUX configuration register for pad: AOGPIO_7, AOGPIO_8, AOGPIO_9, AOGPIO_10, AOGPIO_11, AOGPIO_12, AOGPIO_13, AOGPIO_14
- Offset: 0x408; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	AOGPIO_14_MUX_CFG	RW	MUX configuration for pad: AOGPIO_14 0000: AOGPIO_14 0001: AUDIO_PA25 Value After Reset: 0x0
[27:24]	AOGPIO_13_MUX_CFG	RW	MUX configuration for pad: AOGPIO_13 0000: AOGPIO_13 0001: AUDIO_PA24 Value After Reset: 0x0
[23:20]	AOGPIO_12_MUX_CFG	RW	MUX configuration for pad: AOGPIO_12 0000: AOGPIO_12 0001: AUDIO_PA23 Value After Reset: 0x0
[19:16]	AOGPIO_11_MUX_CFG	RW	MUX configuration for pad: AOGPIO_11 0000: AOGPIO_11 0001: AUDIO_PA22 Value After Reset: 0x0
[15:12]	AOGPIO_10_MUX_CFG	RW	MUX configuration for pad: AOGPIO_10 0000: BISR_BYPASS 0001: AUDIO_PA21 0011: AOGPIO_10 Value After Reset: 0x0
[11:8]	AOGPIO_9_MUX_CFG	RW	MUX configuration for pad: AOGPIO_9 0000: AOUART_RXD 0001: AUDIO_PA20 0010: AOUART_IR_IN 0011: AOGPIO_9 Value After Reset: 0x0
[7:4]	AOGPIO_8_MUX_CFG	RW	MUX configuration for pad: AOGPIO_8 0000: AOUART_TXD 0001: AUDIO_PA19 0010: AOUART_IR_OUT 0011: AOGPIO_8 Value After Reset: 0x0
[3:0]	AOGPIO_7_MUX_CFG	RW	MUX configuration for pad: AOGPIO_7

Bits	Field Name	Access	Description
			0000: PLL_DSKEW_BYPASS 0001: AUDIO_PA18 0011: AOGPIO_7 Value After Reset: 0x0

3.3.4.26 G1_MUXCFG_004

- Description: MUX configuration register for pad: AOGPIO_15, AUDIO_PA0, AUDIO_PA1, AUDIO_PA2, AUDIO_PA3, AUDIO_PA4, AUDIO_PA5, AUDIO_PA6
- Offset: 0x40C; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	AUDIO_PA6_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA6 0000: AUDIO_PA6 0011: GPIO4_6 Value After Reset: 0x0
[27:24]	AUDIO_PA5_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA5 0000: AUDIO_PA5 0011: GPIO4_5 Value After Reset: 0x0
[23:20]	AUDIO_PA4_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA4 0000: AUDIO_PA4 0011: GPIO4_4 Value After Reset: 0x0
[19:16]	AUDIO_PA3_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA3 0000: AUDIO_PA3 0011: GPIO4_3 Value After Reset: 0x0
[15:12]	AUDIO_PA2_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA2 0000: AUDIO_PA2 0011: GPIO4_2 Value After Reset: 0x0
[11:8]	AUDIO_PA1_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA1 0000: AUDIO_PA1 0011: GPIO4_1

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[7:4]	AUDIO_PA0_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA0 0000: AUDIO_PA0 0011: GPIO4_0 Value After Reset: 0x0
[3:0]	AOGPIO_15_MUX_CFG	RW	MUX configuration for pad: AOGPIO_15 0000: AOGPIO_15 0001: AUDIO_PA26 Value After Reset: 0x0

3.3.4.27 G1_MUXCFG_005

- Description: MUX configuration register for pad: AUDIO_PA7, AUDIO_PA8, AUDIO_PA9, AUDIO_PA10, AUDIO_PA11, AUDIO_PA12, AUDIO_PA13, AUDIO_PA14
- Offset: 0x410; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	AUDIO_PA14_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA14 0000: AUDIO_PA14 0011: GPIO4_14 Value After Reset: 0x0
[27:24]	AUDIO_PA13_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA13 0000: AUDIO_PA13 0011: GPIO4_13 Value After Reset: 0x0
[23:20]	AUDIO_PA12_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA12 0000: AUDIO_PA12 0011: GPIO4_12 Value After Reset: 0x0
[19:16]	AUDIO_PA11_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA11 0000: AUDIO_PA11 0011: GPIO4_11 Value After Reset: 0x0

Bits	Field Name	Access	Description
[15:12]	AUDIO_PA10_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA10 0000: AUDIO_PA10 0011: GPIO4_10 Value After Reset: 0x0
[11:8]	AUDIO_PA9_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA9 0000: AUDIO_PA9 0011: GPIO4_9 Value After Reset: 0x0
[7:4]	AUDIO_PA8_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA8 0000: AUDIO_PA8 0011: GPIO4_8 Value After Reset: 0x0
[3:0]	AUDIO_PA7_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA7 0000: AUDIO_PA7 0011: GPIO4_7 Value After Reset: 0x0

3.3.4.28 G1_MUXCFG_006

- Description: MUX configuration register for pad: AUDIO_PA15, AUDIO_PA16, AUDIO_PA17, AUDIO_PA27, AUDIO_PA28, AUDIO_PA29, AUDIO_PA30
- Offset: 0x414; Base Address: 0xFFF4A000 for E902, 0xFFFFF4A000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	RESERVED_1	-	
[27:24]	AUDIO_PA30_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA30 0000: AUDIO_PA30 0001: SE_RSTN 0011: GPIO4_21 Value After Reset: 0x0
[23:20]	AUDIO_PA29_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA29 0000: AUDIO_PA29 0011: GPIO4_20 Value After Reset: 0x0

Bits	Field Name	Access	Description
[19:16]	AUDIO_PA28_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA28 0000: AUDIO_PA28 0011: GPIO4_19 Value After Reset: 0x0
[15:12]	AUDIO_PA27_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA27 0000: AUDIO_PA27 0011: GPIO4_18 Value After Reset: 0x0
[11:8]	AUDIO_PA17_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA17 0000: AUDIO_PA17 0011: GPIO4_17 Value After Reset: 0x0
[7:4]	AUDIO_PA16_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA16 0000: AUDIO_PA16 0011: GPIO4_16 Value After Reset: 0x0
[3:0]	AUDIO_PA15_MUX_CFG	RW	MUX configuration for pad: AUDIO_PA15 0000: AUDIO_PA15 0011: GPIO4_15 Value After Reset: 0x0

3.3.4.29 G2_PADCFG_001

- Description: Pad cell configuration register for pad: QSPI1_SCLK, QSPI1_CSN0
- Offset: 0x0; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	

Bits	Field Name	Access	Description
[25:16]	QSPI1_CSN0_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	QSPI1_SCLK_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.30 G2_PADCFG_002

- Description: Pad cell configuration register for pad: QSPI1_D0_MOSI, QSPI1_D1_MISO
- Offset: 0x4; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	QSPI1_D1_MISO_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	QSPI1_D0_MOSI_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.31 G2_PADCFG_003

- Description: Pad cell configuration register for pad: QSPI1_D2_WP, QSPI1_D3_HOLD
- Offset: 0x8; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	QSPI1_D3_HOLD_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	QSPI1_D2_WP_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.32 G2_PADCFG_004

- Description: Pad cell configuration register for pad: I2C0_SCL, I2C0_SDA
- Offset: 0xC; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2380238

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	I2C0_SDA_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x238
[15:10]	RESERVED_1	-	
[9:0]	I2C0_SCL_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x238

3.3.4.33 G2_PADCFG_005

- Description: Pad cell configuration register for pad: I2C1_SCL, I2C1_SDA
- Offset: 0x10; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2380238

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	I2C1_SDA_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x238
[15:10]	RESERVED_1	-	
[9:0]	I2C1_SCL_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x238

3.3.4.34 G2_PADCFG_006

- Description: Pad cell configuration register for pad: UART1_TXD, UART1_RXD
- Offset: 0x14; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	UART1_RXD_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	UART1_TXD_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.35 G2_PADCFG_007

- Description: Pad cell configuration register for pad: UART4_TXD, UART4_RXD
- Offset: 0x18; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	UART4_RXD_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	UART4_TXD_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.36 G2_PADCFG_008

- Description: Pad cell configuration register for pad: UART4_CTSN, UART4_RTSN
- Offset: 0x1C; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	UART4_RTSN_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	UART4_CTSN_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.37 G2_PADCFG_009

- Description: Pad cell configuration register for pad: UART3_TXD, UART3_RXD
- Offset: 0x20; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	UART3_RXD_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	UART3_TXD_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.38 G2_PADCFG_010

- Description: Pad cell configuration register for pad: GPIO0_18, GPIO0_19
- Offset: 0x24; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO0_19_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO0_18_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.39 G2_PADCFG_011

- Description: Pad cell configuration register for pad: GPIO0_20, GPIO0_21
- Offset: 0x28; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO0_21_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO0_20_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.40 G2_PADCFG_012

- Description: Pad cell configuration register for pad: GPIO0_22, GPIO0_23
- Offset: 0x2C; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO0_23_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO0_22_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.41 G2_PADCFG_013

- Description: Pad cell configuration register for pad: GPIO0_24, GPIO0_25
- Offset: 0x30; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO0_25_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO0_24_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.42 G2_PADCFG_014

- Description: Pad cell configuration register for pad: GPIO0_26, GPIO0_27
- Offset: 0x34; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2380208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO0_27_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x238
[15:10]	RESERVED_1	-	
[9:0]	GPIO0_26_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.43 G2_PADCFG_015

- Description: Pad cell configuration register for pad: GPIO0_28, GPIO0_29
- Offset: 0x38; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2380238

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO0_29_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x238
[15:10]	RESERVED_1	-	
[9:0]	GPIO0_28_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x238

3.3.4.44 G2_PADCFG_016

- Description: Pad cell configuration register for pad: GPIO0_30, GPIO0_31
- Offset: 0x3C; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO0_31_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO0_30_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.45 G2_PADCFG_017

- Description: Pad cell configuration register for pad: GPIO1_0, GPIO1_1
- Offset: 0x40; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO1_1_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO1_0_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.46 G2_PADCFG_018

- Description: Pad cell configuration register for pad: GPIO1_2, GPIO1_3
- Offset: 0x44; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO1_3_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO1_2_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.47 G2_PADCFG_019

- Description: Pad cell configuration register for pad: GPIO1_4, GPIO1_5
- Offset: 0x48; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO1_5_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO1_4_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.48 G2_PADCFG_020

- Description: Pad cell configuration register for pad: GPIO1_6, GPIO1_7
- Offset: 0x4C; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO1_7_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO1_6_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.49 G2_PADCFG_021

- Description: Pad cell configuration register for pad: GPIO1_8, GPIO1_9
- Offset: 0x50; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO1_9_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO1_8_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.50 G2_PADCFG_022

- Description: Pad cell configuration register for pad: GPIO1_10, GPIO1_11
- Offset: 0x54; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO1_11_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO1_10_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.51 G2_PADCFG_023

- Description: Pad cell configuration register for pad: GPIO1_12, GPIO1_13
- Offset: 0x58; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO1_13_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO1_12_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.52 G2_PADCFG_024

- Description: Pad cell configuration register for pad: GPIO1_14, GPIO1_15
- Offset: 0x5C; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO1_15_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO1_14_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.53 G2_PADCFG_025

- Description: Pad cell configuration register for pad: GPIO1_16, CLK_OUT_0
- Offset: 0x60; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	CLK_OUT_0_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO1_16_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.54 G2_PADCFG_026

- Description: Pad cell configuration register for pad: CLK_OUT_1, CLK_OUT_2
- Offset: 0x64; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	CLK_OUT_2_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	CLK_OUT_1_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.55 G2_PADCFG_027

- Description: Pad cell configuration register for pad: CLK_OUT_3, GPIO1_21
- Offset: 0x68; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO1_21_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	CLK_OUT_3_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: write 1 to enable slew rate control, to get a faster transition on pad. ST: write 1 to enable schmitt trigger, make input signal more regular. SPU: write 1 to enable internal strong pull-up resistor. PS: pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.56 G2_PADCFG_028

- Description: Pad cell configuration register for pad: GPIO1_22, GPIO1_23
- Offset: 0x6C; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO1_23_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO1_22_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.57 G2_PADCFG_029

- Description: Pad cell configuration register for pad: GPIO1_24, GPIO1_25
- Offset: 0x70; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO1_25_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO1_24_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.58 G2_PADCFG_030

- Description: Pad cell configuration register for pad: GPIO1_26, GPIO1_27
- Offset: 0x74; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO1_27_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO1_26_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.59 G2_PADCFG_031

- Description: Pad cell configuration register for pad: GPIO1_28, GPIO1_29
- Offset: 0x78; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO1_29_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO1_28_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.60 G2_PADCFG_032

- Description: Pad cell configuration register for pad: GPIO1_30
- Offset: 0x7C; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x208

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9:0]	GPIO1_30_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.61 G2_MUXCFG_001

- Description: MUX configuration register for pad: QSPI1_SCLK, QSPI1_CSN0, QSPI1_D0_MOSI, QSPI1_D1_MISO, QSPI1_D2_WP, QSPI1_D3_HOLD, I2C0_SCL, I2C0_SDA
- Offset: 0x400; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	I2C0_SDA_MUX_CFG	RW	MUX configuration for pad: I2C0_SDA 0000: I2C0_SDA 0011: GPIO0_7 Value After Reset: 0x0
[27:24]	I2C0_SCL_MUX_CFG	RW	MUX configuration for pad: I2C0_SCL 0000: I2C0_SCL 0011: GPIO0_6 Value After Reset: 0x0
[23:20]	QSPI1_D3_HOLD_MUX_CFG	RW	MUX configuration for pad: QSPI1_D3_HOLD 0000: QSPI1_M3_HOLD 0001: ISO7816_DAT 0010: UART5_RXD

Bits	Field Name	Access	Description
			0011: GPIO0_5 Value After Reset: 0x0
[19:16]	QSPI1_D2_WP_MUX_CFG	RW	MUX configuration for pad: QSPI1_D2_WP 0000: QSPI1_M2_WP 0001: ISO7816_RST 0010: UART5_TXD 0011: GPIO0_4 0100: EFUSE_BUSY Value After Reset: 0x0
[15:12]	QSPI1_D1_MISO_MUX_CFG	RW	MUX configuration for pad: QSPI1_D1_MISO 0000: QSPI1_M1_MISO 0001: ISO7816_CLK 0011: GPIO0_3 0100: EFUSE_SPI_SO Value After Reset: 0x0
[11:8]	QSPI1_D0_MOSI_MUX_CFG	RW	MUX configuration for pad: QSPI1_D0_MOSI 0000: QSPI1_M0_MOSI 0001: ISO7816_CVCC_EN 0010: I2C5_SDA 0011: GPIO0_2 0100: EFUSE_SPI_SI Value After Reset: 0x0
[7:4]	QSPI1_CSN0_MUX_CFG	RW	MUX configuration for pad: QSPI1_CSN0 0000: QSPI1_SSN0 0010: I2C5_SCL 0011: GPIO0_1 0100: EFUSE_SPI_NSS Value After Reset: 0x0
[3:0]	QSPI1_SCLK_MUX_CFG	RW	MUX configuration for pad: QSPI1_SCLK 0000: QSPI1_SCLK 0001: ISO7816_DET 0011: GPIO0_0 0100: EFUSE_SPI_CLK Value After Reset: 0x0

3.3.4.62 G2_MUXCFG_002

- Description: MUX configuration register for pad: I2C1_SCL, I2C1_SDA, UART1_TXD, UART1_RXD, UART4_TXD, UART4_RXD, UART4_CTSN, UART4_RTSN
- Offset: 0x404; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	UART4_RTSN_MUX_CFG	RW	MUX configuration for pad: UART4_RTSN 0000: UART4_RTSN 0011: GPIO0_15 Value After Reset: 0x0
[27:24]	UART4_CTSN_MUX_CFG	RW	MUX configuration for pad: UART4_CTSN 0000: UART4_CTSN 0011: GPIO0_14 Value After Reset: 0x0
[23:20]	UART4_RXD_MUX_CFG	RW	MUX configuration for pad: UART4_RXD 0000: UART4_RXD 0011: GPIO0_13 Value After Reset: 0x0
[19:16]	UART4_TXD_MUX_CFG	RW	MUX configuration for pad: UART4_TXD 0000: UART4_TXD 0011: GPIO0_12 Value After Reset: 0x0
[15:12]	UART1_RXD_MUX_CFG	RW	MUX configuration for pad: UART1_RXD 0000: UART1_RXD 0011: GPIO0_11 Value After Reset: 0x0
[11:8]	UART1_TXD_MUX_CFG	RW	MUX configuration for pad: UART1_TXD 0000: UART1_TXD 0011: GPIO0_10 Value After Reset: 0x0
[7:4]	I2C1_SDA_MUX_CFG	RW	MUX configuration for pad: I2C1_SDA 0000: I2C1_SDA 0011: GPIO0_9 Value After Reset: 0x0

Bits	Field Name	Access	Description
[3:0]	I2C1_SCL_MUX_CFG	RW	MUX configuration for pad: I2C1_SCL 0000: I2C1_SCL 0011: GPIO0_8 Value After Reset: 0x0

3.3.4.63 G2_MUXCFG_003

- Description: MUX configuration register for pad: UART3_TXD, UART3_RXD, GPIO0_18, GPIO0_19, GPIO0_20, GPIO0_21, GPIO0_22, GPIO0_23
- Offset: 0x408; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	GPIO0_23_MUX_CFG	RW	MUX configuration for pad: GPIO0_23 0000: GPIO0_23 0001: DSP0_JTG_TMS 0010: I2C4_SDA 0100: DPU_COLOR_2 0101: DPU1_COLOR_2 Value After Reset: 0x0
[27:24]	GPIO0_22_MUX_CFG	RW	MUX configuration for pad: GPIO0_22 0000: GPIO0_22 0001: DSP0_JTG_TRST 0010: I2C4_SCL 0100: DPU_COLOR_1 0101: DPU1_COLOR_1 Value After Reset: 0x0
[23:20]	GPIO0_21_MUX_CFG	RW	MUX configuration for pad: GPIO0_21 0000: GPIO0_21 0001: UART3_RXD 0010: UART3_IR_IN 0100: DPU_COLOR_0 0101: DPU1_COLOR_0 Value After Reset: 0x0

Bits	Field Name	Access	Description
[19:16]	GPIO0_20_MUX_CFG	RW	MUX configuration for pad: GPIO0_20 0000: GPIO0_20 0001: UART3_TXD 0010: UART3_IR_OUT 0100: DPU_COLOR_8 0101: DPU1_COLOR_8 Value After Reset: 0x0
[15:12]	GPIO0_19_MUX_CFG	RW	MUX configuration for pad: GPIO0_19 0000: GPIO0_19 0001: I2C4_SDA 0100: DPU_COLOR_7 0101: DPU1_COLOR_7 Value After Reset: 0x0
[11:8]	GPIO0_18_MUX_CFG	RW	MUX configuration for pad: GPIO0_18 0000: GPIO0_18 0001: I2C4_SCL 0100: DPU_COLOR_6 0101: DPU1_COLOR_6 Value After Reset: 0x0
[7:4]	UART3_RXD_MUX_CFG	RW	MUX configuration for pad: UART3_RXD 0000: CHIP_DBG_RXD 0001: UART3_RXD 0011: GPIO0_17 Value After Reset: 0x0
[3:0]	UART3_TXD_MUX_CFG	RW	MUX configuration for pad: UART3_TXD 0000: CHIP_DBG_TXD 0001: UART3_TXD 0011: GPIO0_16 Value After Reset: 0x0

3.3.4.64 G2_MUXCFG_004

- Description: MUX configuration register for pad: GPIO0_24, GPIO0_25, GPIO0_26, GPIO0_27, GPIO0_28, GPIO0_29, GPIO0_30, GPIO0_31
- Offset: 0x40C; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	GPIO0_31_MUX_CFG	RW	MUX configuration for pad: GPIO0_31 0000: GPIO0_31 0100: DPU_COLOR_10 0101: DPU1_COLOR_10 Value After Reset: 0x0
[27:24]	GPIO0_30_MUX_CFG	RW	MUX configuration for pad: GPIO0_30 0000: GPIO0_30 0100: DPU_COLOR_9 0101: DPU1_COLOR_9 Value After Reset: 0x0
[23:20]	GPIO0_29_MUX_CFG	RW	MUX configuration for pad: GPIO0_29 0000: GPIO0_29 0100: DPU_COLOR_8 0101: DPU1_COLOR_8 Value After Reset: 0x0
[19:16]	GPIO0_28_MUX_CFG	RW	MUX configuration for pad: GPIO0_28 0000: GPIO0_28 0010: I2C1_SDA 0100: DPU_COLOR_7 0101: DPU1_COLOR_7 Value After Reset: 0x0
[15:12]	GPIO0_27_MUX_CFG	RW	MUX configuration for pad: GPIO0_27 0000: GPIO0_27 0010: I2C1_SCL 0100: DPU_COLOR_6 0101: DPU1_COLOR_6 Value After Reset: 0x0
[11:8]	GPIO0_26_MUX_CFG	RW	MUX configuration for pad: GPIO0_26 0000: GPIO0_26 0001: DSP0_JTG_TCLK 0100: DPU_COLOR_5 0101: DPU1_COLOR_5 Value After Reset: 0x0

Bits	Field Name	Access	Description
[7:4]	GPIO0_25_MUX_CFG	RW	MUX configuration for pad: GPIO0_25 0000: GPIO0_25 0001: DSP0_JTG_TDO 0100: DPU_COLOR_4 0101: DPU1_COLOR_4 Value After Reset: 0x0
[3:0]	GPIO0_24_MUX_CFG	RW	MUX configuration for pad: GPIO0_24 0000: GPIO0_24 0001: DSP0_JTG_TDI 0010: QSPI1_SSN1 0100: DPU_COLOR_3 0101: DPU1_COLOR_3 Value After Reset: 0x0

3.3.4.65 G2_MUXCFG_005

- Description: MUX configuration register for pad: GPIO1_0, GPIO1_1, GPIO1_2, GPIO1_3, GPIO1_4, GPIO1_5, GPIO1_6, GPIO1_7
- Offset: 0x410; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	GPIO1_7_MUX_CFG	RW	MUX configuration for pad: GPIO1_7 0000: GPIO1_7 0001: QSPI1_SSN0 0100: DPU_COLOR_18 0101: DPU1_COLOR_18 Value After Reset: 0x0
[27:24]	GPIO1_6_MUX_CFG	RW	MUX configuration for pad: GPIO1_6 0000: GPIO1_6 0001: QSPI1_SCLK 0100: DPU_COLOR_17 0101: DPU1_COLOR_17 Value After Reset: 0x0

Bits	Field Name	Access	Description
[23:20]	GPIO1_5_MUX_CFG	RW	MUX configuration for pad: GPIO1_5 0000: GPIO1_5 0100: DPU_COLOR_16 0101: DPU1_COLOR_16 Value After Reset: 0x0
[19:16]	GPIO1_4_MUX_CFG	RW	MUX configuration for pad: GPIO1_4 0000: GPIO1_4 0001: DSP1_JTG_TCLK 0100: DPU_COLOR_15 0101: DPU1_COLOR_15 Value After Reset: 0x0
[15:12]	GPIO1_3_MUX_CFG	RW	MUX configuration for pad: GPIO1_3 0000: GPIO1_3 0001: DSP1_JTG_TDO 0100: DPU_COLOR_14 0101: DPU1_COLOR_14 Value After Reset: 0x0
[11:8]	GPIO1_2_MUX_CFG	RW	MUX configuration for pad: GPIO1_2 0000: GPIO1_2 0001: DSP1_JTG_TDI 0100: DPU_COLOR_13 0101: DPU1_COLOR_13 Value After Reset: 0x0
[7:4]	GPIO1_1_MUX_CFG	RW	MUX configuration for pad: GPIO1_1 0000: GPIO1_1 0001: DSP1_JTG_TMS 0100: DPU_COLOR_12 0101: DPU1_COLOR_12 Value After Reset: 0x0

Bits	Field Name	Access	Description
[3:0]	GPIO1_0_MUX_CFG	RW	MUX configuration for pad: GPIO1_0 0000: GPIO1_0 0001: DSP1_JTG_TRST 0100: DPU_COLOR_11 0101: DPU1_COLOR_11 Value After Reset: 0x0

3.3.4.66 G2_MUXCFG_006

- Description: MUX configuration register for pad: GPIO1_8, GPIO1_9, GPIO1_10, GPIO1_11, GPIO1_12, GPIO1_13, GPIO1_14, GPIO1_15
- Offset: 0x414; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	GPIO1_15_MUX_CFG	RW	MUX configuration for pad: GPIO1_15 0000: GPIO1_15 0001: UART4_CTSN 0100: DPU_VSYNC 0101: DPU1_VSYNC Value After Reset: 0x0
[27:24]	GPIO1_14_MUX_CFG	RW	MUX configuration for pad: GPIO1_14 0000: GPIO1_14 0001: UART4_RXD 0100: DPU_HSYNC 0101: DPU1_HSYNC Value After Reset: 0x0
[23:20]	GPIO1_13_MUX_CFG	RW	MUX configuration for pad: GPIO1_13 0000: GPIO1_13 0001: UART4_TXD 0100: DPU_COLOR_EN 0101: DPU1_COLOR_EN Value After Reset: 0x0

Bits	Field Name	Access	Description
[19:16]	GPIO1_12_MUX_CFG	RW	MUX configuration for pad: GPIO1_12 0000: GPIO1_12 0001: QSPI1_M3_HOLD 0100: DPU_COLOR_23 0101: DPU1_COLOR_23 Value After Reset: 0x0
[15:12]	GPIO1_11_MUX_CFG	RW	MUX configuration for pad: GPIO1_11 0000: GPIO1_11 0001: QSPI1_M3_HOLD 0100: DPU_COLOR_22 0101: DPU1_COLOR_22 Value After Reset: 0x0
[11:8]	GPIO1_10_MUX_CFG	RW	MUX configuration for pad: GPIO1_10 0000: GPIO1_10 0001: QSPI1_M2_WP 0100: DPU_COLOR_21 0101: DPU1_COLOR_21 Value After Reset: 0x0
[7:4]	GPIO1_9_MUX_CFG	RW	MUX configuration for pad: GPIO1_9 0000: GPIO1_9 0001: QSPI1_M1_MISO 0100: DPU_COLOR_20 0101: DPU1_COLOR_20 Value After Reset: 0x0
[3:0]	GPIO1_8_MUX_CFG	RW	MUX configuration for pad: GPIO1_8 0000: GPIO1_8 0001: QSPI1_M0_MOSI 0100: DPU_COLOR_19 0101: DPU1_COLOR_19 Value After Reset: 0x0

3.3.4.67 G2_MUXCFG_007

- Description: MUX configuration register for pad: GPIO1_16, CLK_OUT_0, CLK_OUT_1, CLK_OUT_2, CLK_OUT_3, GPIO1_21, GPIO1_22, GPIO1_23
- Offset: 0x418; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	GPIO1_23_MUX_CFG	RW	MUX configuration for pad: GPIO1_23 0000: C910_JTG_TDI 0010: ISP0_PRELIGHT_TRIG 0011: GPIO1_23 Value After Reset: 0x0
[27:24]	GPIO1_22_MUX_CFG	RW	MUX configuration for pad: GPIO1_22 0000: C910_JTG_TMS 0010: ISP0_FLASH_TRIG 0011: GPIO1_22 Value After Reset: 0x0
[23:20]	GPIO1_21_MUX_CFG	RW	MUX configuration for pad: GPIO1_21 0000: C910_JTG_TCLK 0010: ISP0_FL_TRIG 0011: GPIO1_21 Value After Reset: 0x0
[19:16]	CLK_OUT_3_MUX_CFG	RW	MUX configuration for pad: CLK_OUT_3 0000: BOOT_SEL3 0001: CLK_OUT_3 0011: GPIO1_20 Value After Reset: 0x0
[15:12]	CLK_OUT_2_MUX_CFG	RW	MUX configuration for pad: CLK_OUT_2 0000: BOOT_SEL2 0001: CLK_OUT_2 0011: GPIO1_19 Value After Reset: 0x0
[11:8]	CLK_OUT_1_MUX_CFG	RW	MUX configuration for pad: CLK_OUT_1 0000: BOOT_SEL1 0001: CLK_OUT_1 0011: GPIO1_18 Value After Reset: 0x0

Bits	Field Name	Access	Description
[7:4]	CLK_OUT_0_MUX_CFG	RW	MUX configuration for pad: CLK_OUT_0 0000: BOOT_SEL0 0001: CLK_OUT_0 0011: GPIO1_17 Value After Reset: 0x0
[3:0]	GPIO1_16_MUX_CFG	RW	MUX configuration for pad: GPIO1_16 0000: GPIO1_16 0001: UART4_RTSN 0100: DPU_PIXELCLK 0101: DPU1_PIXELCLK Value After Reset: 0x0

3.3.4.68 G2_MUXCFG_008

- Description: MUX configuration register for pad: GPIO1_24, GPIO1_25, GPIO1_26, GPIO1_27, GPIO1_28, GPIO1_29, GPIO1_30
- Offset: 0x41C; Base Address: 0xB7F3C000 for E902, 0xFFE7F3C000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	RESERVED_1	-	
[27:24]	GPIO1_30_MUX_CFG	RW	MUX configuration for pad: GPIO1_30 0000: GPIO1_30 0010: ISP1_SHUTTER_OPEN Value After Reset: 0x0
[23:20]	GPIO1_29_MUX_CFG	RW	MUX configuration for pad: GPIO1_29 0000: GPIO1_29 0010: ISP1_SHUTTER_TRIG Value After Reset: 0x0
[19:16]	GPIO1_28_MUX_CFG	RW	MUX configuration for pad: GPIO1_28 0000: GPIO1_28 0010: ISP1_PRELIGHT_TRIG Value After Reset: 0x0

Bits	Field Name	Access	Description
[15:12]	GPIO1_27_MUX_CFG	RW	MUX configuration for pad: GPIO1_27 0000: GPIO1_27 0010: ISP1_FLASH_TRIG Value After Reset: 0x0
[11:8]	GPIO1_26_MUX_CFG	RW	MUX configuration for pad: GPIO1_26 0000: GPIO1_26 0010: ISP1_FL_TRIG Value After Reset: 0x0
[7:4]	GPIO1_25_MUX_CFG	RW	MUX configuration for pad: GPIO1_25 0000: C910_JTG_TRST 0010: ISP0_SHUTTER_OPEN 0011: GPIO1_25 Value After Reset: 0x0
[3:0]	GPIO1_24_MUX_CFG	RW	MUX configuration for pad: GPIO1_24 0000: C910_JTG_TDO 0010: ISP0_SHUTTER_TRIG 0011: GPIO1_24 Value After Reset: 0x0

3.3.4.69 G3_PADCFG_001

- Description: Pad cell configuration register for pad: UART0_TXD, UART0_RXD
- Offset: 0x0; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	UART0_RXD_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down.

Bits	Field Name	Access	Description
			PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	UART0_TXD_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.70 G3_PADCFG_002

- Description: Pad cell configuration register for pad: QSPI0_SCLK, QSPI0_CSN0
- Offset: 0x4; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	QSPI0_CSN0_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-

Bits	Field Name	Access	Description
			down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	QSPI0_SCLK_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.71 G3_PADCFG_003

- Description: Pad cell configuration register for pad: QSPI0_CSN1, QSPI0_D0_MOSI
- Offset: 0x8; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	QSPI0_D0_MOSI_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor.

Bits	Field Name	Access	Description
			PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	QSPI0_CSN1_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.72 G3_PADCFG_004

- Description: Pad cell configuration register for pad: QSPI0_D1_MISO, QSPI0_D2_WP
- Offset: 0xC; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	QSPI0_D2_WP_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular.

Bits	Field Name	Access	Description
			SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	QSPI0_D1_MISO_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.73 G3_PADCFG_005

- Description: Pad cell configuration register for pad: QSPI0_D3_HOLD, I2C2_SCL
- Offset: 0x10; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	I2C2_SCL_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal

Bits	Field Name	Access	Description
			more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	QSPI0_D3_HOLD_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.74 G3_PADCFG_006

- Description: Pad cell configuration register for pad: I2C2_SDA, I2C3_SCL
- Offset: 0x14; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	I2C3_SCL_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad.

Bits	Field Name	Access	Description
			ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	I2C2_SDA_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.75 G3_PADCFG_007

- Description: Pad cell configuration register for pad: I2C3_SDA, GPIO2_13
- Offset: 0x18; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO2_13_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster

Bits	Field Name	Access	Description
			transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	I2C3_SDA_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.76 G3_PADCFG_008

- Description: Pad cell configuration register for pad: SPI_SCLK, SPI_CSN
- Offset: 0x1C; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	SPI_CSN_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core.

Bits	Field Name	Access	Description
			SL: Write 1 to enable slew rate control, to get a faster transition on pad ST: Write 1 to enable schmitt trigger, make input signal more regular SPU: Write 1 to enable internal strong pull-up resistor PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	SPI_SCLK_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: write 1 to enable slew rate control, to get a faster transition on pad. ST: write 1 to enable schmitt trigger, make input signal more regular. SPU: write 1 to enable internal strong pull-up resistor. PS: pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.77 G3_PADCFG_009

- Description: Pad cell configuration register for pad: SPI_MOSI, SPI_MISO
- Offset: 0x20; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	SPI_MISO_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to

Bits	Field Name	Access	Description
			enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	SPI_MOSI_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.78 G3_PADCFG_010

- Description: Pad cell configuration register for pad: GPIO2_18, GPIO2_19
- Offset: 0x24; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO2_19_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0}

Bits	Field Name	Access	Description
			IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO2_18_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.79 G3_PADCFG_011

- Description: Pad cell configuration register for pad: GPIO2_20, GPIO2_21
- Offset: 0x28; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	

Bits	Field Name	Access	Description
[25:16]	GPIO2_21_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO2_20_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.80 G3_PADCFG_012

- Description: Pad cell configuration register for pad: GPIO2_22, GPIO2_23
- Offset: 0x2C; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO2_23_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO2_22_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.81 G3_PADCFG_013

- Description: Pad cell configuration register for pad: GPIO2_24, GPIO2_25
- Offset: 0x30; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO2_25_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO2_24_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.82 G3_PADCFG_014

- Description: Pad cell configuration register for pad: SDIO0_WPRTN, SDIO0_DETN
- Offset: 0x34; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	SDIO0_DETN_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	SDIO0_WPRTN_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.83 G3_PADCFG_015

- Description: Pad cell configuration register for pad: SDIO1_WPRTN, SDIO1_DETN
- Offset: 0x38; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	SDIO1_DETN_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	SDIO1_WPRTN_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.84 G3_PADCFG_016

- Description: Pad cell configuration register for pad: GPIO2_30, GPIO2_31
- Offset: 0x3C; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO2_31_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO2_30_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.85 G3_PADCFG_017

- Description: Pad cell configuration register for pad: GPIO3_0, GPIO3_1
- Offset: 0x40; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO3_1_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO3_0_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.86 G3_PADCFG_018

- Description: Pad cell configuration register for pad: GPIO3_2, GPIO3_3
- Offset: 0x44; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GPIO3_3_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GPIO3_2_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.87 G3_PADCFG_019

- Description: Pad cell configuration register for pad: HDMI_SCL, HDMI_SDA
- Offset: 0x48; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	HDMI_SDA_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	HDMI_SCL_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.88 G3_PADCFG_020

- Description: Pad cell configuration register for pad: HDMI_CEC, GMAC0_TX_CLK
- Offset: 0x4C; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GMAC0_TX_CLK_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	HDMI_CEC_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.89 G3_PADCFG_021

- Description: Pad cell configuration register for pad: GMAC0_RX_CLK, GMAC0_TXEN
- Offset: 0x50; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GMAC0_TXEN_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GMAC0_RX_CLK_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.90 G3_PADCFG_022

- Description: Pad cell configuration register for pad: GMAC0_TXD0, GMAC0_TXD1
- Offset: 0x54; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GMAC0_TXD1_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GMAC0_TXD0_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.91 G3_PADCFG_023

- Description: Pad cell configuration register for pad: GMAC0_TXD2, GMAC0_TXD3
- Offset: 0x58; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GMAC0_TXD3_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GMAC0_TXD2_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.92 G3_PADCFG_024

- Description: Pad cell configuration register for pad: GMAC0_RXDV, GMAC0_RXD0
- Offset: 0x5C; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GMAC0_RXD0_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GMAC0_RXDV_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.93 G3_PADCFG_025

- Description: Pad cell configuration register for pad: GMAC0_RXD1, GMAC0_RXD2
- Offset: 0x60; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GMAC0_RXD2_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GMAC0_RXD1_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.94 G3_PADCFG_026

- Description: Pad cell configuration register for pad: GMAC0_RXD3, GMAC0_MDC
- Offset: 0x64; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GMAC0_MDC_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GMAC0_RXD3_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.95 G3_PADCFG_027

- Description: Pad cell configuration register for pad: GMAC0_MDIO, GMAC0_COL
- Offset: 0x68; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x2080208

Bits	Field Name	Access	Description
[31:26]	RESERVED_2	-	
[25:16]	GMAC0_COL_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208
[15:10]	RESERVED_1	-	
[9:0]	GMAC0_MDIO_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.96 G3_PADCFG_028

- Description: Pad cell configuration register for pad: GMAC0_CRS
- Offset: 0x6C; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x208

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9:0]	GMAC0_CRS_PAD_CFG	RW	{IE, SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} IE: Input enable, software should always write 1 to enable ext data input to the core. SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x208

3.3.4.97 G3_MUXCFG_001

- Description: MUX configuration register for pad: UART0_TXD, UART0_RXD, QSPI0_SCLK, QSPI0_CSN0, QSPI0_CSN1, QSPI0_D0_MOSI, QSPI0_D1_MISO, QSPI0_D2_WP
- Offset: 0x400; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	QSPI0_D2_WP_MUX_CFG	RW	MUX configuration for pad: QSPI0_D2_WP 0000: QSPI0_M2_WP 0001: PWM5 0010: I2S_SCLK 0011: GPIO2_7 Value After Reset: 0x0
[27:24]	QSPI0_D1_MISO_MUX_CFG	RW	MUX configuration for pad: QSPI0_D1_MISO 0000: QSPI0_M1_MISO 0001: PWM4 0010: I2S_MCLK 0011: GPIO2_6 Value After Reset: 0x0

Bits	Field Name	Access	Description
[23:20]	QSPI0_D0_MOSI_MUX_CFG	RW	MUX configuration for pad: QSPI0_D0_MOSI 0000: QSPI0_M0_MOSI 0001: PWM3 0010: I2S_SDA3 0011: GPIO2_5 Value After Reset: 0x0
[19:16]	QSPI0_CSN1_MUX_CFG	RW	MUX configuration for pad: QSPI0_CSN1 0000: QSPI0_SSN1 0001: PWM2 0010: I2S_SDA2 0011: GPIO2_4 Value After Reset: 0x0
[15:12]	QSPI0_CSN0_MUX_CFG	RW	MUX configuration for pad: QSPI0_CSN0 0000: QSPI0_SSN0 0001: PWM1 0010: I2S_SDA1 0011: GPIO2_3 Value After Reset: 0x0
[11:8]	QSPI0_SCLK_MUX_CFG	RW	MUX configuration for pad: QSPI0_SCLK 0000: QSPI0_SCLK 0001: PWM0 0010: I2S_SDA0 0011: GPIO2_2 Value After Reset: 0x0
[7:4]	UART0_RXD_MUX_CFG	RW	MUX configuration for pad: UART0_RXD 0000: UART0_RXD 0011: GPIO2_1 Value After Reset: 0x0
[3:0]	UART0_TXD_MUX_CFG	RW	MUX configuration for pad: UART0_TXD 0000: UART0_TXD 0011: GPIO2_0 Value After Reset: 0x0

3.3.4.98 G3_MUXCFG_002

- Description: MUX configuration register for pad: QSPI0_D3_HOLD, I2C2_SCL, I2C2_SDA, I2C3_SCL, I2C3_SDA, GPIO2_13, SPI_SCLK, SPI_CSN
- Offset: 0x404; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	SPI_CSN_MUX_CFG	RW	MUX configuration for pad: SPI_CSN 0000: SPI_SSN0 0001: UART2_RXD 0010: UART2_IR_IN 0011: GPIO2_15 Value After Reset: 0x0
[27:24]	SPI_SCLK_MUX_CFG	RW	MUX configuration for pad: SPI_SCLK 0000: SPI_SCLK 0001: UART2_TXD 0010: UART2_IR_OUT 0011: GPIO2_14 Value After Reset: 0x0
[23:20]	GPIO2_13_MUX_CFG	RW	MUX configuration for pad: GPIO2_13 0000: GPIO2_13 0001: SPI_SSN1 Value After Reset: 0x0
[19:16]	I2C3_SDA_MUX_CFG	RW	MUX configuration for pad: I2C3_SDA 0000: I2C3_SDA 0011: GPIO2_12 Value After Reset: 0x0
[15:12]	I2C3_SCL_MUX_CFG	RW	MUX configuration for pad: I2C3_SCL 0000: I2C3_SCL 0011: GPIO2_11 Value After Reset: 0x0
[11:8]	I2C2_SDA_MUX_CFG	RW	MUX configuration for pad: I2C2_SDA 0000: I2C2_SDA 0001: UART2_RXD 0011: GPIO2_10 Value After Reset: 0x0

Bits	Field Name	Access	Description
[7:4]	I2C2_SCL_MUX_CFG	RW	MUX configuration for pad: I2C2_SCL 0000: I2C2_SCL 0001: UART2_TXD 0011: GPIO2_9 Value After Reset: 0x0
[3:0]	QSPI0_D3_HOLD_MUX_CFG	RW	MUX configuration for pad: QSPI0_D3_HOLD 0000: QSPI0_M3_HOLD 0010: I2S_WS 0011: GPIO2_8 Value After Reset: 0x0

3.3.4.99 G3_MUXCFG_003

- Description: MUX configuration register for pad: SPI_MOSI, SPI_MISO, GPIO2_18, GPIO2_19, GPIO2_20, GPIO2_21, GPIO2_22, GPIO2_23
- Offset: 0x408; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	GPIO2_23_MUX_CFG	RW	MUX configuration for pad: GPIO2_23 0000: GPIO2_23 0001: GMAC1_TXD2 Value After Reset: 0x0
[27:24]	GPIO2_22_MUX_CFG	RW	MUX configuration for pad: GPIO2_22 0000: GPIO2_22 0001: GMAC1_TXD1 Value After Reset: 0x0
[23:20]	GPIO2_21_MUX_CFG	RW	MUX configuration for pad: GPIO2_21 0000: GPIO2_21 0001: GMAC1_TXD0 Value After Reset: 0x0
[19:16]	GPIO2_20_MUX_CFG	RW	MUX configuration for pad: GPIO2_20 0000: GPIO2_20 0001: GMAC1_TXEN Value After Reset: 0x0

Bits	Field Name	Access	Description
[15:12]	GPIO2_19_MUX_CFG	RW	MUX configuration for pad: GPIO2_19 0000: GPIO2_19 0001: GMAC1_RX_CLK Value After Reset: 0x0
[11:8]	GPIO2_18_MUX_CFG	RW	MUX configuration for pad: GPIO2_18 0000: GPIO2_18 0001: GMAC1_TX_CLK Value After Reset: 0x0
[7:4]	SPI_MISO_MUX_CFG	RW	MUX configuration for pad: SPI_MISO 0000: SPI_MISO 0011: GPIO2_17 Value After Reset: 0x0
[3:0]	SPI_MOSI_MUX_CFG	RW	MUX configuration for pad: SPI_MOSI 0000: SPI_MOSI 0011: GPIO2_16 Value After Reset: 0x0

3.3.4.100 G3_MUXCFG_004

- Description: MUX configuration register for pad: GPIO2_24, GPIO2_25, SDIO0_WPRTN, SDIO0_DETN, SDIO1_WPRTN, SDIO1_DETN, GPIO2_30, GPIO2_31
- Offset: 0x40C; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	GPIO2_31_MUX_CFG	RW	MUX configuration for pad: GPIO2_31 0000: GPIO2_31 0001: GMAC1_RXD1 Value After Reset: 0x0
[27:24]	GPIO2_30_MUX_CFG	RW	MUX configuration for pad: GPIO2_30 0000: GPIO2_30 0001: GMAC1_RXD0 Value After Reset: 0x0

Bits	Field Name	Access	Description
[23:20]	SDIO1_DETN_MUX_CFG	RW	MUX configuration for pad: SDIO1_DETN 0000: SDIO1_DETN 0011: GPIO2_29 Value After Reset: 0x0
[19:16]	SDIO1_WPRTN_MUX_CFG	RW	MUX configuration for pad: SDIO1_WPRTN 0000: SDIO1_WPRTN 0011: GPIO2_28 Value After Reset: 0x0
[15:12]	SDIO0_DETN_MUX_CFG	RW	MUX configuration for pad: SDIO0_DETN 0000: SDIO0_DETN 0011: GPIO2_27 Value After Reset: 0x0
[11:8]	SDIO0_WPRTN_MUX_CFG	RW	MUX configuration for pad: SDIO0_WPRTN 0000: SDIO0_WPRTN 0011: GPIO2_26 Value After Reset: 0x0
[7:4]	GPIO2_25_MUX_CFG	RW	MUX configuration for pad: GPIO2_25 0000: GPIO2_25 0001: GMAC1_RXDV Value After Reset: 0x0
[3:0]	GPIO2_24_MUX_CFG	RW	MUX configuration for pad: GPIO2_24 0000: GPIO2_24 0001: GMAC1_TXD3 Value After Reset: 0x0

3.3.4.101 G3_MUXCFG_005

- Description: MUX configuration register for pad: GPIO3_0, GPIO3_1, GPIO3_2, GPIO3_3, HDMI_SCL, HDMI_SDA, HDMI_CEC, GMAC0_TX_CLK
- Offset: 0x410; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	GMAC0_TX_CLK_MUX_CFG	RW	MUX configuration for pad: GMAC0_TX_CLK 0000: GMAC0_TX_CLK 0011: GPIO3_7

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[27:24]	HDMI_CEC_MUX_CFG	RW	MUX configuration for pad: HDMI_CEC 0000: HDMI_CEC 0011: GPIO3_6 Value After Reset: 0x0
[23:20]	HDMI_SDA_MUX_CFG	RW	MUX configuration for pad: HDMI_SDA 0000: HDMI_SDA 0001: PWM3 0011: GPIO3_5 Value After Reset: 0x0
[19:16]	HDMI_SCL_MUX_CFG	RW	MUX configuration for pad: HDMI_SCL 0000: HDMI_SCL 0001: PWM2 0011: GPIO3_4 Value After Reset: 0x0
[15:12]	GPIO3_3_MUX_CFG	RW	MUX configuration for pad: GPIO3_3 0000: GPIO3_3 0001: PWM1 Value After Reset: 0x0
[11:8]	GPIO3_2_MUX_CFG	RW	MUX configuration for pad: GPIO3_2 0000: GPIO3_2 0001: PWM0 Value After Reset: 0x0
[7:4]	GPIO3_1_MUX_CFG	RW	MUX configuration for pad: GPIO3_1 0000: GPIO3_1 0001: GMAC1_RXD3 Value After Reset: 0x0
[3:0]	GPIO3_0_MUX_CFG	RW	MUX configuration for pad: GPIO3_0 0000: GPIO3_0 0001: GMAC1_RXD2 Value After Reset: 0x0

3.3.4.102 G3_MUXCFG_006

- Description: MUX configuration register for pad: GMAC0_RX_CLK, GMAC0_TXEN, GMAC0_TXD0, GMAC0_TXD1, GMAC0_TXD2, GMAC0_TXD3, GMAC0_RXDV, GMAC0_RXD0
- Offset: 0x414; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	GMAC0_RXD0_MUX_CFG	RW	MUX configuration for pad: GMAC0_RXD0 0000: GMAC0_RXD0 0001: I2C3_SCL 0011: GPIO3_15 Value After Reset: 0x0
[27:24]	GMAC0_RXDV_MUX_CFG	RW	MUX configuration for pad: GMAC0_RXDV 0000: GMAC0_RXDV 0001: I2C2_SDA 0011: GPIO3_14 Value After Reset: 0x0
[23:20]	GMAC0_TXD3_MUX_CFG	RW	MUX configuration for pad: GMAC0_TXD3 0000: GMAC0_TXD3 0001: I2C2_SCL 0011: GPIO3_13 Value After Reset: 0x0
[19:16]	GMAC0_TXD2_MUX_CFG	RW	MUX configuration for pad: GMAC0_TXD2 0000: GMAC0_TXD2 0001: UART0_RXD 0011: GPIO3_12 Value After Reset: 0x0
[15:12]	GMAC0_TXD1_MUX_CFG	RW	MUX configuration for pad: GMAC0_TXD1 0000: GMAC0_TXD1 0001: UART0_TXD 0011: GPIO3_11 Value After Reset: 0x0

Bits	Field Name	Access	Description
[11:8]	GMAC0_TXD0_MUX_CFG	RW	MUX configuration for pad: GMAC0_TXD0 0000: GMAC0_TXD0 0001: UART2_RXD 0011: GPIO3_10 Value After Reset: 0x0
[7:4]	GMAC0_TXEN_MUX_CFG	RW	MUX configuration for pad: GMAC0_TXEN 0000: GMAC0_TXEN 0001: UART2_TXD 0011: GPIO3_9 Value After Reset: 0x0
[3:0]	GMAC0_RX_CLK_MUX_CFG	RW	MUX configuration for pad: GMAC0_RX_CLK 0000: GMAC0_RX_CLK 0011: GPIO3_8 Value After Reset: 0x0

3.3.4.103 G3_MUXCFG_007

- Description: MUX configuration register for pad: GMAC0_RXD1, GMAC0_RXD2, GMAC0_RXD3, GMAC0_MDC, GMAC0_MDIO, GMAC0_COL, GMAC0_CRS
- Offset: 0x418; Base Address: 0xBC007000 for E902, 0xFFEC007000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	RESERVED_1	-	
[27:24]	GMAC0_CRS_MUX_CFG	RW	MUX configuration for pad: GMAC0_CRS 0000: GMAC0_CRS 0001: PWM5 0011: GPIO3_22 Value After Reset: 0x0
[23:20]	GMAC0_COL_MUX_CFG	RW	MUX configuration for pad: GMAC0_COL 0000: GMAC0_COL 0001: PWM4 0011: GPIO3_21 Value After Reset: 0x0

Bits	Field Name	Access	Description
[19:16]	GMAC0_MDIO_MUX_CFG	RW	MUX configuration for pad: GMAC0_MDIO 0000: GMAC0_MDIO 0001: SPI_MISO 0010: GMAC1_MDIO 0011: GPIO3_20 Value After Reset: 0x0
[15:12]	GMAC0_MDC_MUX_CFG	RW	MUX configuration for pad: GMAC0_MDC 0000: GMAC0_MDC 0001: SPI_MOSI 0010: GMAC1_MDC 0011: GPIO3_19 Value After Reset: 0x0
[11:8]	GMAC0_RXD3_MUX_CFG	RW	MUX configuration for pad: GMAC0_RXD3 0000: GMAC0_RXD3 0001: SPI_SSN0 0011: GPIO3_18 Value After Reset: 0x0
[7:4]	GMAC0_RXD2_MUX_CFG	RW	MUX configuration for pad: GMAC0_RXD2 0000: GMAC0_RXD2 0001: SPI_SCLK 0011: GPIO3_17 Value After Reset: 0x0
[3:0]	GMAC0_RXD1_MUX_CFG	RW	MUX configuration for pad: GMAC0_RXD1 0000: GMAC0_RXD1 0001: I2C3_SDA 0011: GPIO3_16 Value After Reset: 0x0

3.3.4.104 AUDIO_IO_GPIO_SEL

- Description: AUDIO PAD mode configuration register
- Offset: 0x00; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	

Bits	Field Name	Access	Description
[30]	AUDIO_PA30_GPIO_SEL	RW	AUDIO_PA30 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in UDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[29]	AUDIO_PA29_GPIO_SEL	RW	AUDIO_PA29 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[28]	AUDIO_PA28_GPIO_SEL	RW	AUDIO_PA28 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in UDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[27]	AUDIO_PA27_GPIO_SEL	RW	AUDIO_PA27 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[26]	AUDIO_PA26_GPIO_SEL	RW	AUDIO_PA26 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[25]	AUDIO_PA25_GPIO_SEL	RW	AUDIO_PA25 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[24]	AUDIO_PA24_GPIO_SEL	RW	AUDIO_PA24 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0

Bits	Field Name	Access	Description
[23]	AUDIO_PA23_GPIO_SEL	RW	AUDIO_PA23 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[22]	AUDIO_PA22_GPIO_SEL	RW	AUDIO_PA22 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[21]	AUDIO_PA21_GPIO_SEL	RW	AUDIO_PA21 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[20]	AUDIO_PA20_GPIO_SEL	RW	AUDIO_PA20 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[19]	AUDIO_PA19_GPIO_SEL	RW	AUDIO_PA19 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[18]	AUDIO_PA18_GPIO_SEL	RW	AUDIO_PA18 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[17]	AUDIO_PA17_GPIO_SEL	RW	AUDIO_PA17 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0

Bits	Field Name	Access	Description
[16]	AUDIO_PA16_GPIO_SEL	RW	AUDIO_PA16 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[15]	AUDIO_PA15_GPIO_SEL	RW	AUDIO_PA15 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[14]	AUDIO_PA14_GPIO_SEL	RW	AUDIO_PA14 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[13]	AUDIO_PA13_GPIO_SEL	RW	AUDIO_PA13 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[12]	AUDIO_PA12_GPIO_SEL	RW	AUDIO_PA12 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[11]	AUDIO_PA11_GPIO_SEL	RW	AUDIO_PA11 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[10]	AUDIO_PA10_GPIO_SEL	RW	AUDIO_PA10 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0

Bits	Field Name	Access	Description
[9]	AUDIO_PA9_GPIO_SEL	RW	AUDIO_PA9 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[8]	AUDIO_PA8_GPIO_SEL	RW	AUDIO_PA8 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[7]	AUDIO_PA7_GPIO_SEL	RW	AUDIO_PA7 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[6]	AUDIO_PA6_GPIO_SEL	RW	AUDIO_PA6 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[5]	AUDIO_PA5_GPIO_SEL	RW	AUDIO_PA5 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[4]	AUDIO_PA4_GPIO_SEL	RW	AUDIO_PA4 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[3]	AUDIO_PA3_GPIO_SEL	RW	AUDIO_PA3 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0

Bits	Field Name	Access	Description
[2]	AUDIO_PA2_GPIO_SEL	RW	AUDIO_PA2 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[1]	AUDIO_PA1_GPIO_SEL	RW	AUDIO_PA1 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0
[0]	AUDIO_PA0_GPIO_SEL	RW	AUDIO_PA0 GPIO or hardware mode selection 0: GPIO mode, controlled by GPIO in AUDIO_SUBSYS 1: Hardware mode, controlled by other modules in AUDIO_SUBSYS Value After Reset: 0x0

3.3.4.105 AUDIO_IO_MUXCFG_001

- Description: AUDIO PAD Alternative function mode selection register
- Offset: 0x4; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:30]	AUDIO_PA15_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S1_BCLK 01: VAD_PDM_DIN1 10: VAD_DIN1 11: CLK_12M Value After Reset: 0x0
[29:28]	AUDIO_PA14_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S1_WSCLK 01: VAD_PDM_DIN0 10: VAD_DIN0 11: I2S0_WSCLK Value After Reset: 0x0

Bits	Field Name	Access	Description
[27:26]	AUDIO_PA13_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S1_MCLK 01: I2C1_DATA 10: VAD_MCLK 11: UART_RX Value After Reset: 0x0
[25:24]	AUDIO_PA12_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S0_MCLK 01: I2C1_CLK 10: UART_TX 11: I2S1_DOUT Value After Reset: 0x0
[23:22]	AUDIO_PA11_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S0_SDA 01: T_AUDIO_CLK 10: TDM_WSCLK 11: I2S1_DIN Value After Reset: 0x0
[21:20]	AUDIO_PA10_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S0_BCLK 01: T_UART_CLK 10: TDM_BCLK 11: I2S1_BCLK Value After Reset: 0x0
[19:18]	AUDIO_PA9_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S0_WSCLK 01: T_APB_CLK 10: TDM_DAT 11: I2S1_WSCLK Value After Reset: 0x0

Bits	Field Name	Access	Description
[17:16]	AUDIO_PA8_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: CLK_12M 01: T_AHB_CLK 10: VAD_MCLK 11: I2S_8CH_MCLK Value After Reset: 0x0
[15:14]	AUDIO_PA7_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2C0_DATA 01: T_AXI_CLK 10: I2C1_DATA 11: UART_TX Value After Reset: 0x0
[13:12]	AUDIO_PA6_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2C0_CLK 01: T_CPU_CLK 10: I2C1_CLK 11: UART_RX Value After Reset: 0x0
[11:10]	AUDIO_PA5_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: VAD_DIN3 01: VAD_PDM_DIN3 10: UART_TX 11: I2S_8CH_SDA1 Value After Reset: 0x0
[9:8]	AUDIO_PA4_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: VAD_DIN2 01: VAD_PDM_DIN2 10: UART_RX 11: I2S_8CH_SDA0 Value After Reset: 0x0

Bits	Field Name	Access	Description
[7:6]	AUDIO_PA3_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: VAD_SCLK 01: VAD_PDM_CLK 10: SPDIF1_DIN 11: I2S_8CH_BCLK Value After Reset: 0x0
[5:4]	AUDIO_PA2_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: VAD_WS 10: SPDIF1_DOUT 11: I2S_8CH_WSCLK Value After Reset: 0x0
[3:2]	AUDIO_PA1_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: VAD_DIN1 01: VAD_PDM_DIN1 10: SPDIF0_DIN 11: I2S_8CH_SDA3 Value After Reset: 0x0
[1:0]	AUDIO_PA0_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: VAD_DIN0 01: VAD_PDM_DIN0 10: SPDIF0_DOUT 11: I2S_8CH_SDA2 Value After Reset: 0x0

3.3.4.106 AUDIO_IO_MUXCFG_002

- Description: AUDIO PAD alternative function mode selection register
- Offset: 0x08; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:30]	RESERVED_1	-	

Bits	Field Name	Access	Description
[29:28]	AUDIO_PA30_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S_8CH_SDA1 10: I2C0_DATA 11: I2S0_MCLK Value After Reset: 0x0
[27:26]	AUDIO_PA29_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S_8CH_SDA0 01: TDM_DAT 10: I2C0_CLK 11: I2S0_SDA Value After Reset: 0x0
[25:24]	AUDIO_PA28_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S_8CH_BCLK 01: TDM_BCLK 10: SPDIF1_DOUT 11: I2S0_BCLK Value After Reset: 0x0
[23:22]	AUDIO_PA27_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S_8CH_WSCLK 01: TDM_WSCLK 10: SPDIF1_DIN 11: I2S0_WSCLK Value After Reset: 0x0
[21:20]	AUDIO_PA26_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S_8CH_SDA3 01: UART_CTS 10: SPDIF0_DOUT 11: I2C1_CLK Value After Reset: 0x0

Bits	Field Name	Access	Description
[19:18]	AUDIO_PA25_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S_8CH_SDA2 01: UART_RTS 10: SPDIF0_DIN 11: I2C1_DATA Value After Reset: 0x0
[17:16]	AUDIO_PA24_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: UART_RX 01: SPDIF1_DIN 10: SPDIF0_DIN 11: I2S_8CH_MCLK Value After Reset: 0x0
[15:14]	AUDIO_PA23_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: UART_TX 01: SPDIF1_DOUT 10: SPDIF0_DOUT Value After Reset: 0x0
[13:12]	AUDIO_PA22_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S2_DOUT 01: SPDIF0_DOUT 10: CLK_12M Value After Reset: 0x0
[11:10]	AUDIO_PA21_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S2_DIN 01: SPDIF0_DIN 10: I2C1_DATA 11: I2C1_CLK Value After Reset: 0x0
[9:8]	AUDIO_PA20_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S2_MCLK 01: TDM_WSCLK 10: I2C1_CLK 11: I2C1_DATA Value After Reset: 0x0

Bits	Field Name	Access	Description
[7:6]	AUDIO_PA19_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S2_BCLK 01: TDM_BCLK 10: VAD_DIN3 11: UART_RTS Value After Reset: 0x0
[5:4]	AUDIO_PA18_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S2_WSCLK 01: TDM_DAT 10: VAD_DIN2 11: UART_CTS Value After Reset: 0x0
[3:2]	AUDIO_PA17_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S1_DOUT 01: VAD_PDM_DIN2 10: VAD_SCLK 11: I2C1_DATA Value After Reset: 0x0
[1:0]	AUDIO_PA16_AF_SEL	RW	AUDIO_PA15 alternative function mode selection 00: I2S1_DIN 01: VAD_PDM_CLK 10: VAD_WS 11: I2C1_CLK Value After Reset: 0x0

3.3.4.107 AUDIO_IO_PADCFG_001

- Description: PAD cell configuration register for AUDIO_PA0 and AUDIO_PA1. Only valid when PAD in AUDIO_SUBSYS function mode.
- Offset: 0x0C; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:25]	RESERVED_1	-	
[24:16]	AUDIO_PA1_PAD_CFG_SUB	RW	AUDIO_PA1 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS

Bits	Field Name	Access	Description
			function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0
[15:0]	AUDIO_PA0_PAD_CFG_SUB	RW	AUDIO_PA0 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

3.3.4.108 AUDIO_IO_PADCFG_002

- Description: PAD cell configuration register for AUDIO_PA2 and AUDIO_PA3. Only valid when PAD in AUDIO_SUBSYS function mode.
- Offset: 0x10; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:25]	RESERVED_1	-	

Bits	Field Name	Access	Description
[24:16]	AUDIO_PA3_PAD_CFG_SUB	RW	AUDIO_PA3 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0
[15:0]	AUDIO_PA2_PAD_CFG_SUB	RW	AUDIO_PA2 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

3.3.4.109 AUDIO_IO_PADCFG_003

- Description: PAD cell configuration register for AUDIO_PA4 and AUDIO_PA5. Only valid when PAD in AUDIO_SUBSYS function mode.
- Offset: 0x14; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:25]	RESERVED_1	-	
[24:16]	AUDIO_PA5_PAD_CFG_SUB	RW	AUDIO_PA5 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0
[15:0]	AUDIO_PA4_PAD_CFG_SUB	RW	AUDIO_PA4 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

3.3.4.110 AUDIO_IO_PADCFG_004

- Description: PAD cell configuration register for AUDIO_PA6 and AUDIO_PA7. Only valid when PAD in AUDIO_SUBSYS function mode.
- Offset: 0x18; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:25]	RESERVED_1	-	
[24:16]	AUDIO_PA7_PAD_CFG_SUB	RW	AUDIO_PA7 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0
[15:0]	AUDIO_PA6_PAD_CFG_SUB	RW	AUDIO_PA6 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

3.3.4.111 AUDIO_IO_PADCFG_005

- Description: PAD cell configuration register for AUDIO_PA8 and AUDIO_PA9. Only valid when PAD in AUDIO_SUBSYS function mode.

- Offset: 0x1C; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:25]	RESERVED_1	-	
[24:16]	AUDIO_PA9_PAD_CFG_SUB	RW	AUDIO_PA9 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0
[15:0]	AUDIO_PA8_PAD_CFG_SUB	RW	AUDIO_PA8 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

3.3.4.112 AUDIO_IO_PADCFG_006

- Description: PAD cell configuration register for AUDIO_PA10 and AUDIO_PA11. Only valid when PAD in AUDIO_SUBSYS function mode.
- Offset: 0x20; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:25]	RESERVED_1	-	
[24:16]	AUDIO_PA11_PAD_CFG_SUB	RW	AUDIO_PA11 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0
[15:0]	AUDIO_PA10_PAD_CFG_SUB	RW	AUDIO_PA10 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

3.3.4.113 AUDIO_IO_PADCFG_007

- Description: PAD cell configuration register for AUDIO_PA12 and AUDIO_PA13. Only valid when PAD in AUDIO_SUBSYS function mode.
- Offset: 0x24; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:25]	RESERVED_1	-	
[24:16]	AUDIO_PA13_PAD_CFG_SUB	RW	AUDIO_PA13 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0
[15:0]	AUDIO_PA12_PAD_CFG_SUB	RW	AUDIO_PA12 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

3.3.4.114 AUDIO_IO_PADCFG_008

- Description: PAD cell configuration register for AUDIO_PA14 and AUDIO_PA15. Only valid when PAD in AUDIO_SUBSYS function mode.
- Offset: 0x28; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:25]	RESERVED_1	-	
[24:16]	AUDIO_PA15_PAD_CFG_SUB	RW	AUDIO_PA15 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0
[15:0]	AUDIO_PA14_PAD_CFG_SUB	RW	AUDIO_PA14 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

3.3.4.115 AUDIO_IO_PADCFG_009

- Description: PAD cell configuration register for AUDIO_PA16 and AUDIO_PA17. Only valid when PAD in AUDIO_SUBSYS function mode.
- Offset: 0x2C; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:25]	RESERVED_1	-	
[24:16]	AUDIO_PA17_PAD_CFG_SUB	RW	AUDIO_PA17 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0
[15:0]	AUDIO_PA16_PAD_CFG_SUB	RW	AUDIO_PA16 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

3.3.4.116 AUDIO_IO_PADCFG_010

- Description: PAD cell configuration register for AUDIO_PA18 and AUDIO_PA19. Only valid when PAD in AUDIO_SUBSYS function mode.
- Offset: 0x30; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:25]	RESERVED_1	-	
[24:16]	AUDIO_PA19_PAD_CFG_SUB	RW	AUDIO_PA19 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0
[15:0]	AUDIO_PA18_PAD_CFG_SUB	RW	AUDIO_PA18 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

3.3.4.117 AUDIO_IO_PADCFG_011

- Description: PAD cell configuration register for AUDIO_PA20 and AUDIO_PA21. Only valid when PAD in AUDIO_SUBSYS function mode.
- Offset: 0x34; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:25]	RESERVED_1	-	
[24:16]	AUDIO_PA21_PAD_CFG_SUB	RW	AUDIO_PA21 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0
[15:0]	AUDIO_PA20_PAD_CFG_SUB	RW	AUDIO_PA20 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

3.3.4.118 AUDIO_IO_PADCFG_012

- Description: PAD cell configuration register for AUDIO_PA22 and AUDIO_PA23. Only valid when PAD in AUDIO_SUBSYS function mode.
- Offset: 0x38; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:25]	RESERVED_1	-	
[24:16]	AUDIO_PA23_PAD_CFG_SUB	RW	AUDIO_PA23 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0
[15:0]	AUDIO_PA22_PAD_CFG_SUB	RW	AUDIO_PA22 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

3.3.4.119 AUDIO_IO_PADCFG_013

- Description: PAD cell configuration register for AUDIO_PA24 and AUDIO_PA25. Only valid when PAD in AUDIO_SUBSYS function mode.
- Offset: 0x3C; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:25]	RESERVED_1	-	
[24:16]	AUDIO_PA25_PAD_CFG_SUB	RW	AUDIO_PA25 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0
[15:0]	AUDIO_PA24_PAD_CFG_SUB	RW	AUDIO_PA24 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

3.3.4.120 AUDIO_IO_PADCFG_014

- Description: PAD cell configuration register for AUDIO_PA26 and AUDIO_PA27. Only valid when PAD in AUDIO_SUBSYS function mode.
- Offset: 0x40; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:25]	RESERVED_1	-	
[24:16]	AUDIO_PA27_PAD_CFG_SUB	RW	AUDIO_PA27 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0
[15:0]	AUDIO_PA26_PAD_CFG_SUB	RW	AUDIO_PA26 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

3.3.4.121 AUDIO_IO_PADCFG_015

- Description: PAD cell configuration register for AUDIO_PA28 and AUDIO_PA29. Only valid when PAD in AUDIO_SUBSYS function mode.
- Offset: 0x44; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:25]	RESERVED_1	-	
[24:16]	AUDIO_PA29_PAD_CFG_SUB	RW	AUDIO_PA29 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0
[15:0]	AUDIO_PA28_PAD_CFG_SUB	RW	AUDIO_PA28 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

3.3.4.122 AUDIO_IO_PADCFG_016

- Description: PAD cell configuration register for AUDIO_PA30. Only valid when PAD in AUDIO_SUBSYS function mode.
- Offset: 0x48; Base Address: 0xCB01D000 for E902, 0xFFCB01D000 for C906 and C910
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	AUDIO_PA30_PAD_CFG_SUB	RW	AUDIO_PA30 pad configuration register. Only valid when current PAD is configured in AUDIO_SUBSYS function mode. {SL, ST, SPU, PS, PE, DS3, DS2, DS1, DS0} SL: Write 1 to enable slew rate control, to get a faster transition on pad. ST: Write 1 to enable schmitt trigger, make input signal more regular. SPU: Write 1 to enable internal strong pull-up resistor. PS: Pull down/pull up select, 1 for pull-up, 0 for pull-down. PE: Pull up/down enable, write 1 to enable pull up/down, use PS to select pull-up or pull-down. DS[3:0]: Driver strength, larger driver strength provides good performance but more power consumption. Value After Reset: 0x0

4 Clock

4.1 Overview

The clock management module is used to manage chip clock input, clock generation and clock control, including:

- Management and control of clock input
- Clock frequency division and control
- Generating working clocks for each module

4.2 Main Features

- Support external crystal oscillator 24MHz input, external crystal oscillator 32.768KHz input, and built-in 24~26MHz RC.
- Support clock frequency division, clock switch, and clock gate.

4.3 Function Description

4.3.1 Clock Source

4.3.1.1 XTAL0 (24MHz)

The passive crystal oscillator clock, 24MHz, provides a reference clock for PLL.

4.3.1.2 XTAL1 (32.768KHz)

The passive crystal oscillator clock, 32.768KHz, provides a reference clock for RTC.

4.3.1.3 RC (24MHz~26MHz)

The internal crystal oscillator clock, 24MHz, provides clocks for AON_SUBSYS and TEE_SUBSYS.

4.3.2 PLL Resources

Figure & Table 4-1 PLL resources table

PLL Type	Parameter	Value
DDR_PLL	FOUTPOSTDIV clock output range	200~1067MHz. The default is 798MHz.
	Reference clock	24MHz
	Max Lock time (default configuration)	~21250ns
	Max Callock time (default configuration)	~906667ns

PLL Type	Parameter	Value
CPU_PLL0	FOUTPOSTDIV clock output range	100~2000MHz
	Reference clock	24MHz
	Max Lock time (default configuration)	~21250ns
	Max callock time (default configuration)	~906667ns
CPU_PLL1	FOUTPOSTDIV clock output range	100~2000MHz
	Reference clock	24MHz
	Maximum lock time (default configuration)	~21250ns
	Maximum Callock time (default configuration)	~906667ns
VIDEO_PLL	FOUTVCO clock output range	2376MHz (fixed)
	FOUTPOSTDIV clock output range	792MHz (fixed)
	Reference clock	24MHz
	Maximum lock time (default configuration)	~21250ns
	Maximum callock time (default configuration)	~906667ns
GMAC_PLL	FOUTPOSTDIV clock output range	1000MHz (fixed)
	Reference clock	24MHz
	Maximum Lock time (default configuration)	~21250ns
	Maximum Callock time (default configuration)	~906667ns
AUDIO_PLL	FOUTVCO clock output range	884.736MHz/2064.384MHz
	FOUTPOSTDIV clock output range	294.912MHz
	Reference clock	24MHz
	Max Lock time (default configuration)	~21250ns
	Max Callock time (default configuration)	~906667ns
SYS_PLL	FOUTVCO Clock output range	884.736MHz/2438.554MHz
	FOUTPOSTDIV clock output range	294.912MHz/812.8512MHz
	Reference clock	24MHz
	Maximum lock time (default configuration)	~21250ns
	Maximum callock time (default configuration)	~906667ns
DPU_PLL0	FOUTPOSTDIV clock output range	40MHz~594MHz
	Reference clock	24MHz

PLL Type	Parameter	Value
	Maximum lock time (default configuration)	~21250ns
	Maximum callock time (default configuration)	~906667ns
DPU_PLL1	FOUTPOSTDIV clock output range	40MHz~297MHz
	Reference clock	24MHz
	Maximum lock time (default configuration)	~21250ns
	Maximum callock time (default configuration)	~906667ns
TEE_PLL	FOUTPOSTDIV clock output range	792MHz (fixed)
	Reference clock	24MHz~26MHz
	Maximum lock time (default configuration)	~21250ns
	Maximum callock time (default configuration)	~906667ns

Details of each PLL are as follows:

4.3.2.1 CPU_PLL0

Silicon Creations Integer PLL, integer PLL, a clock used for C910 frequency division. The maximum output of FOUTPOSTDIV clock is 2000MHz and the default is 300MHz. CPU_PLL0 frequency is adjustable.

4.3.2.2 CPU_PLL1

Silicon Creations Integer PLL, integer PLL, a clock used for C910 frequency division. FOUTVCO clock is not used. The maximum output of FOUTPOSTDIV clock is 2000MHz and the default is 300MHz. CPU_PLL1 frequency is adjustable.

4.3.2.3 VIDEO_PLL

Silicon Creations Sigma-Delta PLL, integer PLL, used for frequency division to get system bus clock and VIDEO_SUBSYS clock. The maximum output of FOUTPOSTDIV clock is 792MHz and the default is 792MHz. The maximum output of FOUTVCO clock is 2376MHz and the default is 2376MHz. The maximum output of FOUTPH0 clock is 396MHz and the default is 396MHz. VIDEO_PLL frequency is fixed.

4.3.2.4 GMAC_PLL

Silicon Creations Sigma-Delta PLL, integer PLL, used for frequency division to get GMAC interface clock, system bus clock and peripheral clock. The maximum output of FOUTPOSTDIV clock is 1000MHz and the default is 1000MHz. The maximum output of FOUTPH0 clock is 500MHz and the

default is 500MHz. The maximum output of FOUT4 clock is 125MHz and the default is 125MHz. GMAC_PLL frequency is fixed.

4.3.2.5 AUDIO_PLL

Silicon Creations Sigma-Delta PLL, fractional PLL, used for frequency division to get AUDIO module sample clock and AON_SUBSYS working clock. The maximum output of FOUTPOSTDIV clock is 294.912MHz and the default is 288MHz. The maximum output of FOUTVCO clock is 2064.384MHz and the default is 864MHz. The maximum output of FOUT3 clock is 49.152MHz and the default is 48MHz. AUDIO_PLL frequency is adjustable.

AUDIO_PLL is mainly used to provide 8kHz/16kHz/24kHz/32kHz/48kHz/64kHz/96kHz/192kHz/384kHz sample source clocks to AUDIO module, and provide working clock to AON_SUBSYS. AUDIO_PLL is integer frequency division by default. AUDIO_PLL_FOUTVCO clock output is 864MHz, which is automatically calibrated by hardware on startup. The calibrated value will be locked. AUDIO_PLL_FOUTVCO needs to switch to 884.736MHz using software in the Bootloader stage. Since PFD and FBDIV are not changed, there is no need to calibrate again. The maximum output of AUDIO_PLL_FOUTVCO clock can be 2064.384MHz for facilitating expansion. It is not recommended to change 884.736MHz configuration using software except in special cases.

4.3.2.6 SYS_PLL

Silicon Creations Sigma-Delta PLL, fractional PLL, used for frequency division to get AUDIO module sample clock and system bus clock. The maximum output of FOUTPOSTDIV clock is 812.8512MHz and the default is 808MHz. The maximum output of FOUTVCO clock is 2438.5536MHz and the default is 2424MHz. SYS_PLL frequency is adjustable.

SYS_PLL is mainly used to provide 11.025kHz/22.05kHz/44.1kHz/88.2kHz sample source clocks to AUDIO module, and provide working clocks to C906, AUDIO_SUBSYS bus and 1.5MB share SRAM.

SYS_PLL is integer frequency division by default. SYS_PLL_FOUTVCO clock output is 2424MHz, which is automatically calibrated by hardware on startup. The calibrated value will be locked. SYS_PLL_FOUTVCO needs to switch to 2438.5536MHz using software in the Bootloader stage. Since PFD and FBDIV are not changed, there is no need to calibrate again.

The maximum output of SYS_PLL_FOUTVCO clock is 2438.5536MHz. At this frequency, C906 and 1.5M share SRAM can work at 812.8512MHz/609.6384MHz/487.7107MHz/406.4256MHz/304.8192MHz/203.2128MHz/162.5702MHz. If the frequencies above cannot meet demands, such as overclocking, SYS_PLL configuration can be modified using software.

NOTE

- SYS_PLL_FOUTVCO should be frequency multiplication of 135.4752MHz.
- If PFD and FBDIV are changed, it needs to calibrate PLL again.

4.3.2.7 DPU_PLL0

Silicon Creations Sigma-Delta PLL, integer PLL, used for frequency division to get VIDEO module DPU0 pixel clock. The maximum output of FOUTPOSTDIV clock is 1188MHz and the default is 1188MHz. DPU_PLL0 frequency is adjustable.

4.3.2.8 DPU_PLL1

Silicon Creations Sigma-Delta PLL, integer PLL, used for frequency division to get VIDEO module DPU1 pixel clock. The maximum output of FOUTPOSTDIV clock output is 1188MHz and the default is 1188MHz. DPU_PLL1 frequency is adjustable.

4.3.2.9 TEE_PLL

Silicon Creations Sigma-Delta PLL, integer PLL, used for frequency division to get TEE_SUBSYS working clock. The reference clock is RC_CLK, whose frequency range is 24MHz~26MHz before calibration. It is required to calibrate RC_CLK before using TEE_PLL. FOUTVCO is not used. When RC_CLK frequency is 24MHz, the maximum output of FOUTPOSTDIV clock is 792MHz. TEE_PLL frequency is fixed.

4.3.3 Recommended PLL Configuration

The recommended PLL configuration in this project is shown in Figure & Table 4-2. The one marked in red is the default configuration.

Figure & Table 4-2 Recommended PLL configuration

PLL	DACPD	DSMPD	REFDIV	FREF	FPFD	FVCO (MHz)	FBDIV	FRAC	POSTDIV1	POSTDIV2	FOUTPOST (MHz)
DDR_PLL	1	1	1	24	24	3192	133	0	4	1	798
DDR_PLL	1	1	1	24	24	3192	133	0	6	1	532
DDR_PLL	1	1	1	24	24	2112	88	0	2	1	1056
CPU_PLL	1	1	1	24	24	3000	125	0	6	4	125
CPU_PLL	1	1	1	24	24	3000	125	0	5	3	200
CPU_PLL	1	1	1	24	24	3000	125	0	5	2	300
CPU_PLL	1	1	1	24	24	2400	100	0	3	2	400
CPU_PLL	1	1	1	24	24	3000	125	0	6	1	500
CPU_PLL	1	1	1	24	24	3000	125	0	5	1	600
CPU_PLL	1	1	1	24	24	2808	117	0	4	1	702
CPU_PLL	1	1	1	24	24	2400	100	0	3	1	800
CPU_PLL	1	1	1	24	24	1800	75	0	2	1	900
CPU_PLL	1	1	1	24	24	3000	125	0	3	1	1000
CPU_PLL	1	1	1	24	24	2208	92	0	2	1	1104
CPU_PLL	1	1	1	24	24	2400	100	0	2	1	1200

PLL	DACPD	DSMPD	REFDIV	FREF	FPFD	FVCO (MHz)	FBDIV	FRAC	POSTDIV1	POSTDIV2	FOUTPOST (MHz)
CPU_PLL	1	1	1	24	24	2592	108	0	2	1	1296
CPU_PLL	1	1	1	24	24	2808	117	0	2	1	1404
CPU_PLL	1	1	1	24	24	3000	125	0	2	1	1500
CPU_PLL	1	1	1	24	24	1608	67	0	1	1	1608
CPU_PLL	1	1	1	24	24	1704	71	0	1	1	1704
CPU_PLL	1	1	1	24	24	1800	75	0	1	1	1800
CPU_PLL	1	1	1	24	24	1896	79	0	1	1	1896
CPU_PLL	1	1	1	24	24	1992	83	0	1	1	1992
CPU_PLL	1	1	1	24	24	2112	88	0	1	1	2112
CPU_PLL	1	1	1	24	24	2208	92	0	1	1	2208
CPU_PLL	1	1	1	24	24	2304	96	0	1	1	2304
CPU_PLL	1	1	1	24	24	2400	100	0	1	1	2400
VIDEO_PLL	1	1	1	24	24	2376	99	0	3	1	792
GMAC_PLL	1	1	1	24	24	3000	125	0	3	1	1000
AUDIO_PLL	0	0	1	24	24	884.736	36	14495600	3	1	294.912
AUDIO_PLL	0	0	1	24	24	2064.384	86	268500	7	1	294.912
AUDIO_PLL	1	1	1	24	24	864	36	0	3	1	288
SYS_PLL	0	0	1	24	24	2438.5536	101	10173704	6	3	135.4752
SYS_PLL	1	1	1	24	24	2424	101	0	6	3	134.667
SYS_PLL	0	0	1	24	24	884.736	36	14495600	3	1	294.912
DPU_PLL	1	1	1	24	24	2376	99	0	2	1	1188
TEE_PLL	1	1	1	24	24	2376	99	0	3	1	792

4.3.4 Clock Frequency of Key Module

Descriptions of clocks generated in the chip are shown in Figure & Table 4-3.

Figure & Table 4-3 Clock generation

Clock	Description	Default Frequency (MHz)	Maximum Frequency (MHz)
osc clk	Crystal oscillator clock	24	24
rtc clk	RTC count source clock	0.32768	0.32768
rc clk	RC clock	-	24 (after calibration)

Clock	Description	Default Frequency (MHz)	Maximum Frequency (MHz)
aon clk	Working clock of AON_SUBSYS bus and its submodules, which is got through frequency division of source clock AUDIO PLL FOUTPOSTDIV, PAD OSC CLK or RC CLK.	72	73.728
share sram clk	1.5M SRAM core clock and DSP_SUBSYS AXI bus slave interface clock, which is got through frequency division of source clock SYS PLL FOUTVCO or AUDIO PLL FOUTVCO.	808	812.8512
audio aclk	AUDIO_SUBSYS AXI bus clock and 1.5M SRAM AXI bus Port4 interface clock, which is got through frequency division of source clock SYS PLL FOUTVCO or AUDIO PLL FOUTVCO.	808	812.8512
audio i2s clk	AUDIO SUBSYS I2S sample source clock, source clock AUDIO PLL FOUTPOSTDIV or AUDIO PLL FOUT3.	288	294.912
c906 clk	Working clock of AUDIO SUBSYS C906, which is got through frequency division of source clock SYS PLL FOUTVCO or AUDIO PLL FOUTVCO.	808	812.8512
aon i2c clk	AON SUBSYS I2C sample source clock, source clock AUDIO PLL FOUT3 or PAD OSC CLK.	24	49.152
cpusys hclk	AP SUBSYS AHB2 CPUSYS bus clock, which is got through frequency division of source clock GMAC PLL FOUT1PH0.	125	250
cpusys pclk	AP SUBSYS APB3 CPUSYS bus clock, which is got through frequency division of AHB2 CPUSYS HCLK.	125	125
cpusys2 aclk	AP SUBSYS AXI4 CPUSYS2 bus clock, which is got through frequency division of source clock GMAC PLL FOUTPOSTDIV.	500	500
c910 clk	Working clock of AP SUBSYS C910, source clock CPU PLL0 FOUTPOSTDIV, CPU PLL1 FOUTPOSTDIV or PAD OSC CLK.	300	1500MHz @ SSG 0.9V M40/0/125
cpusys1 aclk	AP SUBSYS AXI4 CPUSYS1 bus clock, which is got through frequency division of C910 CCLK.	150	750
ap axi aclk	AP SUBSYS CFG AXI bus clock, which is got through frequency division of source clock VIDEO PLL FOUTPOSTDIV, or PAD OSC CLK.	396	396
teesys hclk	TEE SUBSYS submodule AHB and AXI interface clock, which is got through frequency division of source clock VIDEO PLL FOUTPOSTDIV or TEE PLL FOUTPOSTDIV.	198	396

Clock	Description	Default Frequency (MHz)	Maximum Frequency (MHz)
teesys pclk	TEE SUBSYS APB clock, which is 4 frequency division of source clock TEESYS HCLK.	49.5	99
perisys ahb hclk	PERI SUBSYS AHB bus and submodule clock, which is got through frequency division of source clock GMAC PLL FOUT1PH0, or PAD OSC CLK.	62.5	250
perisys apb pclk	PERI SUBSYS APB bus and submodule clock, which is got through frequency division of PERISYS AHB HCLK.	62.5	62.5
peri2sys apb pclk	PERI2 SUBSYS APB bus and submodule clock, which is got through frequency division of source clock GMAC PLL FOUT4.	62.5	62.5
qspi0 clk	QSPI0 sample source clock, which is got through frequency division of source clock VIDEO PLL FOUTPOSTDIV, or PAD OSC CLK.	792	792
qspi1 clk	QSPI1 sample source clock, which is got through frequency division of source clock VIDEO PLL FOUT1PH0.	396	396
spi clk	SPI sample source clock, which is got through frequency division of source clock VIDEO PLL FOUT1PH0.	396	396
sensor clk1	External sensor clock 0, which is got through frequency division of source clock PAD OSC CLK.	24	24
sensor clk2	External sensor clock 1, which is got through frequency division of source clock PAD OSC CLK.	24	24
sensor clk3	External sensor clock 2, which is got through frequency division of source clock PAD OSC CLK.	24	24
sensor clk4	External sensor clock 3, which is got through frequency division of source clock PAD OSC CLK.	24	24
gmac cclk	GMAC sample source clock, source clock GMAC PLL FOUT1PH0.	500	500
peri i2s clk	PERI SUBSYS I2S sample source clock, source clock AUDIO PLL FOUTPOSTDIV or SYS PLL FOUTPOSTDIV.	288	294.912
vosys aclk	VO SUBSYS AXI bus master interface clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO.	792	792
npu cclk	NPU working clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO, or GMAC PLL FOUTPOSTDIV.	1000	1000

Clock	Description	Default Frequency (MHz)	Maximum Frequency (MHz)
cfg apb pclk	CFG APB bus clock, which is got through frequency division of source clock GMAC PLL FOUTPOSTDIV, or PAD OSC CLK.	250	250
visys m	VI SUBSYS AXI bus master interface clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO.	792	792
visys hclk	VI SUBSYS AHB bus clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO.	396	396
vpsys pclk	VP SUBSYS APB bus clock, which is got through frequency division of source clock GMAC PLL FOUT1PH0.	250	250
vpsys aclk	VP SUBSYS AXI bus clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO.	79	79
venc cclk	Video encoder working clock, which is got through frequency division of source clock GMAC PLL FOUTPOSTDIV.	500	500
uart sclk	UART baud rate generation source clock, which is got through frequency division of source clock GMAC PLL FOUTPOSTDIV, or PAD OSC CLK.	100	100
i2c ic clk	I2C sample source clock, which is got through frequency division of source clock GMAC PLL FOUTPOSTDIV.	50	50
emmc sdio ref clk	eMMC/SDIO sample source clock, which is got through frequency division of source clock VIDEO PLL FOUTPOSTDIV.	792	792
vdec cclk	VP SUBSYS VDEC working clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO.	594	594
g2d cclk	VP SUBSYS G2D working clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO.	792	792
fce cclk	VP SUBSYS FCE working clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO.	792	792
mipi csi0 pixelclk	VI SUBSYS MIPI CSI0 pixel clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO.	792	792
dw200 clk vse	VI SUBSYS DW200 VSE clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO.	792	792
dw200 clk dwe	VI SUBSYS DW200 DWE clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO.	792	792

Clock	Description	Default Frequency (MHz)	Maximum Frequency (MHz)
isp0 clk	VI SUBSYS ISP0 working clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO.	396	396
isp1_clk	VI SUBSYS ISP1 working clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO.	396	396
isp_ry cclk	VI SUBSYS ISP RY working clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO.	594	594
vosys pclk	VO SUBSYS APB clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO.	396	396
dpu0 clk	DPU0 PLL frequency division clock, source clock DPU0 PLL FOUTPOSTDIV.	594	594
dpu1 clk	DPU1 PLL frequency division clock, source clock DPU1 PLL FOUTPOSTDIV.	594	594
dpu0_pixelclk	VO SUBSYS DPU0 pixel clock, source clock DPU0 PLL DIV CLK or DPU1 PLL DIV CLK.	594	594
pu_cclk	VO SUBSYS DPU working clock, which is got through frequency division of source clock VIDEO PLL FOUTVCO.	792	792
vosys i2s_clk	VO SUBSYS HDMI I2S clock, output of AP SUBSYS I2S.	12.288	12.288
usb suspend clk	MISC SUBSYS USB3 suspend clock, which is got through frequency division of source clock PAD OSC CLK24.	1	1
dsp0 clk	DSP SUBSYS DSP0 clock, which is got through frequeny division of source clock DSP0 CLK SWITCH.	1000	1000
dsp1 clk	DSP SUBSYS DSP1 clock, which is got through frequency division of source clock DSP1 CLK SWITCH.	1000	1000
dsp0 mclk	DSP SUBSYS DSP0 master clock, which is got through frequency division of source clock DSPSYS DSP0 CLK.	1000	1000
dsp0 sclk	DSP SUBSYS DSP0 slave clock, which is got through frequency division of source clock DSPSYS DSP0 CLK.	1000	1000
dsp1 mclk	DSP SUBSYS DSP1 master clock, which is got through frequency division of source clock DSPSYS DSP1 CLK.	1000	1000
dsp1 sclk	DSP SUBSYS DSP1 slave clock, which is got through frequency division of source clock DSPSYS DSP1 CLK.	1000	1000
dsp0 cclk	DSP SUBSYS DSP0 working clock, which is got through frequency division of source clock DSP0 CLK SWITCH.	1000	1000

Clock	Description	Default Frequency (MHz)	Maximum Frequency (MHz)
dsp1 cclk	DSP SUBSYS DSP1 working clock, which is got through frequency division of source clock DSP1 CLK SWITCH.	1000	1000

4.4 Register Description

4.4.1 Register Memory Map

SUBSYS	REE BASE ADDRESS(C910)	TEE BASE ADDRESS(C910)	REE BASE ADDRESS(E902)	TEE BASE ADDRESS(E902)
AON_SUBSYS	NA	0xFF_FFF4_6000	NA	0xFFF4_6000
AP_SUBSYS	0xFF_EF01_0000	0xFF_FF01_0000	0xBF01_0000	0xFF01_0000
DDR_SUBSYS	NA	0xFF_FF00_5000	NA	0xFF00_5000
MISC_SUBSYS	0xFF_EC02_C000	0xFF_FC02_C000	0xBC02_C000	0xFC02_C000
VI_SUBSYS	0xFF_E404_0000	0xFF_F404_0000	0xB404_0000	0xF404_0000
VO_SUBSYS	0xFF_EF52_8000	0xFF_FF52_8000	0xBF52_8000	0xFF52_8000
VP_SUBSYS	0xFF_ECC3_0000	0xFF_FCC3_0000	0xBCC3_0000	0xFCC3_0000
DSP_SUBSYS	0xFF_EF04_0000	0xFF_FF04_0000	0xBF04_0000	0xFF04_0000
AUDIO_SUBSYS	NA	0xFF_CB00_0000	NA	0xCB00_0000

4.4.1.1 AON_SUBSYS

Register	Offset	Description	Section/Page
AUDIO_PLL_CFG0	0x00	Audio PLL's configuration register 0	4.4.2.1.1/216
AUDIO_PLL_CFG1	0x04	Audio PLL's configuration register 1	4.4.2.1.2/216
AUDIO_PLL_CFG2	0x08	Audio PLL's configuration register 2	4.4.2.1.3/217
AUDIO_PLL_CFG3	0x0c	Audio PLL's configuration register 3	4.4.2.1.4/218
SYS_PLL_CFG0	0x10	System PLL's configuration register 0	4.4.2.1.5/220
SYS_PLL_CFG1	0x14	System PLL's configuration register 1	4.4.2.1.6/220
SYS_PLL_CFG2	0x18	System PLL's configuration register 2	4.4.2.1.7/221
SYS_PLL_CFG3	0x1c	System PLL's configuration register 3	4.4.2.1.8/222
AONSYS_PLL_STS	0x90	System and audio PLL lock flag	4.4.2.1.9/224

Register	Offset	Description	Section/Page
AONSYS_CLK_CFG	0x100	AON clock control register	4.4.2.1.10/224
SHARE_SRAM_CLK_CFG	0x104	Share RAM clock configuration register	4.4.2.1.11/225
AUDIO_SUBSYS_ACLK_CFG	0x108	Audio subsystem aclk configuration register	4.4.2.1.12/227
AUDIO_I2S_CLK_CFG	0x10c	Audio I2S clock switch register	4.4.2.1.13/228
AUDIO_C906_CCLK_CFG	0x110	Audio C906 clock switch and divide control register	4.4.2.1.14/228
AUDIO_CLK_GATE	0x114	Audio aclock gate enable register	4.4.2.1.15/230
AOI2C_CLK_CFG	0x11c	AON I2C clock mux select register	4.4.2.1.16/230
AONSYS_CLK_GATE	0x120	AON clock gate control register	4.4.2.1.17/230
APSYS_CLK_GATE	0x130	APSYS clock gate control register	4.4.2.1.18/233
DSP0_CLK_GATE	0x134	DSP0 clock gate control register	4.4.2.1.19/233
DSP1_CLK_GATE	0x138	DSP1 clock gate control register	4.4.2.1.20/234
GPU_CLK_GATE	0x13c	GPU clock gate control register	4.4.2.1.21/234
VDEC_CLK_GATE	0x140	VDEC clock gate control register	4.4.2.1.22/234
VENC_CLK_GATE	0x144	VENC clock gate control register	4.4.2.1.23/234
RESERVED_REG_0	0x160	Reserved	4.4.2.1.24/235
RESERVED_REG_1	0x164	Reserved	4.4.2.1.25/235
RESERVED_REG_2	0x168	Reserved	4.4.2.1.26/235
RESERVED_REG_3	0x16c	Reserved	4.4.2.1.27/235
AONSYS_CLK_MNT_TEECFG	0x170	AON clock monitor register	4.4.2.1.28/236
TEST_CLK_CFG	0x180	Test clock configuration register	4.4.2.1.29/237
TEST_CLK_STS	0x184	Test clock output register	4.4.2.1.30/237

4.4.1.2 AP_SUBSYS

Register	Offset	Description	Section/Page
CPU_PLL0_CFG0	0x00	CPU PLL configuration register 0	4.4.2.2.1/237
CPU_PLL0_CFG1	0x04	CPU PLL0 configuration register 1	4.4.2.2.2/238
CPU_PLL0_CFG2	0x08	CPU PLL0 configuration register 2	4.4.2.2.3/239

Register	Offset	Description	Section/Page
CPU_PLL0_CFG3	0x0c	CPU PLL0 configuration register 3	4.4.2.2.4/240
CPU_PLL1_CFG0	0x10	CPU PLL1 configuration register 0	4.4.2.2.5/241
CPU_PLL1_CFG1	0x14	CPU PLL1 configuration register 1	4.4.2.2.6/242
CPU_PLL1_CFG2	0x18	CPU PLL1 configuration register 2	4.4.2.2.7/243
CPU_PLL1_CFG3	0x1c	CPU PLL1 configuration register 3	4.4.2.2.8/244
GMAC_PLL_CFG0	0x20	GMAC PLL REE configuration register 0	4.4.2.2.9/245
GMAC_PLL_CFG1	0x24	GMAC PLL REE configuration register 1	4.4.2.2.10/246
GMAC_PLL_CFG2	0x28	GMAC PLL REE configuration register 2	4.4.2.2.11/247
GMAC_PLL_CFG3	0x2c	GMAC PLL REE configuration register 3	4.4.2.2.12/248
VIDEO_PLL_CFG0	0x30	Video PLL REE configuration register 0	4.4.2.2.13/249
VIDEO_PLL_CFG1	0x34	Video PLL REE configuration register 1	4.4.2.2.14/250
VIDEO_PLL_CFG2	0x38	Video PLL REE configuration register 2	4.4.2.2.15/251
VIDEO_PLL_CFG3	0x3c	Video PLL REE configuration register 3	4.4.2.2.16/252
DPU0_PLL_CFG0	0x40	DPU0 PLL REE configuration register 0	4.4.2.2.17/253
DPU0_PLL_CFG1	0x44	DPU0 PLL REE configuration register 1	4.4.2.2.18/254
DPU0_PLL_CFG2	0x48	DPU0 PLL REE configuration register 2	4.4.2.2.19/255
DPU0_PLL_CFG3	0x4c	DPU0 PLL REE configuration register 3	4.4.2.2.20/256
DPU1_PLL_CFG0	0x50	DPU1 PLL REE configuration register 0	4.4.2.2.21/257
DPU1_PLL_CFG1	0x54	DPU1 PLL REE configuration register 1	4.4.2.2.22/258
DPU1_PLL_CFG2	0x58	DPU1 PLL REE configuration register 2	4.4.2.2.23/259
DPU1_PLL_CFG3	0x5c	DPU1 PLL REE configuration register 3	4.4.2.2.24/260
TEE_PLL_CFG0	0x60	TEE PLL REE configuration register 0	4.4.2.2.25/261
TEE_PLL_CFG1	0x64	TEE PLL REE configuration register 1	4.4.2.2.26/262
TEE_PLL_CFG2	0x68	TEE PLL REE configuration register 2	4.4.2.2.27/263
TEE_PLL_CFG3	0x6c	TEE PLL REE configuration register 3	4.4.2.2.28/264
PLL_STS	0x80	All PLLs' status register	4.4.2.2.29/265
C910_CLK_CFG	0x100	C910 clock configuration register	4.4.2.2.30/266
C910_CORE_CLK_CFG	0x104	C910 core clock configuration register	4.4.2.2.31/267
AHB2_CPUSYS_HCLK_CFG	0x120	AHB2_CPUSYS_HCLK configuration register	4.4.2.2.32/270

Register	Offset	Description	Section/Page
APB3_CPUSYS_PCLK_CFG	0x130	APB3_CPUSYS_PCLK configuration register	4.4.2.2.33/271
AXI4_CPUSYS_ACLK_CFG	0x134	AXI4_CPUSYS2_ACLK configuration register	4.4.2.2.34/272
CFG_AXI_ACLK_CFG	0x138	CFG_AXI_ACLK configuration register	4.4.2.2.35/273
PERISYS_AHB_HCLK_CFG	0x140	PERISYS_AHB_HCLK configuration register	4.4.2.2.36/274
PERISYS_APB_PCLK_CFG	0x150		4.4.2.2.37/274
CLK_OUT_1_CFG	0x1b4	Sensor clock configuration register	4.4.2.2.38/276
CLK_OUT_2_CFG	0x1b8	Sensor clock configuration register	4.4.2.2.39/277
CLK_OUT_3_CFG	0x1bc	Sensor clock configuration register	4.4.2.2.40/278
CLK_OUT_4_CFG	0x1c0	Sensor clock configuration register	4.4.2.2.41/278
CFG_APB_PCLK_CFG	0x1c4	cfg_apb_pclk REE configuration register	4.4.2.2.42/279
NPU_CCLK_CFG	0x1c8	npu_cclk REE configuration register	4.4.2.2.43/280
VISYS_CLK_CFG	0x1d0	visys_clk REE configuration register	4.4.2.2.44/281
VOSYS_PCLK_CFG	0x1d8	vosys_pclk REE configuration register	4.4.2.2.45/282
VOSYS_ACLK_CFG	0x1dc	vosys_aclk REE configuration register	4.4.2.2.46/283
VPSYS_CLK_CFG	0x1e0	VPSYS_ACLK configuration register	4.4.2.2.47/283
VENC_CCLK_CFG	0x1e4	VENC CCLK configuration register	4.4.2.2.48/285
DPU0_PLL_DIV_CFG	0x1e8	dpu0_pll_div REE configuration register	4.4.2.2.49/285
DPU1_PLL_DIV_CFG	0x1ec	dpu1_pll_div REE configuration register	4.4.2.2.50/286
PERI_I2S_SRC_CLK_CFG	0x1f0	PERI_I2S_SRC_CLK configuration register	4.4.2.2.51/287
PERI_CLK_CFG	0x204	Peripheral clock gate control register	4.4.2.2.52/287
CTRL_CLK_CFG	0x208	CTRL_CLK configuration register	4.4.2.2.53/291
SRAM_AXI_CLK_CFG	0x20c	SRAM_AXI_CLK configuration register	4.4.2.2.54/292
UART_SCLK_CFG	0x210	uart_aclk REE configuration register	4.4.2.2.55/293
SUBSYS_CLK_CFG	0x220	Subsystem REE configuration register	4.4.2.2.56/293
BOOT_CLK_SEL_CFG	0x280		4.4.2.2.57/294
TEST_CLK_CFG	0x300	TEST_CLK configuration register	4.4.2.2.58/294
TEST_CLK_STS	0x304	TEST_CLK status register	4.4.2.2.59/295
BOOT_OSC_EN	0x308	Reserved	4.4.2.2.60/295
RESERVED_REG_0	0x310	RESERVED_REG_0	4.4.2.2.61/296

Register	Offset	Description	Section/Page
RESERVED_REG_1	0x314	RESERVED_REG_1	4.4.2.2.62/296
RESERVED_REG_2	0x318	RESERVED_REG_2	4.4.2.2.63/296
RESERVED_REG_3	0x31c	RESERVED_REG_3	4.4.2.2.64/296
CPU_PLL0_TEECFG0	0x1000	CPU PLL0 TEE configuration register 0	4.4.2.2.65/297
CPU_PLL0_TEECFG1	0x1004	CPU PLL0 TEE configuration register 1	4.4.2.2.66/297
CPU_PLL0_TEECFG2	0x1008	CPU PLL0 TEE configuration register 2	4.4.2.2.67/298
CPU_PLL0_TEECFG3	0x100c	CPU PLL0 TEE configuration register 3	4.4.2.2.68/299
CPU_PLL1_TEECFG0	0x1010	CPU PLL1 TEE configuration register 0	4.4.2.2.69/301
CPU_PLL1_TEECFG1	0x1014	CPU PLL1 TEE configuration register 1	4.4.2.2.70/301
CPU_PLL1_TEECFG2	0x1018	CPU PLL1 TEE configuration register 2	4.4.2.2.71/302
CPU_PLL1_TEECFG3	0x101c	CPU PLL1 TEE configuration register 3	4.4.2.2.72/303
GMAC_PLL_TEECFG0	0x1020	GMAC PLL TEE configuration register 0	4.4.2.2.73/304
GMAC_PLL_TEECFG1	0x1024	GMAC PLL TEE configuration register 1	4.4.2.2.74/305
GMAC_PLL_TEECFG2	0x1028	GMAC PLL TEE configuration register 2	4.4.2.2.75/306
GMAC_PLL_TEECFG3	0x102c	GMAC PLL TEE configuration register 3	4.4.2.2.76/307
VIDEO_PLL_TEECFG0	0x1030	VIDEO PLL TEE configuration register 0	4.4.2.2.77/308
VIDEO_PLL_TEECFG1	0x1034	VIDEO PLL TEE configuration register 1	4.4.2.2.78/309
VIDEO_PLL_TEECFG2	0x1038	VIDEO PLL TEE configuration register 2	4.4.2.2.79/310
VIDEO_PLL_TEECFG3	0x103c	VIDEO PLL TEE configuration register 3	4.4.2.2.80/311
DPU0_PLL_TEECFG0	0x1040	DPU0 PLL TEE configuration register 0	4.4.2.2.81/312
DPU0_PLL_TEECFG1	0x1044	DPU0 PLL TEE configuration register 1	4.4.2.2.82/313
DPU0_PLL_TEECFG2	0x1048	DPU0 PLL TEE configuration register 2	4.4.2.2.83/314
DPU0_PLL_TEECFG3	0x104c	DPU0 PLL TEE configuration register 3	4.4.2.2.84/315
DPU1_PLL_TEECFG0	0x1050	DPU1 PLL TEE configuration register 0	4.4.2.2.85/316
DPU1_PLL_TEECFG1	0x1054	DPU1 PLL TEE configuration register 1	4.4.2.2.86/317
DPU1_PLL_TEECFG2	0x1058	DPU1 PLL TEE configuration register 2	4.4.2.2.87/318
DPU1_PLL_TEECFG3	0x105c	DPU1 PLL TEE configuration register 3	4.4.2.2.88/319
TEE_PLL_TEECFG0	0x1060	TEE PLL TEE configuration register 0	4.4.2.2.89/320
TEE_PLL_TEECFG1	0x1064	TEE PLL TEE configuration register 1	4.4.2.2.90/321

Register	Offset	Description	Section/Page
TEE_PLL_TEECFG2	0x1068	TEE PLL TEE configuration register 2	4.4.2.2.91/321
TEE_PLL_TEECFG3	0x106c	TEE PLL TEE configuration register 3	4.4.2.2.92/323
PLL_TEESTS	0x1080	All PLLs' status register	4.4.2.2.93/324
C910_CLK_TEECFG	0x1100	C910 clock configuration register	4.4.2.2.94/325
C910_CORE_CLK_TEECFG	0x1104	C910 core clock configuration register	4.4.2.2.95/326
AHB2_CPUSYS_HCLK_TEECFG	0x1120	AHB2_CPUSYS_HCLK configuration register	4.4.2.2.96/329
APB3_CPUSYS_PCLK_TEECFG	0x1130	APB3_CPUSYS_PCLK configuration register	4.4.2.2.97/330
AXI4_CPUSYS_ACLK_TEECFG	0x1134	AXI4_CPUSYS2_ACLK configuration register	4.4.2.2.98/330
CFG_AXI_ACLK_TEECFG	0x1138	CFG_AXI_ACLK configuration register	4.4.2.2.99/331
PERISYS_AHB_HCLK_TEECFG	0x1140	PERISYS_AHB_HCLK configuration register	4.4.2.2.100/332
PERISYS_APB_PCLK_TEECFG	0x1150	PERISYS PCLK configuration reigster	4.4.2.2.101/333
CLK_OUT_1_TEECFG	0x11b4	Sensor clock configuration register	4.4.2.2.102/334
CLK_OUT_2_TEECFG	0x11b8	Sensor clock configuration register	4.4.2.2.103/335
CLK_OUT_3_TEECFG	0x11bc	Sensor clock configuration register	4.4.2.2.104/336
CLK_OUT_4_TEECFG	0x11c0	Sensor clock configuration register	4.4.2.2.105/337
CFG_APB_PCLK_TEECFG	0x11c4	cfg_apb_pclk TEE configuration register	4.4.2.2.106/338
NPU_CCLK_TEECFG	0x11c8	npu_cclk TEE configuration register	4.4.2.2.107/338
TEESYS_CLK_TEECFG	0x11cc	teesys_clk TEE configuration register	4.4.2.2.108/339
VISYS_CLK_TEECFG	0x11d0	visys_clk TEE configuration register	4.4.2.2.109/340
VOSYS_PCLK_TEECFG	0x11d8	vosys_pclk TEE configuration register	4.4.2.2.110/341
VOSYS_ACLK_TEECFG	0x11dc	vosys_aclk TEE configuration register	4.4.2.2.111/342
VPSYS_CLK_TEECFG	0x11e0	VPSYS_ACLK configuration register	4.4.2.2.112/343
VENC_CCLK_TEECFG	0x11e4	VENC CCLK configuration register	4.4.2.2.113/344
DPU0_PLL_DIV_TEECFG	0x11e8	dpu0_pll_div TEE configuration register	4.4.2.2.114/345
DPU1_PLL_DIV_TEECFG	0x11ec	dpu1_pll_div TEE configuration register	4.4.2.2.115/345
PERI_I2S_SRC_CLK_TEECFG	0x11f0	PERI_I2S_SRC_CLK configuration register	4.4.2.2.116/346
PERI_CLK_TEECFG	0x1204	Peripheral clock gate control register	4.4.2.2.117/346
CTRL_CLK_TEECFG	0x1208	CTRL_CLK configuration register	4.4.2.2.118/350
SRAM_AXI_CLK_TEECFG	0x120c	SRAM_AXI_CLK configuration register	4.4.2.2.119/351

Register	Offset	Description	Section/Page
UART_SCLK_TEECFG	0x1210	uart_aclk TEE configuration register	4.4.2.2.120/352
SUBSYS_CLK_TEECFG	0x1220	Subsystem TEE configuration register	4.4.2.2.121/352
BOOT_CLK_SEL_TEECFG	0x1280		4.4.2.2.122/353
TEST_CLK_TEECFG	0x1300	TEST_CLK configuration register	4.4.2.2.123/353
TEST_CLK_TEESTS	0x1304	TEST_CLK status register	4.4.2.2.124/354
BOOT_OSC_EN_TEE	0x1308	Invalid register, software do not use.	4.4.2.2.125/354
RESERVED_TEEREG_0	0x1310	RESERVED_REG_0	4.4.2.2.126/355
RESERVED_TEEREG_1	0x1314	RESERVED_REG_1	4.4.2.2.127/355
RESERVED_TEEREG_2	0x1318	RESERVED_REG_2	4.4.2.2.128/355
RESERVED_TEEREG_3	0x131c	RESERVED_REG_3	4.4.2.2.129/355
CFG_LOCK_0	0x1800	TEE side register domain write lock register	4.4.2.2.130/356
CFG_LOCK_1	0x1804	TEE side register domain write lock register	4.4.2.2.131/358
CFG_LOCK_2	0x1808	TEE side register domain write lock register	4.4.2.2.132/360
CPU_PLL0_MNT_TEECFG	0x1C00	cpu_pll0_foutpostdiv frequency monitor configuration register	4.4.2.2.133/362
CPU_PLL1_MNT_TEECFG	0x1C04	cpu_pll1_foutpostdiv frequency monitor configuration register	4.4.2.2.134/362
TEESYS_HCLK_MNT_TEECFG	0x1C08	teesys_hclk frequency monitor configuration register	4.4.2.2.135/363

4.4.1.3 DDR_SUBSYS

Register	Offset	Description	Section/Page
DDR_CFG1	0x4	Clock auto gate configuration	4.4.2.3.1/364
DDR_PLL_CFG0	0x08	DDR PLL configuration 0	4.4.2.3.2/365
DDR_PLL_CFG1	0x0c	DDR PLL configuration 1	4.4.2.3.3/365
DDR_PLL_CFG2	0x10	DDR PLL configuration 2	4.4.2.3.4/366
DDR_PLL_CFG3	0x14	DDR PLL configuration 3	4.4.2.3.5/367
DDR_PLL_STS	0x18	PLL output configuration	4.4.2.3.6/368
DDR_PLL_MON_STS	0x20	DDR clock monitor frequency indicator	4.4.2.3.7/368
DDR_PLL_MON_CFG	0x24	Clock monitor configuration	4.4.2.3.8/369

4.4.1.4 MISC_SUBSYS

Register	Offset	Description	Section/Page
MISCSYS_BUS_CLK_CTRL	0x100	MISCSYS_BUS_CLK configuration register	4.4.2.4.1/369
MISCSYS_USB_CLK_CTRL	0x104	MISCSYS_USB_CLK configuration register	4.4.2.4.2/369
MISCSYS_EMMC_CLK_CTRL	0x108	MISCSYS_EMMC_CLK configuration register	4.4.2.4.3/370
MISCSYS_SDIO0_CLK_CTRL	0x10c	MISCSYS_SDIO0_CLK configuration register	4.4.2.4.4/370
MISCSYS_SDIO1_CLK_CTRL	0x110	MISCSYS_SDIO1_CLK configuration register	4.4.2.4.5/371
MISCSYS_BUS_CLK_CTRL_TEE	0x1100	MISCSYS_BUS_CLK configuration register	4.4.2.4.6/371
MISCSYS_USB_CLK_CTRL_TEE	0x1104	MISCSYS_USB_CLK configuration register	4.4.2.4.7/371
MISCSYS_EMMC_CLK_CTRL_TEE	0x1108	MISCSYS_EMMC_CLK configuration register	4.4.2.4.8/372
MISCSYS_SDIO0_CLK_CTRL_TEE	0x110c	MISCSYS_SDIO0_CLK configuration register	4.4.2.4.9/372
MISCSYS_SDIO1_CLK_CTRL_TEE	0x1110	MISCSYS_SDIO1_CLK configuration register	4.4.2.4.10/373
MISCSYS_TEE_CLK_CTRL_TEE	0x1120	TEE subsystem clock reset configuration register	4.4.2.4.11/373
TEESYS_PCLK_MNT_TEECFG	0x1124	TEE subsystem APB clock monitor register	4.4.2.4.12/375

4.4.1.5 VI_SUBSYS

Register	Offset	Description	Section/Page
VI_APB_PCLK_CFG	0x10	VISYS_PCLK configuration register	4.4.2.5.1/375
DW200_CLK_DWE_CFG	0x14	DEWARP dewarp core clock configuration register	4.4.2.5.2/376
DW200_CLK_VSE_CFG	0x18	DEWARP scaler core clock configuration register	4.4.2.5.3/376
ISP0_CLK_CFG	0x24	ISP core0 clock configuration register	4.4.2.5.4/377
ISP1_CLK_CFG	0x28	ISP core1 clock configuration register	4.4.2.5.5/377
ISP_RY_CLK_CFG	0x2c	POST ISP clock configuration register	4.4.2.5.6/378
MIPI_CSI0_PIXELCLK	0x30	MIPI CSI output pixel clock configuration register	4.4.2.5.7/379
VISYS_CLK_GATE_EN_0	0xa0	VISYS_CLK_GATE_EN_0	4.4.2.5.8/379
VISYS_CLK_GATE_EN_1	0xa4	VISYS_CLK_GATE_EN_1	4.4.2.5.9/383
TEST_CLK_FREQ_STAT	0x108	TEST_CLK_FREQ_STAT	4.4.2.5.10/384

Register	Offset	Description	Section/Page
TEST_CLK_CFG	0x10c	TEST_CLK_CFG	4.4.2.5.11/384
VI_APB_PCLK_CFG_TEE	0x1010	VISYS_PCLK configuration register	4.4.2.5.12/384
DW200_CLK_DWE_CFG_TEE	0x1014	DEWARP dewarp core clock configuration register	4.4.2.5.13/385
DW200_CLK_VSE_CFG_TEE	0x1018	DEWARP scaler core clock configuration register	4.4.2.5.14/385
ISP0_CLK_CFG_TEE	0x1024	ISP core0 clock configuration register	4.4.2.5.15/386
ISP1_CLK_CFG_TEE	0x1028	ISP core1 clock configuration register	4.4.2.5.16/387
ISP_RY_CLK_CFG_TEE	0x102c	POST ISP clock configuration register	4.4.2.5.17/387
MIPI_CSI0_PIXELCLK_TEE	0x1030	MIPI CSI output pixel clock configuration register	4.4.2.5.18/388
VISYS_CLK_GATE_EN_0_TEE	0x10a0	VISYS_CLK_GATE_EN_0	4.4.2.5.19/388
VISYS_CLK_GATE_EN_1_TEE	0x10a4	VISYS_CLK_GATE_EN_1	4.4.2.5.20/392
TEST_CLK_FREQ_STAT_TEE	0x1108	TEST_CLK_FREQ_STAT	4.4.2.5.21/393
TEST_CLK_CFG_TEE	0x110c	TEST_CLK_CFG	4.4.2.5.22/393
CFG_CLK_LOCK_TEE	0x1200	VI clock registers TEE lock	4.4.2.5.23/394

4.4.1.6 VO_SUBSYS

Register	Offset	Description	Section/Page
VOSYS_CLK_GATE	0x50	Clock gate register	4.4.2.6.1/395
VOSYS_CLK_GATE1	0x54	HDMI pixclk gate register	4.4.2.6.2/399
VOSYS_DPU_CCLK_CFG	0x64	DPU core clock divider register	4.4.2.6.3/399
TEST_CLK_FREQ_STAT	0xc4	Clock frequency register	4.4.2.6.4/400
TEST_CLK_CFG	0xc8	Clock sample control register	4.4.2.6.5/400
VOSYS_CLK_GATE_TEE	0x1050	Clock enable TEE register	4.4.2.6.6/400
VOSYS_CLK_GATE1_TEE	0x1054	HDMI pixel clock enable TEE register	4.4.2.6.7/404
VOSYS_DPU_CCLK_CFG_TEE	0x1064	DPU core clock divider TEE register	4.4.2.6.8/404
TEST_CLK_FREQ_STAT_TEE	0x10c4	Clock frequency TEE register	4.4.2.6.9/405
TEST_CLK_CFG_TEE	0x10c8	Clock sample control TEE register	4.4.2.6.10/405
CFG_LOCK_TEE	0x1a00	Configuration lock TEE register	4.4.2.6.11/405

4.4.1.7 VP_SUBSYS

Register	Offset	Description	Section/Page
VPSYS_CK_CFG	0x20	VPSYS_CK_CFG	4.4.2.7.1/406
VPSYS_VDEC_CCLK_CFG	0x24	VPSYS_VDEC_CCLK_CFG	4.4.2.7.2/408
VPSYS_FCE_CCLK_CFG	0x2c	VPSYS_FCE_CCLK_CFG	4.4.2.7.3/408
VPSYS_G2D_CCLK_CFG	0x30	VPSYS_G2D_CCLK_CFG	4.4.2.7.4/408
VPSYS_FREQM_CFG	0x50	VPSYS_FREQM_CFG	4.4.2.7.5/409
VPSYS_FREQ_STS	0x54	VPSYS_FREQ_STS	4.4.2.7.6/409
VPSYS_CK_TEECFG	0x1020	VPSYS_CK_TEECFG	4.4.2.7.7/410
VPSYS_VDEC_CCLK_TEECFG	0x1024	VPSYS_VDEC_CCLK_TEECFG	4.4.2.7.8/411
VPSYS_FCE_CCLK_TEECFG	0x102c	VPSYS_FCE_CCLK_TEECFG	4.4.2.7.9/411
VPSYS_G2D_CCLK_TEECFG	0x1030	VPSYS_G2D_CCLK_TEECFG	4.4.2.7.10/412
VPSYS_FREQM_TEECFG	0x1050	VPSYS_FREQM_TEECFG	4.4.2.7.11/412
VPSYS_FREQ_TEESTS	0x1054	VPSYS_FREQ_TEESTS	4.4.2.7.12/413
VPSYS_ADDR_TEESEL	0x1060	VPSYS_ADDR_TEESEL	4.4.2.7.13/413

4.4.1.8 DSP_SUBSYS

Register	Offset	Description	Section/Page
DSP0_CLK_CFG	0x0	DSP0 clock configuration register	4.4.2.8.1/413
DSP1_CLK_CFG	0x4	DSP1 clock configuration register	4.4.2.8.2/414
DSP_CLK_CFG	0x8	DSP clock configuration register	4.4.2.8.3/415
DSP0_BUS_SCLK_CFG	0xc	DSP0 slave bus clock configuration register	4.4.2.8.4/415
DSP0_BUS_MCLK_CFG	0x10	DSP0 master bus clock configuration register	4.4.2.8.5/415
DSP1_BUS_SCLK_CFG	0x14	DSP1 slave bus clock configuration register	4.4.2.8.6/416
DSP1_BUS_MCLK_CFG	0x18	DSP1 master bus clock configuration register	4.4.2.8.7/416
DSP0_BUS_CLK_CFG1	0x1c	DSP0 clock switch register	4.4.2.8.8/417
DSP1_BUS_CLK_CFG1	0x20	DSP1 clock switch register	4.4.2.8.9/417
DSPSYS_CLK_GATE_EN_1	0x24	DSP subsystem clock enable register	4.4.2.8.10/418

Register	Offset	Description	Section/Page
TEST_CLK_FREQ_STAT	0x2c	Clock frequency status register	4.4.2.8.11/419
TEST_CLK_CFG	0x30	Test clock configuration register	4.4.2.8.12/419
DSP0_CLK_CFG_TEE	0x1000	DSP0 clock configuration TEE register	4.4.2.8.13/419
DSP1_CLK_CFG_TEE	0x1004	DSP1 clock configuration TEE register	4.4.2.8.14/420
DSP_CLK_CFG_TEE	0x1008	DSP clock configuration TEE register	4.4.2.8.15/420
DSP0_BUS_SCLK_CFG_TEE	0x100c	DSP0 slave bus clock configuration TEE register	4.4.2.8.16/421
DSP0_BUS_MCLK_CFG_TEE	0x1010	DSP0 master bus clock configuration TEE register	4.4.2.8.17/421
DSP1_BUS_SCLK_CFG_TEE	0x1014	DSP1 slave bus clock configuration TEE register	4.4.2.8.18/422
DSP1_BUS_MCLK_CFG_TEE	0x1018	DSP1 master bus clock configuration TEE register	4.4.2.8.19/422
DSP0_BUS_CLK_CFG1_TEE	0x101c	DSP0 clock switch TEE register	4.4.2.8.20/423
DSP1_BUS_CLK_CFG1_TEE	0x1020	DSP1 clock switch TEE register	4.4.2.8.21/423
DSPSYS_CLK_GATE_EN_1_TEE	0x1024	DSP subsystem clock enable TEE register	4.4.2.8.22/423
TEST_CLK_FREQ_STAT_TEE	0x102c	Clock frequency status TEE register	4.4.2.8.23/425
TEST_CLK_CFG_TEE	0x1030	Test clock configuration TEE register	4.4.2.8.24/425
RESERVED_REG_0_TEE	0x1100	Reserved TEE register	4.4.2.8.25/425
RESERVED_REG_1_TEE	0x1104	Reserved TEE register	4.4.2.8.26/425
CFG_CLK_LOCK_TEE	0x1140	Clock lock TEE register	4.4.2.8.27/426
CFG_RST_LOCK_TEE	0x1144	Reset lock TEE register	4.4.2.8.28/426
CFG_DSPSYS_LOCK_TEE	0x1148	DSP subsystem lock TEE register	4.4.2.8.29/427

4.4.1.9 AUDIO_SUBSYS

Register	Offset	Description	Section/Page
SYS_CLK_DIV_REG	0x0	System clock divide select register	4.4.2.9.1/428
PERI_DIV_SEL_REG	0x4	Peripheral working clock divide select register	4.4.2.9.2/430
PERI_CLK_SEL_REG	0x8	Audio peripheral clock source select register	4.4.2.9.3/432

Register	Offset	Description	Section/Page
IP_CG_REG	0x10	Module CG control register	4.4.2.9.4/433
TESTCLK_CTRL_REG	0x98	Test clock control register	4.4.2.9.5/435

4.4.2 Register and Field Description

4.4.2.1 AON_SUBSYS

4.4.2.1.1 AUDIO_PLL_CFG0

- Description: Audio PLL configuration register 0
- Offset: 0x00
- Default Value: 0x1302401

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	
[26:24]	AUDIO_PLL_POSTDIV2	RW	Audio PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x1
[23]	RESERVED_2	-	
[22:20]	AUDIO_PLL_POSTDIV1	RW	Audio PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x3
[19:8]	AUDIO_PLL_FBDIV	RW	Audio PLL feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode) Value After Reset: 0x24
[7:6]	RESERVED_1	-	
[5:0]	AUDIO_PLL_REFDIV	RW	Audio PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.1.2 AUDIO_PLL_CFG1

- Description: Audio PLL configuration register 1
- Offset: 0x04
- Default Value: 0x1000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	

Bits	Field Name	Access	Description
[30]	AUDIO_PLL_BYPASS	RW	Audio PLL FREF is bypassed to FOUTPOSTDIV. Value After Reset: 0x0
[29]	AUDIO_PLL_RST	RW	Audio PLL clock power down control, active high Value After Reset: 0x0
[28]	AUDIO_PLL_FOUTPOSTDIVPD	RW	Audio PLL post divide power down Value After Reset: 0x0
[27]	AUDIO_PLL_FOUT4PHASEPD	RW	Audio PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	
[25]	AUDIO_PLL_DACPD	RW	Power down noise cancelling DAC in FRAC mode 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x0
[24]	AUDIO_PLL_DSMPD	RW	Audio PLL power down Delta-Sigma modulator，active high 0x1: Integer mode，DSM is powered down. 0x0: Fractional mode，DSM is active. Value After Reset: 0x1
[23:0]	AUDIO_PLL_FRAC	RW	Audio PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.1.3 AUDIO_PLL_CFG2

- Description: Audio PLL configuration register 2
- Offset: 0x08
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	AUDIO_PLL_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0
[29]	AUDIO_PLL_DSKEWCALBYP	RW	Anti-skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the

Bits	Field Name	Access	Description
			phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	AUDIO_PLL_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled. 1: Enable skew calibration. Value After Reset: 0x0
[27]	AUDIO_PLL_DSKEWFASTCAL	RW	Anti-skew quick calibration enable Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0
[26:24]	AUDIO_PLL_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default value of 3'd2. Value After Reset: 0x2
[23:12]	AUDIO_PLL_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration sequence. Value After Reset: 0x0
[11:0]	AUDIO_PLL_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.1.4 AUDIO_PLL_CFG3

- Description: Audio PLL configuration register 3
- Offset: 0x0c
- Default Value: 0x7fff400

Bits	Field Name	Access	Description
[31:12]	AUDIO_PLL_CALLOCK_CNT	RW	Offset calibration lock count, received from register,

Bits	Field Name	Access	Description
			quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	AUDIO_PLL_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1
[9]	AUDIO_PLL_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit. Value After Reset: 0x0
[8]	AUDIO_PLL_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the calibration circuit can be bypassed. Value After Reset: 0x0
[7]	AUDIO_PLL_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	

Bits	Field Name	Access	Description
[3:0]	AUDIO_PLL_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.1.5 SYS_PLL_CFG0

- Description: System PLL configuration register 0
- Offset: 0x10
- Default Value: 0x3606501

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	
[26:24]	SYS_PLL_POSTDIV2	RW	System PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x3
[23]	RESERVED_2	-	
[22:20]	SYS_PLL_POSTDIV1	RW	System PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x6
[19:8]	SYS_PLL_FBDIV	RW	Integer value of PLL feedback division divisor (range: 16 ~ 3200 in integer mode and 20 ~ 320 in decimal mode) Value After Reset: 0x65
[7:6]	RESERVED_1	-	
[5:0]	SYS_PLL_REFDIV	RW	System PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.1.6 SYS_PLL_CFG1

- Description: System PLL configuration register 1
- Offset: 0x14
- Default Value: 0x1000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	
[30]	SYS_PLL_BYPASS	RW	System PLL FREF is bypassed to FOUTPOSTDIV. Value After Reset: 0x0
[29]	SYS_PLL_RST	RW	System PLL clock power down control, active high Value After Reset: 0x0
[28]	SYS_PLL_FOUTPOSTDIVPD	RW	System PLL post divide power down Value After Reset: 0x0
[27]	SYS_PLL_FOUT4PHASEPD	RW	System PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	
[25]	SYS_PLL_DACPD	RW	Power down noise cancelling DAC in FRAC mode 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x0
[24]	SYS_PLL_DSMPD	RW	System PLL power down Delta-Sigma modulator 0x1: Integer mode，DSM is powered down. 0x0: Fractional mode，DSM is active. Value After Reset: 0x1
[23:0]	SYS_PLL_FRAC	RW	System PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.1.7 SYS_PLL_CFG2

- Description: System PLL configuration register 2
- Offset: 0x18
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	SYS_PLL_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0

Bits	Field Name	Access	Description
[29]	SYS_PLL_DSKEWCALBYP	RW	Anti-skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	SYS_PLL_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled. 1: Enable skew calibration. Value After Reset: 0x0
[27]	SYS_PLL_DSKEWFASTCAL	RW	Anti-skew quick calibration enable Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0
[26:24]	SYS_PLL_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default value of 3'd2. Value After Reset: 0x2
[23:12]	SYS_PLL_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration sequence. Value After Reset: 0x0
[11:0]	SYS_PLL_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.1.8 SYS_PLL_CFG3

- Description: System PLL configuration register 3
- Offset: 0x1c

- Default Value: 0x7fff400

Bits	Field Name	Access	Description
[31:12]	SYS_PLL_CALLOCK_CNT	RW	Offset calibration lock count, received from register, quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	SYS_PLL_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1
[9]	SYS_PLL_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit. Value After Reset: 0x0
[8]	SYS_PLL_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the calibration circuit can be bypassed. Value After Reset: 0x0
[7]	SYS_PLL_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	

Bits	Field Name	Access	Description
[3:0]	SYS_PLL_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.1.9 AONSYS_PLL_STS

- Description: System and audio PLL lock flag
- Offset: 0x90
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SYS_PLL_LOCK	RO	System PLL frequency lock flag Value After Reset: 0x0
[0]	AUDIO_PLL_LOCK	RO	Audio PLL frequency lock flag Value After Reset: 0x0

4.4.2.1.10 AONSYS_CLK_CFG

- Description: AON clock control register
- Offset: 0x100
- Default Value: 0xc18

Bits	Field Name	Access	Description
[31:12]	RESERVED_2	-	
[11]	AONSYS_CLK_PLL_SRC_DIV_EN	RW	Aonsys_Clk_Pll_SRC frequency division enable Configuration steps are as follows: 1. Configure frequency division enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure frequency division enabling div_EN to be high level.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[10:8]	AONSYS_CLK_PLL_SRC_DIV_NUM	RW	Aonsys_Clk_Pll_SRC frequency division factor 4: 4 frequency division ... 7: 7 frequency division Value After Reset: 0x4
[7:6]	RESERVED_1	-	
[5]	AONSYS_CLK_SWITCH_1_SWITCH_SEL	RW	Aonsys_Clk_Switch_1 option, support no burr switch. 0: aonsys_ Clk_Switch_0 1: rc_ CLK Value After Reset: 0x0
[4]	AONSYS_CLK_SWITCH_0_SWITCH_SEL	RW	Aonsys_Clk_Switch_0 option, support no burr switch. 0: aonsys_ Clk_Pll_SRC 1: pll_Osc_CLK Value After Reset: 0x1
[3]	AONSYS_CLK_CDE_SYNC	RW	Aonsys_CLK frequency division synchronization Configuration steps are as follows: 1. Configure frequency division sync to be low level. 2. Delay 1us. 3. Configure the frequency dividing factor ratio. 4. Configure frequency division sync to be high level. Value After Reset: 0x1
[2:0]	AONSYS_CLK_CDE_RATIO	RW	Aonsys_CLK frequency division factor 0:1 frequency division 1: 2 frequency division ... 7: 8 frequency division Value After Reset: 0x0

4.4.2.1.11 SHARE_SRAM_CLK_CFG

- Description: Share RAM clock configuration register
- Offset: 0x104
- Default Value: 0x1313

Bits	Field Name	Access	Description
[31:14]	RESERVED_2	-	
[13]	SHARE_SRAM_CLK_SWITCH_SEL	RW	Share SRAM clock switch select 0: sys_pll_foutvcco 1: audio_pll_foutvco Value After Reset: 0x0
[12]	SHARE_SRAM_CLK_DIV_1_DIV_EN	RW	Share_Sram_Clk_Div_1 frequency division enable Configuration steps are as follows: 1. Configure frequency division enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure frequency division enabling div_EN to be high level. Value After Reset: 0x1
[11:8]	SHARE_SRAM_CLK_DIV_1_DIV_NUM	RW	Share_Sram_Clk_Div_1 frequency division factor, clock source audio_Pll_Foutvco 3: 3 frequency division ... 15: 15 Frequency Value After Reset: 0x3
[7:5]	RESERVED_1	-	
[4]	SHARE_SRAM_CLK_DIV_0_DIV_EN	RW	Share_Sram_Clk_Div_0 frequency division enable Configuration steps are as follows: 1. Configure frequency division enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure frequency division enabling div_EN to be high level. Value After Reset: 0x1

Bits	Field Name	Access	Description
[3:0]	SHARE_SRAM_CLK_DIV_0_DIV_NUM	RW	Share_Sram_Clk_Div_0 frequency division factor, clock source sys_Pll_Foutvco 3: 3 frequency division ... 15: 15 frequency division Value After Reset: 0x3

4.4.2.1.12 AUDIO_SUBSYS_ACLK_CFG

- Description: Audio SUBSYS aclk configuration register
- Offset: 0x108
- Default Value: 0x1313

Bits	Field Name	Access	Description
[31:14]	RESERVED_2	-	
[13]	AUDIO_SUBSYS_ACLK_SWITCH_SEL	RW	audio_subsys_aclk_switch_sel 0: aclk div0, from system PLL FOUTVCO 1: aclk div1, from audio PLL FOUTVCO Value After Reset: 0x0
[12]	AUDIO_SUBSYS_ACLK_DIV_1_DIV_EN	RW	Audio_Subsys_Aclk_Div_1 frequency division enable Configuration steps are as follows: 1. Configure frequency division enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure frequency division enabling div_EN to be high level. Value After Reset: 0x1
[11:8]	AUDIO_SUBSYS_ACLK_DIV_1_DIV_NUM	RW	Audio_Subsys_Aclk_Div_1 frequency division factor, source clock audio_Pll_Foutvco 3: 3 frequency division ... 15: 15 frequency division Value After Reset: 0x3
[7:5]	RESERVED_1	-	

Bits	Field Name	Access	Description
[4]	AUDIO_SUBSYS_ACLK_DIV_0_DIV_EN	RW	Audio_Subsys_Aclk_Div_0 frequency division enable Configuration steps are as follows: 1. Configure frequency division enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure frequency division enabling div_EN to be high level. Value After Reset: 0x1
[3:0]	AUDIO_SUBSYS_ACLK_DIV_0_DIV_NUM	RW	Audio_Subsys_Aclk_Div_0 frequency division factor, source clock sys_Pll_Foutvco 3: 3 frequency division ... 15: 15 frequency division Value After Reset: 0x3

4.4.2.1.13 AUDIO_I2S_CLK_CFG

- Description: Audio I2S clock switch register
- Offset: 0x10c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	AUDIO_I2S_SRC_CLK_SWITCH_SEL	RW	I2S clock switch 0: Audio PLL FOUTPOSTDIV 1: Audio PLL FOUT3 Value After Reset: 0x0

4.4.2.1.14 AUDIO_C906_CCLK_CFG

- Description: Audio C906 clock switch and divide control register
- Offset: 0x110
- Default Value: 0x1313

Bits	Field Name	Access	Description
[31:14]	RESERVED_2	-	
[13]	AUDIO_C906_CCLK_SWITCH_SEL	RW	audio_c906_cclk_switch_sel

Bits	Field Name	Access	Description
			0: From sys_pll_foutvco div 1: From audio_pll_foutvco div Value After Reset: 0x0
[12]	AUDIO_C906_CCLK_DIV_1_DIV_EN	RW	Audio_C906_Cclk_Div_1 frequency division enable Configuration steps are as follows: 1. Configure frequency division enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure frequency division enabling div_EN to be high level. Value After Reset: 0x1
[11:8]	AUDIO_C906_CCLK_DIV_1_DIV_NUM	RW	Audio_C906_Cclk_Div_1 frequency division factor, source clock audio_Pll_Foutvco 3: 3 frequency division ... 15: 15 frequency division Value After Reset: 0x3
[7:5]	RESERVED_1	-	
[4]	AUDIO_C906_CCLK_DIV_0_DIV_EN	RW	Audio_C906_Cclk_Div_0 frequency division enable Configuration steps are as follows: 1. Configure frequency division enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure frequency division enabling div_EN to be high level. Value After Reset: 0x1
[3:0]	AUDIO_C906_CCLK_DIV_0_DIV_NUM	RW	Audio_C906_Cclk_Div_0 frequency division factor, source clock sys_Pll_Foutvco 3: 3 frequency division ... 15: 15 frequency division Value After Reset: 0x3

4.4.2.1.15 AUDIO_CLK_GATE

- Description: Audio aclock gate enable register
- Offset: 0x114
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	AUDIO_SUBSYS_ACLK_AP2CP_EN	RW	Audio_Subsys_Aclk_Ap2cp gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[0]	AUDIO_SUBSYS_ACLK_CP2AP_EN	RW	Audio_Subsys_Aclk_Cp2ap gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1

4.4.2.1.16 AOI2C_CLK_CFG

- Description: AON I2C clock mux select register
- Offset: 0x11c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	AOI2C_IC_CLK_MUX_SEL	RW	Aoi2c_Ic_CLK selection, no burr switching supported. 0: audio_Pll_Fout3 1: pad_Osc_CLK Value After Reset: 0x1

4.4.2.1.17 AONSYS_CLK_GATE

- Description: AON clock gate control register
- Offset: 0x120
- Default Value: 0x3fef5f

Bits	Field Name	Access	Description
[31:22]	RESERVED_4	-	
[21]	AOUART_PCLK_EN	RW	aouart_pclk gated enable 0: Clock off.

Bits	Field Name	Access	Description
			1: Turn on the clock. Value After Reset: 0x1
[20]	AOUART_SCLK_EN	RW	aouart_sclk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[19]	AOI2C_PCLK_EN	RW	aoi2c_pclk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[18]	AOI2C_IC_CLK_EN	RW	aoi2c_ic_clk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[17]	AUDGPIO_DBCLK_EN	RW	audgpio_dbclk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[16]	AUDGPIO_PCLK_EN	RW	audgpio_pclk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[15]	ADC_PCLK_EN	RW	adc_pclk gated enable 0: Clock off. 1: Turn on the clock Value After Reset: 0x1
[14]	DSPSYS_ACLK_S_EN	RW	dspsys_aclk_s gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[13]	AOWDT_PCLK_EN	RW	aowdt_pclk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1

Bits	Field Name	Access	Description
[12]	RESERVED_3	-	
[11]	AOTIMER_CCLK_EN	RW	aotimer_cclk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[10]	AOTIMER_PCLK_EN	RW	aotimer_pclk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[9]	AOGPIO_DBCLK_EN	RW	aogpio_dbclk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[8]	AOGPIO_PCLK_EN	RW	aogpio_pclk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[7]	RESERVED_2	-	
[6]	AOSRAM_HCLK_EN	RW	aosram_hclk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[5]	RESERVED_1	-	
[4]	AOPAD_PCLK_EN	RW	aopad_pclk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[3]	PVTC_PCLK_EN	RW	pvtc_pclk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1

Bits	Field Name	Access	Description
[2]	SRAM_AXI_ACLK_4_EN	RW	sram_axi_aclk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[1]	SRAM_AXI_CORE_CLK_EN	RW	Sram_Axi_Core_CLK gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[0]	RTC_PCLK_EN	RW	Rtc_PCLK gated enable, source clock aonsys_CLK 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1

4.4.2.1.18 APSYS_CLK_GATE

- Description: APSYS clock gate control register
- Offset: 0x130
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	APSYS_CLK_EN	RW	apsys_clk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1

4.4.2.1.19 DSP0_CLK_GATE

- Description: DSP0 clock gate control register
- Offset: 0x134
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	DSP0_CLK_EN	RW	dsp0_clk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1

4.4.2.1.20 DSP1_CLK_GATE

- Description: DSP1 clock gate control register
- Offset: 0x138
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	DSP1_CLK_EN	RW	dsp1_clk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1

4.4.2.1.21 GPU_CLK_GATE

- Description: GPU clock gate control register
- Offset: 0x13c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	GPU_CLK_EN	RW	gpu_clk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1

4.4.2.1.22 VDEC_CLK_GATE

- Description: VDEC clock gate control register
- Offset: 0x140
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	VDEC_CLK_EN	RW	vdec_clk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1

4.4.2.1.23 VENC_CLK_GATE

- Description: VENC clock gate control register

- Offset: 0x144
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	VENC_CLK_EN	RW	venc_clk gated enable 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1

4.4.2.1.24 RESERVED_REG_0

- Description: Reserved
- Offset: 0x160
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_0	RW	Reserved Value After Reset: 0x0

4.4.2.1.25 RESERVED_REG_1

- Description: Reserved
- Offset: 0x164
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_1	RW	Reserved Value After Reset: 0x0

4.4.2.1.26 RESERVED_REG_2

- Description: Reserved
- Offset: 0x168
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_2	RW	Reserved Value After Reset: 0x0

4.4.2.1.27 RESERVED_REG_3

- Description: Reserved

- Offset: 0x16c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_3	RW	Reserved Value After Reset: 0x0

4.4.2.1.28 AONSYS_CLK_MNT_TEECFG

- Description: AON clock monitor register
- Offset: 0x170
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	AONSYS_CLK_MNT_CFG_LOCK	RW	Aonsys_CLK monitor register domain latch, cannot write to other domains when this bit is 1. Value After Reset: 0x0
[30]	AONSYS_CLK_MNT_EN	RW	Aonsys_CLK monitoring enable. When aonsys_Clk_Mnt_Cfg_lock is 1, the bit cannot be written. aonsys_Clk_Mnt_Cfg_Lock needs to be set to 0 before writing. Value After Reset: 0x0
[29:20]	AONSYS_CLK_MNT_THH	RW	Aonsys_CLK monitoring frequency upper limit. When aonsys_Clk_Mnt_Cfg_lock is 1, the bit cannot be written. aonsys_Clk_Mnt_Cfg_Lock needs to be set to 0 before writing. Value After Reset: 0x0
[19:10]	AONSYS_CLK_MNT_THL	RW	Aonsys_CLK monitoring frequency lower limit. When aonsys_Clk_Mnt_Cfg_lock is 1, the bit cannot be written, aonsys_Clk_Mnt_Cfg_Lock needs to be set to 0 before writing. Value After Reset: 0x0
[9:0]	AONSYS_CLK_MNTEDCLK_DIVFACTOR	RW	Aonsys_CLK monitoring clock frequency dividing factor 0,1: Illegal 2: 2 frequency division 3: 3 frequency division ... Value After Reset: 0x0

4.4.2.1.29 TEST_CLK_CFG

- Description: Test clock configuration register
- Offset: 0x180
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	TEST_CLK_SAMPLE_EN	RW	test_clk's sample enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x0
[3:0]	TEST_CLK_SEL	RW	test_clk[0]: share_sram_clk test_clk[1]: aonsys_clk test_clk[2]: audio_i2s_src_clk test_clk[3]: audio_c906_cclk test_clk[4]: rc_clk test_clk[5]: audio_subsys_aclk test_clk[15:6]: 10'd0 Value After Reset: 0x0

4.4.2.1.30 TEST_CLK_STS

- Description: Test clock output register
- Offset: 0x184
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	TEST_CLK_FREQ_STAT	RO	Read test clock frequency, unit: kHz Value After Reset: 0x0

4.4.2.2 AP_SUBSYS

4.4.2.2.1 CPU_PLL0_CFG0

- Description: CPU PLL configuration register 0
- Offset: 0x00
- Default Value: 0x2507d01

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	

Bits	Field Name	Access	Description
[26:24]	CPU_PLL0_POSTDIV2	RW	CPU PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x2
[23]	RESERVED_2	-	
[22:20]	CPU_PLL0_POSTDIV1	RW	CPU PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x5
[19:8]	CPU_PLL0_FBDIV	RW	CPU PLL feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode) Value After Reset: 0x7D
[7:6]	RESERVED_1	-	
[5:0]	CPU_PLL0_REFDIV	RW	CPU PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.2.2 CPU_PLL0_CFG1

- Description: CPU PLL0 configuration register 1
- Offset: 0x04
- Default Value: 0x3000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	
[30]	CPU_PLL0_BYPASS	RW	CPU PLL FREF is bypassed to FOUTPOSTDIV. Value After Reset: 0x0
[29]	CPU_PLL0_RST	RW	CPU PLL VCO rate output clock power down Value After Reset: 0x0
[28]	CPU_PLL0_FOUTPOSTDIVPD	RW	CPU PLL post divide power down Value After Reset: 0x0
[27]	CPU_PLL0_FOUT4PHASEPD	RW	CPU PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	

Bits	Field Name	Access	Description
[25]	CPU_PLL0_DACPD	RW	Power down noise cancelling DAC in FRAC mode 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x1
[24]	CPU_PLL0_DSMPD	RW	CPU PLL power down Delta-Sigma modulator 0x1: Integer mode, DSM is powered down. 0x0: Fractional mode, DSM is active. Value After Reset: 0x1
[23:0]	CPU_PLL0_FRAC	RW	CPU PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.2.3 CPU_PLL0_CFG2

- Description: CPU PLL0 configuration register 2
- Offset: 0x08
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	CPU_PLL0_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0
[29]	CPU_PLL0_DSKEWCALBYP	RW	Anti-skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	CPU_PLL0_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled. 1: Enable skew calibration. Value After Reset: 0x0
[27]	CPU_PLL0_DSKEWFASTCAL	RW	Anti-skew quick calibration enable Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0

Bits	Field Name	Access	Description
[26:24]	CPU_PLL0_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default value of 3'd2. Value After Reset: 0x2
[23:12]	CPU_PLL0_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration sequence. Value After Reset: 0x0
[11:0]	CPU_PLL0_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.2.4 CPU_PLL0_CFG3

- Description: CPU PLL0 configuration register 3
- Offset: 0x0c
- Default Value: 0x7fff400

Bits	Field Name	Access	Description
[31:12]	CPU_PLL0_CALLOCK_CNT	RW	Offset calibration lock count, received from register, quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	CPU_PLL0_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1

Bits	Field Name	Access	Description
[9]	CPU_PLL0_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit. Value After Reset: 0x0
[8]	CPU_PLL0_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the calibration circuit can be bypassed. Value After Reset: 0x0
[7]	CPU_PLL0_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	
[3:0]	CPU_PLL0_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.2.5 CPU_PLL1_CFG0

- Description: CPU PLL1 configuration register 0
- Offset: 0x10
- Default Value: 0x2507d01

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	

Bits	Field Name	Access	Description
[26:24]	CPU_PLL1_POSTDIV2	RW	CPU PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x2
[23]	RESERVED_2	-	
[22:20]	CPU_PLL1_POSTDIV1	RW	CPU PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x5
[19:8]	CPU_PLL1_FBDIV	RW	CPUP LL feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode) Value After Reset: 0x7D
[7:6]	RESERVED_1	-	
[5:0]	CPU_PLL1_REFDIV	RW	CPU PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.2.6 CPU_PLL1_CFG1

- Description: CPU PLL1 configuration register 1
- Offset: 0x14
- Default Value: 0x3000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	
[30]	CPU_PLL1_BYPASS	RW	CPU PLL FREF is bypassed to FOUTPOSTDIV. Value After Reset: 0x0
[29]	CPU_PLL1_RST	RW	CPU PLL clock power down control, active high Value After Reset: 0x0
[28]	CPU_PLL1_FOUTPOSTDIVPD	RW	CPU PLL post divide power down Value After Reset: 0x0
[27]	CPU_PLL1_FOUT4PHASEPD	RW	CPU PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	

Bits	Field Name	Access	Description
[25]	CPU_PLL1_DACPD	RW	Power down noise cancelling DAC in FRAC mode 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x1
[24]	CPU_PLL1_DSMPD	RW	CPU PLL power down Delta-Sigma modulator 0x1: Integer mode, DSM is powered down. 0x0: Fractional mode, DSM is active. Value After Reset: 0x1
[23:0]	CPU_PLL1_FRAC	RW	CPU PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.2.7 CPU_PLL1_CFG2

- Description: CPU PLL1 configuration register 2
- Offset: 0x18
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	CPU_PLL1_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0
[29]	CPU_PLL1_DSKEWCALBYP	RW	Anti-skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	CPU_PLL1_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled. 1: Enable skew calibration. Value After Reset: 0x0
[27]	CPU_PLL1_DSKEWFASTCAL	RW	Anti-skew quick calibration enable Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0

Bits	Field Name	Access	Description
[26:24]	CPU_PLL1_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default value of 3'd2. Value After Reset: 0x2
[23:12]	CPU_PLL1_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration sequence. Value After Reset: 0x0
[11:0]	CPU_PLL1_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.2.8 CPU_PLL1_CFG3

- Description: CPU PLL1 configuration register 3
- Offset: 0x1c
- Default Value: 0x7fff400

Bits	Field Name	Access	Description
[31:12]	CPU_PLL1_CALLOCK_CNT	RW	Offset calibration lock count, received from register, quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	CPU_PLL1_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1

Bits	Field Name	Access	Description
[9]	CPU_PLL1_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit. Value After Reset: 0x0
[8]	CPU_PLL1_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the calibration circuit can be bypassed. Value After Reset: 0x0
[7]	CPU_PLL1_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	
[3:0]	CPU_PLL1_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.2.9 GMAC_PLL_CFG0

- Description: GMAC PLL REE configuration register 0
- Offset: 0x20
- Default Value: 0x1307d01

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	

Bits	Field Name	Access	Description
[26:24]	GMAC_PLL_POSTDIV2	RW	GMAC PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x1
[23]	RESERVED_2	-	
[22:20]	GMAC_PLL_POSTDIV1	RW	GMAC PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x3
[19:8]	GMAC_PLL_FBDIV	RW	GMAC PLL feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode) Value After Reset: 0x7D
[7:6]	RESERVED_1	-	
[5:0]	GMAC_PLL_REFDIV	RW	GMAC PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.2.10 GMAC_PLL_CFG1

- Description: GMAC PLL REE configuration register 1
- Offset: 0x24
- Default Value: 0x3000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	
[30]	GMAC_PLL_BYPASS	RW	GMAC PLL clock power down control, active high Value After Reset: 0x0
[29]	GMAC_PLL_RST	RW	GMAC PLL VCO rate output clock power down Value After Reset: 0x0
[28]	GMAC_PLL_FOUTPOSTDIVPD	RW	GMAC PLL post divide power down Value After Reset: 0x0
[27]	GMAC_PLL_FOUT4PHASEPD	RW	GMAC PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	

Bits	Field Name	Access	Description
[25]	GMAC_PLL_DACPD	RW	Power down noise cancelling DAC in FRAC mode 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x1
[24]	GMAC_PLL_DSMPD	RW	CPU PLL power down Delta-Sigma modulator 0x1: Integer mode, DSM is powered down. 0x0: Fractional mode, DSM is active. Value After Reset: 0x1
[23:0]	GMAC_PLL_FRAC	RW	GMAC PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.2.11 GMAC_PLL_CFG2

- Description: GMAC PLL REE configuration register 2
- Offset: 0x28
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	GMAC_PLL_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0
[29]	GMAC_PLL_DSKEWCALBYP	RW	Anti-skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	GMAC_PLL_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled. 1: Enable skew calibration. Value After Reset: 0x0
[27]	GMAC_PLL_DSKEWFASTCAL	RW	Anti-skew quick calibration enable Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0

Bits	Field Name	Access	Description
[26:24]	GMAC_PLL_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default value of 3'd2. Value After Reset: 0x2
[23:12]	GMAC_PLL_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration sequence. Value After Reset: 0x0
[11:0]	GMAC_PLL_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.2.12 GMAC_PLL_CFG3

- Description: GMAC PLL REE configuration register 3
- Offset: 0x2c
- Default Value: 0x7fff400

Bits	Field Name	Access	Description
[31:12]	GMAC_PLL_CALLOCK_CNT	RW	Offset calibration lock count, received from register, quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	GMAC_PLL_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1

Bits	Field Name	Access	Description
[9]	GMAC_PLL_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit. Value After Reset: 0x0
[8]	GMAC_PLL_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the calibration circuit can be bypassed. Value After Reset: 0x0
[7]	GMAC_PLL_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	
[3:0]	GMAC_PLL_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.2.13 VIDEO_PLL_CFG0

- Description: Video PLL REE configuration register 0
- Offset: 0x30
- Default Value: 0x1306301

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	

Bits	Field Name	Access	Description
[26:24]	VIDEO_PLL_POSTDIV2	RW	Video PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x1
[23]	RESERVED_2	-	
[22:20]	VIDEO_PLL_POSTDIV1	RW	Video PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x3
[19:8]	VIDEO_PLL_FBDIV	RW	Video PLL feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode) Value After Reset: 0x63
[7:6]	RESERVED_1	-	
[5:0]	VIDEO_PLL_REFDIV	RW	Video PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.2.14 VIDEO_PLL_CFG1

- Description: Video PLL REE configuration register 1
- Offset: 0x34
- Default Value: 0x3000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	
[30]	VIDEO_PLL_BYPASS	RW	Video PLL clock power down control, active high Value After Reset: 0x0
[29]	VIDEO_PLL_RST	RW	Video PLL VCO rate output clock power down Value After Reset: 0x0
[28]	VIDEO_PLL_FOUTPOSTDIVPD	RW	Video PLL post divide power down Value After Reset: 0x0
[27]	VIDEO_PLL_FOUT4PHASEPD	RW	Video PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	

Bits	Field Name	Access	Description
[25]	VIDEO_PLL_DACPD	RW	Power down noise cancelling DAC in FRAC mode 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x1
[24]	VIDEO_PLL_DSMPD	RW	CPU PLL power down Delta-Sigma modulator 0x1: Integer mode, DSM is powered down. 0x0: Fractional mode, DSM is active. Value After Reset: 0x1
[23:0]	VIDEO_PLL_FRAC	RW	Video PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.2.15 VIDEO_PLL_CFG2

- Description: Video PLL REE configuration register 2
- Offset: 0x38
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	VIDEO_PLL_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0
[29]	VIDEO_PLL_DSKEWCALBYP	RW	Anti-skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	VIDEO_PLL_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled. 1: Enable skew calibration. Value After Reset: 0x0
[27]	VIDEO_PLL_DSKEWFASTCAL	RW	Anti-skew quick calibration enable Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0

Bits	Field Name	Access	Description
[26:24]	VIDEO_PLL_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default value of 3'd2. Value After Reset: 0x2
[23:12]	VIDEO_PLL_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration sequence. Value After Reset: 0x0
[11:0]	VIDEO_PLL_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.2.16 VIDEO_PLL_CFG3

- Description: Video PLL REE configuration register 3
- Offset: 0x3c
- Default Value: 0x7fff400

Bits	Field Name	Access	Description
[31:12]	VIDEO_PLL_CALLOCK_CNT	RW	Offset calibration lock count, received from register, quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	VIDEO_PLL_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1

Bits	Field Name	Access	Description
[9]	VIDEO_PLL_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit. Value After Reset: 0x0
[8]	VIDEO_PLL_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the calibration circuit can be bypassed. Value After Reset: 0x0
[7]	VIDEO_PLL_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	
[3:0]	VIDEO_PLL_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.2.17 DPU0_PLL_CFG0

- Description: DPU0 PLL REE configuration register 0
- Offset: 0x40
- Default Value: 0x1206301

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	

Bits	Field Name	Access	Description
[26:24]	DPU0_PLL_POSTDIV2	RW	DPU0 PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x1
[23]	RESERVED_2	-	
[22:20]	DPU0_PLL_POSTDIV1	RW	DPU0 PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x2
[19:8]	DPU0_PLL_FBDIV	RW	DPU0 PLL feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode) Value After Reset: 0x63
[7:6]	RESERVED_1	-	
[5:0]	DPU0_PLL_REFDIV	RW	DPU0 PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.2.18 DPU0_PLL_CFG1

- Description: DPU0 PLL REE configuration register 1
- Offset: 0x44
- Default Value: 0x3000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	
[30]	DPU0_PLL_BYPASS	RW	DPU0 PLL clock power down control, active high Value After Reset: 0x0
[29]	DPU0_PLL_RST	RW	DPU0 PLL VCO rate output clock power down, active high Value After Reset: 0x0
[28]	DPU0_PLL_FOUTPOSTDIVPD	RW	DPU0 PLL post divide power down, active high Value After Reset: 0x0
[27]	DPU0_PLL_FOUT4PHASEPD	RW	DPU0 PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	

Bits	Field Name	Access	Description
[25]	DPU0_PLL_DACPD	RW	Power down noise cancelling DAC in FRAC mode 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x1
[24]	DPU0_PLL_DSMPD	RW	CPU PLL power down Delta-Sigma modulator 0x1: Integer mode, DSM is powered down. 0x0: Fractional mode, DSM is active. Value After Reset: 0x1
[23:0]	DPU0_PLL_FRAC	RW	DPU0 PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.2.19 DPU0_PLL_CFG2

- Description: DPU0 PLL REE configuration register 2
- Offset: 0x48
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	DPU0_PLL_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0.
[29]	DPU0_PLL_DSKEWCALBYP	RW	Anti-skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	DPU0_PLL_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled. 1: Enable skew calibration. Value After Reset: 0x0
[27]	DPU0_PLL_DSKEWFASTCAL	RW	Anti-skew quick calibration enable Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0

Bits	Field Name	Access	Description
[26:24]	DPU0_PLL_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default value of 3'd2. Value After Reset: 0x2
[23:12]	DPU0_PLL_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration sequence. Value After Reset: 0x0
[11:0]	DPU0_PLL_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.2.20 DPU0_PLL_CFG3

- Description: DPU0 PLL REE configuration register 3
- Offset: 0x4c
- Default Value: 0x7fff400

Bits	Field Name	Access	Description
[31:12]	DPU0_PLL_CALLOCK_CNT	RW	Offset calibration lock count, received from register, quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	DPU0_PLL_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1

Bits	Field Name	Access	Description
[9]	DPU0_PLL_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit. Value After Reset: 0x0
[8]	DPU0_PLL_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the calibration circuit can be bypassed. Value After Reset: 0x0
[7]	DPU0_PLL_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	
[3:0]	DPU0_PLL_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.2.21 DPU1_PLL_CFG0

- Description: DPU1 PLL REE configuration register 0
- Offset: 0x50
- Default Value: 0x1206301

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	

Bits	Field Name	Access	Description
[26:24]	DPU1_PLL_POSTDIV2	RW	DPU1 PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x1
[23]	RESERVED_2	-	
[22:20]	DPU1_PLL_POSTDIV1	RW	DPU1 PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x2
[19:8]	DPU1_PLL_FBDIV	RW	DPU1 PLL feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode) Value After Reset: 0x63
[7:6]	RESERVED_1	-	
[5:0]	DPU1_PLL_REFDIV	RW	DPU1 PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.2.22 DPU1_PLL_CFG1

- Description: DPU1 PLL REE configuration register 1
- Offset: 0x54
- Default Value: 0x3000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	
[30]	DPU1_PLL_BYPASS	RW	DPU1 PLL clock power down control, active high Value After Reset: 0x0
[29]	DPU1_PLL_RST	RW	DPU1 PLL VCO rate output clock power down Value After Reset: 0x0
[28]	DPU1_PLL_FOUTPOSTDIVPD	RW	DPU1 PLL post divide power down Value After Reset: 0x0
[27]	DPU1_PLL_FOUT4PHASEPD	RW	DPU1 PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	

Bits	Field Name	Access	Description
[25]	DPU1_PLL_DACPD	RW	Power down noise cancelling DAC in FRAC mode 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x1
[24]	DPU1_PLL_DSMPD	RW	CPU PLL power down Delta-Sigma modulator 0x1: Integer mode, DSM is powered down. 0x0: Fractional mode, DSM is active. Value After Reset: 0x1
[23:0]	DPU1_PLL_FRAC	RW	DPU1 PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.2.23 DPU1_PLL_CFG2

- Description: DPU1 PLL REE configuration register 2
- Offset: 0x58
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	DPU1_PLL_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0
[29]	DPU1_PLL_DSKEWCALBYP	RW	Anti-skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	DPU1_PLL_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled. 1: Enable skew calibration. Value After Reset: 0x0
[27]	DPU1_PLL_DSKEWFASTCAL	RW	Anti-skew quick calibration enable Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0

Bits	Field Name	Access	Description
[26:24]	DPU1_PLL_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default value of 3'd2. Value After Reset: 0x2
[23:12]	DPU1_PLL_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration sequence. Value After Reset: 0x0
[11:0]	DPU1_PLL_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.2.24 DPU1_PLL_CFG3

- Description: DPU1 PLL REE configuration register 3
- Offset: 0x5c
- Default Value: 0x7fff400

Bits	Field Name	Access	Description
[31:12]	DPU1_PLL_CALLOCK_CNT	RW	Offset calibration lock count, received from register, quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	DPU1_PLL_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1

Bits	Field Name	Access	Description
[9]	DPU1_PLL_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit. Value After Reset: 0x0
[8]	DPU1_PLL_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the calibration circuit can be bypassed. Value After Reset: 0x0
[7]	DPU1_PLL_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	
[3:0]	DPU1_PLL_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.2.25 TEE_PLL_CFG0

- Description: TEE PLL REE configuration register 0
- Offset: 0x60
- Default Value: 0x1306301

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	

Bits	Field Name	Access	Description
[26:24]	TEE_PLL_POSTDIV2	RW	TEE PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x1
[23]	RESERVED_2	-	
[22:20]	TEE_PLL_POSTDIV1	RW	TEE PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x3
[19:8]	TEE_PLL_FBDIV	RW	TEE PLL feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode) Value After Reset: 0x63
[7:6]	RESERVED_1	-	
[5:0]	TEE_PLL_REFDIV	RW	TEE PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.2.26 TEE_PLL_CFG1

- Description: TEE PLL REE configuration register 1
- Offset: 0x64
- Default Value: 0x63000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	
[30]	TEE_PLL_BYPASS	RW	TEE PLL clock power down control, active high Value After Reset: 0x1
[29]	TEE_PLL_RST	RW	TEE PLL VCO rate output clock power down Value After Reset: 0x1
[28]	TEE_PLL_FOUTPOSTDIVPD	RW	TEE PLL post divide power down Value After Reset: 0x0
[27]	TEE_PLL_FOUT4PHASEPD	RW	TEE PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	

Bits	Field Name	Access	Description
[25]	TEE_PLL_DACPD	RW	Power down noise cancelling DAC in FRAC mode 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x1
[24]	TEE_PLL_DSMPD	RW	CPU PLL power down Delta-Sigma modulator 0x1: Integer mode, DSM is powered down. 0x0: Fractional mode, DSM is active. Value After Reset: 0x1
[23:0]	TEE_PLL_FRAC	RW	TEE PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.2.27 TEE_PLL_CFG2

- Description: TEE PLL REE configuration register 2
- Offset: 0x68
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	TEE_PLL_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0
[29]	TEE_PLL_DSKEWCALBYP	RW	Anti skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	TEE_PLL_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled. 1: Enable skew calibration. Value After Reset: 0x0
[27]	TEE_PLL_DSKEWFASTCAL	RW	Anti-skew quick calibration enable Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0

Bits	Field Name	Access	Description
[26:24]	TEE_PLL_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default value of 3'd2. Value After Reset: 0x2
[23:12]	TEE_PLL_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration sequence. Value After Reset: 0x0
[11:0]	TEE_PLL_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.2.28 TEE_PLL_CFG3

- Description: TEE PLL REE configuration register 3
- Offset: 0x6c
- Default Value: 0x7fff500

Bits	Field Name	Access	Description
[31:12]	TEE_PLL_CALLOCK_CNT	RW	Offset calibration lock count, received from register, quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	TEE_PLL_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1

Bits	Field Name	Access	Description
[9]	TEE_PLL_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit. Value After Reset: 0x0
[8]	TEE_PLL_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the calibration circuit can be bypassed. Value After Reset: 0x1
[7]	TEE_PLL_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	
[3:0]	TEE_PLL_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.2.29 PLL_STS

- Description: All PLLs' status register
- Offset: 0x80
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	

Bits	Field Name	Access	Description
[10]	TEE_PLL_LOCK	RO	TEE PLL frequency locked status Value After Reset: 0x0
[9]	DPU1_PLL_LOCK	RO	DPU1 PLL frequency locked status Value After Reset: 0x0
[8]	DPU0_PLL_LOCK	RO	DPU0 PLL frequency locked status Value After Reset: 0x0
[7]	VIDEO_PLL_LOCK	RO	Video PLL frequency locked status Value After Reset: 0x0
[6]	SYS_PLL_LOCK	RO	System PLL frequency locked status Value After Reset: 0x0
[5]	AUDIO_PLL_LOCK	RO	Audio PLL frequency locked status Value After Reset: 0x0
[4]	CPU_PLL1_LOCK	RO	CPU PLL1 frequency locked status Value After Reset: 0x0
[3]	GMAC_PLL_LOCK	RO	GMAC PLL frequency locked status Value After Reset: 0x0
[2]	DDR_PLL_LOCK	RO	DDR PLL frequency locked status Value After Reset: 0x0
[1]	CPU_PLL0_LOCK	RO	CPU PLL0 frequency locked status Value After Reset: 0x0
[0]	ALL_PLL_LOCK	RO	All PLLs' frequency locked status Value After Reset: 0x0

4.4.2.2.30 C910_CLK_CFG

- Description: C910 clock configuration reigster
- Offset: 0x100
- Default Value: 0x9f0

Bits	Field Name	Access	Description
[31:12]	RESERVED_2	-	
[11]	C910_BUS_CLK_SYNC	RW	c910_bus_clk's divider enable, software needs to be pulled low and then pulled high. Value After Reset: 0x1

Bits	Field Name	Access	Description
[10:8]	C910_BUS_CLK_RATIO	RW	c910_bus_clk's divider ratio 3'd1: 1:2 3'd2: 1:3 ..... 3'd7: 1:8 Value After Reset: 0x1
[7]	C910_BUS_CLK_EN	RW	c910_bus_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[6]	C910_CLK_EN	RW	c910_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[5]	BMU_C910_CLK_EN	RW	bmu_c910_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	C910_BROM_HCLK_EN	RW	c910_brom_hclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[3:2]	RESERVED_1	-	
[1]	C910_CCLK_I0_SWITCH_SEL	RW	c910_cclk_i0 clock select 0: PLL0 1: OSC_CLK Value After Reset: 0x0
[0]	C910_CCLK_SWITCH_SEL	RW	c910_cclk clock select 0: c910_cclk_i0 1: PLL1 Value After Reset: 0x0

4.4.2.2.31 C910_CORE_CLK_CFG

- Description: C910 core clock configuration register

- Offset: 0x104
- Default Value: 0x30303030

Bits	Field Name	Access	Description
[31:30]	RESERVED_4	-	
[29]	C910_CORE3_CLK_EN	RW	c910_core3_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[28]	C910_CORE3_CLK_DIV_EN	RW	c910_core3_clk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[27:24]	C910_CORE3_CLK_DIV_NUM	RW	c910_core3_clk's divider ratio 3'd0: 1:1 3'd1: 1:2 ..... 3'd6: 1:7 3'd7: 1:8 Value After Reset: 0x0
[23:22]	RESERVED_3	-	
[21]	C910_CORE2_CLK_EN	RW	c910_core2_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[20]	C910_CORE2_CLK_DIV_EN	RW	c910_core2_clk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1

Bits	Field Name	Access	Description
[19:16]	C910_CORE2_CLK_DIV_NUM	RW	c910_core2_clk's divider ratio 3'd0: 1:1 3'd1: 1:2 ..... 3'd6: 1:7 3'd7: 1:8 Value After Reset: 0x0
[15:14]	RESERVED_2	-	
[13]	C910_CORE1_CLK_EN	RW	c910_core1_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[12]	C910_CORE1_CLK_DIV_EN	RW	c910_core1_clk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[11:8]	C910_CORE1_CLK_DIV_NUM	RW	c910_core1_clk's divider ratio 3'd0: 1:1 3'd1: 1:2 ..... 3'd6: 1:7 3'd7: 1:8 Value After Reset: 0x0
[7:6]	RESERVED_1	-	
[5]	C910_CORE0_CLK_EN	RW	c910_core0_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

Bits	Field Name	Access	Description
[4]	C910_CORE0_CLK_DIV_EN	RW	c910_core0_clk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3:0]	C910_CORE0_CLK_DIV_NUM	RW	c910_core0_clk's divider ratio 3'd0: 1:1 3'd1: 1:2 ..... 3'd6: 1:7 3'd7: 1:8 Value After Reset: 0x0

4.4.2.2.32 AHB2_CPUSYS_HCLK_CFG

- Description: AHB2_CPUSYS_HCLK configuration register
- Offset: 0x120
- Default Value: 0xd4

Bits	Field Name	Access	Description
[31:8]	RESERVED_2	-	
[7]	X2H_CPUSYS_CLK_EN	RW	Reserved, software can't write this field. Value After Reset: 0x1
[6]	AHB2_CPUSYS_HCLK_EN	RW	Reserved, software can't write this field. Value After Reset: 0x1
[5]	AHB2_CPUSYS_HCLK_SWITCH_SEL	RW	ahb2_cpusys_hclk clock select 0: PLL 1: OSC_CLK Value After Reset: 0x0

Bits	Field Name	Access	Description
[4]	AHB2_CPUSYS_HCLK_DIV_EN	RW	ahb2_cpusys_hclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3]	RESERVED_1	-	
[2:0]	AHB2_CPUSYS_HCLK_DIV_NUM	RW	ahb2_cpusys_hclk's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x4

4.4.2.2.33 APB3_CPUSYS_PCLK_CFG

- Description: APB3_CPUSYS_PCLK configuration register
- Offset: 0x130
- Default Value: 0x18

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	APB3_CPUSYS_HCLK_EN	RW	Reserved, software can't write this field. Value After Reset: 0x1
[3]	APB3_CPUSYS_PCLK_CDE_SYNC	RW	apb3_cpusys_hclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1

Bits	Field Name	Access	Description
[2:0]	APB3_CPUSYS_PCLK_CDE_RATIO	RW	apb3_cpusys_hclk's divider ratio 3'd1: 1:2 3'd2: 1:3 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.2.34 AXI4_CPUSYS_ACLK_CFG

- Description: AXI4_CPUSYS2_ACLK configuration register
- Offset: 0x134
- Default Value: 0x1b2

Bits	Field Name	Access	Description
[31:9]	RESERVED_3	-	
[8]	AON2CPU_A2X_CLK_EN	RW	aon2cpu_a2x_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[7]	X2X_CPUSYS_CLK_EN	RW	x2x_cpusys_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[6]	RESERVED_2	-	
[5]	AXI4_CPUSYS2_CLK_EN	RW	Reserved, software can't write this field. Value After Reset: 0x1
[4]	AXI4_CPUSYS2_ACLK_DIV_EN	RW	axi4_cpusys2_clk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3]	RESERVED_1	-	

Bits	Field Name	Access	Description
[2:0]	AXI4_CPUSYS2_ACLK_DIV_NUM	RW	axi4_cpusys2_clk's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.35 CFG_AXI_ACLK_CFG

- Description: CFG_AXI_ACLK configuration register
- Offset: 0x138
- Default Value: 0x112

Bits	Field Name	Access	Description
[31:9]	RESERVED_2	-	
[8]	CPU2AON_X2H_CLK_EN	RW	cpu2aon_x2h_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[7:6]	RESERVED_1	-	
[5]	CFG_AXI_ACLK_SWITCH_SEL	RW	cfg_axi_aclk clock select 0: PLL 1: OSC_CLK Value After Reset: 0x0
[4]	CFG_AXI_ACLK_DIV_EN	RW	cfg_axi_aclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3:0]	CFG_AXI_ACLK_DIV_NUM	RW	cfg_axi_aclk's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.36 PERISYS_AHB_HCLK_CFG

- Description: PERISYS_AHB_HCLK configuration register
- Offset: 0x140
- Default Value: 0x258

Bits	Field Name	Access	Description
[31:10]	RESERVED_2	-	
[9]	CPU2PERI_X2H_CLK_EN	RW	cpu2peri_x2h_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[8:7]	RESERVED_1	-	
[6]	PERISYS_AHB_HCLK_EN	RW	perisys_ahb_hclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[5]	PERISYS_AHB_HCLK_SWITCH_SEL	RW	perisys_ahb_hclk clock select 0: PLL 1: OSC_CLK Value After Reset: 0x0
[4]	PERISYS_AHB_HCLK_DIV_EN	RW	perisys_ahb_hclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3:0]	PERISYS_AHB_HCLK_DIV_NUM	RW	perisys_ahb_hclk's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x8

4.4.2.2.37 PERISYS_APB_PCLK_CFG

- Description:

- Offset: 0x150
- Default Value: 0x1f28

Bits	Field Name	Access	Description
[31:13]	RESERVED_2	-	
[12]	PERISYS_APB4_HCLK_EN	RW	perisys_apb4_hclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[11]	PERISYS_APB3_HCLK_EN	RW	perisys_apb3_hclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[10]	PERISYS_APB2_HCLK_EN	RW	perisys_apb2_hclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[9]	PERISYS_APB1_HCLK_EN	RW	perisys_apb1_hclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[8]	PERI2SYS_APB_PCLK_DIV_EN	RW	peri2sys_apb_pclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[7]	RESERVED_1	-	
[6:4]	PERI2SYS_APB_PCLK_DIV_NUM	RW	peri2sys_apb_pclk's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

Bits	Field Name	Access	Description
[3]	PERISYS_APB_PCLK_CDE_SYNC	RW	perisys_pclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[2:0]	PERISYS_APB_PCLK_CDE_RATIO	RW	perisys_pclk's divider ratio 3'd3: 1:4 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.2.38 CLK_OUT_1_CFG

- Description: Sensor clock configuration register
- Offset: 0x1b4
- Default Value: 0x2a

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	CLK_OUT_1_CLK_EN	RW	Sensor clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	CLK_OUT_1_MUX_SEL	RW	Sensor clock select 0: 24MHz 1: 12MHz divider Value After Reset: 0x0
[3]	CLK_OUT_1_DIV_EN	RW	Sensor clock's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1

Bits	Field Name	Access	Description
[2:0]	CLK_OUT_1_DIV_NUM	RW	Sensor clock 's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.39 CLK_OUT_2_CFG

- Description: Sensor clock configuration register
- Offset: 0x1b8
- Default Value: 0x2a

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	CLK_OUT_2_CLK_EN	RW	Sensor clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	CLK_OUT_2_MUX_SEL	RW	Sensor clock select 0: 24MHz 1: 12MHz divider Value After Reset: 0x0
[3]	CLK_OUT_2_DIV_EN	RW	Sensor clock’s divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[2:0]	CLK_OUT_2_DIV_NUM	RW	Sensor clock’s divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.40 CLK_OUT_3_CFG

- Description: Sensor clock configuration register
- Offset: 0x1bc
- Default Value: 0x2a

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	CLK_OUT_3_CLK_EN	RW	Sensor clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	CLK_OUT_3_MUX_SEL	RW	Sensor clock select 0: 24MHz 1: 12MHz divider Value After Reset: 0x0
[3]	CLK_OUT_3_DIV_EN	RW	Sensor clock's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[2:0]	CLK_OUT_3_DIV_NUM	RW	Sensor clock's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.41 CLK_OUT_4_CFG

- Description: Sensor clock configuration register
- Offset: 0x1c0
- Default Value: 0x2a

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	CLK_OUT_4_CLK_EN	RW	Sensor clock gate enable signal 0: Gate clock.

Bits	Field Name	Access	Description
			1: Open clock. Value After Reset: 0x1
[4]	CLK_OUT_4_MUX_SEL	RW	Sensor clock select 0: 24MHz 1: 12MHz divider Value After Reset: 0x0
[3]	CLK_OUT_4_DIV_EN	RW	Sensor clock's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[2:0]	CLK_OUT_4_DIV_NUM	RW	Sensor clock's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.42 CFG_APB_PCLK_CFG

- Description: cfg_apb_pclk REE configuration register
- Offset: 0x1c4
- Default Value: 0x34

Bits	Field Name	Access	Description
[31:8]	RESERVED_2	-	
[7]	CFG_APB_PCLK_SWITCH_SEL	RW	cfg_apb_pclk_switch_sel Value After Reset: 0x0
[6]	RESERVED_1	-	
[5]	APB_CPU2CFG_HCLK_EN	RW	apb_cpu2cfg_hclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

Bits	Field Name	Access	Description
[4]	CFG_APB_PCLK_DIV_EN	RW	cfg_apb_pclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3:0]	CFG_APB_PCLK_DIV_NUM	RW	cfg_apb_pclk's divider ratio 4'd4: 1:4 ..... 4'd15: 1:15 Value After Reset: 0x4

4.4.2.2.43 NPU_CCLK_CFG

- Description: npu_cclk REE configuration register
- Offset: 0x1c8
- Default Value: 0xb

Bits	Field Name	Access	Description
[31:7]	RESERVED_1	-	
[6]	NPU_CCLK_SWITCH_SEL	RW	0: 1000M 1: The maximum frequency is 792. Can be changed by configuring bit[3:0]. Value After Reset: 0x0
[5]	NPU_AXI_ACLK_EN	RW	npu_axi_aclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x0
[4]	NPU_CORE_CLK_EN	RW	npu_core_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x0

Bits	Field Name	Access	Description
[3]	NPU_CCLK_DIV_EN	RW	npu_cclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[2:0]	NPU_CCLK_DIV_NUM	RW	npu_cclk's divider ratio 3'd3: 1:3 ..... 3'd7: 1:7 Value After Reset: 0x3

4.4.2.2.44 VISYS_CLK_CFG

- Description: visys_clk REE configuration register
- Offset: 0x1d0
- Default Value: 0x330016

Bits	Field Name	Access	Description
[31:22]	RESERVED_2	-	
[21]	CPU2VI_X2H_CLK_EN	RW	cpu2vi_x2h_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[20]	VISYS_ACLK_M_DIV_EN	RW	visys_aclk_m's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1

Bits	Field Name	Access	Description
[19:16]	VISYS_ACLK_M_DIV_NUM	RW	visys_aclk_m's divider ratio 3'd3: 1:3 ..... 3'd7: 1:7 Value After Reset: 0x3
[15:5]	RESERVED_1	-	
[4]	VISYS_AHB_HCLK_DIV_EN	RW	visys_ahb_hclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN is to be high level. Value After Reset: 0x1
[3:0]	VISYS_AHB_HCLK_DIV_NUM	RW	visys_ahb_hclk's divider ratio 4'd6: 1:6 ..... 4'd15: 1:15 Value After Reset: 0x6

4.4.2.2.45 VOSYS_PCLK_CFG

- Description: vosys_pclk REE configuration register
- Offset: 0x1d8
- Default Value: 0x16

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VOSYS_PCLK_DIV_EN	RW	vosys_pclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1

Bits	Field Name	Access	Description
[3:0]	VOSYS_PCLK_DIV_NUM	RW	Vosys_PCLK frequency division factor 4'd6: 1:6 .... 4'd12: 1:12 Value After Reset: 0x6

4.4.2.2.46 VOSYS_ACLK_CFG

- Description: vosys_aclk REE configuration register
- Offset: 0x1dc
- Default Value: 0x33

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	VOSYS_AXI_ACLK_EN	RW	vosys_axi_aclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	VOSYS_ACLK_M_DIV_EN	RW	vosys_aclk_m's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3:0]	VOSYS_ACLK_M_DIV_NUM	RW	vosys_aclk_m's divider ratio 3'd3: 1:3 ..... 3'd7: 1:7 Value After Reset: 0x3

4.4.2.2.47 VPSYS_CLK_CFG

- Description: VPSYS_ACLK configuration register
- Offset: 0x1e0
- Default Value: 0xb312

Bits	Field Name	Access	Description
[31:16]	RESERVED_4	-	
[15]	VPSYS_AXI_ACLK_EN	RW	vpsys_axi_aclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[14]	RESERVED_3	-	
[13]	CPU2VP_X2P_CLK_EN	RW	cpu2vp_x2p_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[12]	VPSYS_AXI_ACLK_DIV_EN	RW	vpsys_axi_aclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[11:8]	VPSYS_AXI_ACLK_DIV_NUM	RW	vpsys_axi_aclk's divider ratio 3'd3: 1:3 ..... 3'd7: 1:7 Value After Reset: 0x3
[7:5]	RESERVED_2	-	
[4]	VPSYS_APB_PCLK_DIV_EN	RW	vpsys_apb_pclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3]	RESERVED_1	-	

Bits	Field Name	Access	Description
[2:0]	VPSYS_APB_PCLK_DIV_NUM	RW	vpsys_apb_pclk's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.48 VENC_CCLK_CFG

- Description: VENC CCLK configuration register
- Offset: 0x1e4
- Default Value: 0x32

Bits	Field Name	Access	Description
[31:6]	RESERVED_2	-	
[5]	VENC_CCLK_EN	RW	VENC cclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	VENC_CCLK_DIV_EN	RW	vpsys_vend_cclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3]	RESERVED_1	-	
[2:0]	VENC_CCLK_DIV_NUM	RW	vpsys_venc_cclk's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.49 DPU0_PLL_DIV_CFG

- Description: dpu0_pll_div REE configuration register
- Offset: 0x1e8
- Default Value: 0x102

Bits	Field Name	Access	Description
[31:9]	RESERVED_1	-	
[8]	DPU0_PLL_DIV_CLK_DIV_EN	RW	dpu0_pll_div_clk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[7:0]	DPU0_PLL_DIV_CLK_DIV_NUM	RW	dpu0_pll_div_clk's divider ratio 8'd2: 1:2 ..... 8'd7: 1:7 ..... Value After Reset: 0x2

4.4.2.2.50 DPU1_PLL_DIV_CFG

- Description: dpu1_pll_div REE configuration register
- Offset: 0x1ec
- Default Value: 0x102

Bits	Field Name	Access	Description
[31:9]	RESERVED_1	-	
[8]	DPU1_PLL_DIV_CLK_DIV_EN	RW	dpu1_pll_div_clk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[7:0]	DPU1_PLL_DIV_CLK_DIV_NUM	RW	dpu1_pll_div_clk's divider ratio 8'd2: 1:2 ..... 8'd7: 1:7 ..... Value After Reset: 0x2

4.4.2.2.51 PERI_I2S_SRC_CLK_CFG

- Description: PERI_I2S_SRC_CLK configuration register
- Offset: 0x1f0
- Default Value: 0x2

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	PERI_I2S_CLK_EN	RW	peri_i2s_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[0]	PERI_I2S_SRC_CLK_MUX_SEL	RW	Peripheral system I2S source clock select 0: 294.912MHz 1: 135.4752MHz Value After Reset: 0x0

4.4.2.2.52 PERI_CLK_CFG

- Description: Peripheral clock gate control register
- Offset: 0x204
- Default Value: 0x55ffffff

Bits	Field Name	Access	Description
[31]	RESERVED_4	-	
[30]	EMMC_SDIO_REF_CLK_EN	RW	eMMC SDIO reference clock enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[29]	RESERVED_3	-	
[28]	RESERVED_REG_PERI	RW	reserved_reg_peri Value After Reset: 0x1
[27]	RESERVED_2	-	
[26]	GMAC1_CLK_EN	RW	GMAC1 clock's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[25]	RESERVED_1	-	

Bits	Field Name	Access	Description
[24]	PADCTRL1_APSYS_PCLK_EN	RW	PADCTRL1 clock's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[23]	DSMART_CLK_EN	RW	dsmart_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[22]	PADCTRL0_APSYS_PCLK_EN	RW	PADCTRL0 clock's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[21]	GMAC_AXI_CLK_EN	RW	GMAC axi4_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[20]	GPIO3_CLK_EN	RW	gpio3_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[19]	GMAC0_CLK_EN	RW	gmac_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[18]	PWM_CLK_EN	RW	pwm_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[17]	QSPI0_CLK_EN	RW	qspi0_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

Bits	Field Name	Access	Description
[16]	QSPI1_CLK_EN	RW	qspi1_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[15]	SPI_CLK_EN	RW	spi_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[14]	UART0_CLK_EN	RW	uart0_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[13]	UART1_CLK_EN	RW	uart1_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[12]	UART2_CLK_EN	RW	uart2_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[11]	UART3_CLK_EN	RW	uart3_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[10]	UART4_CLK_EN	RW	uart4_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[9]	UART5_CLK_EN	RW	uart5_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

Bits	Field Name	Access	Description
[8]	GPIO0_CLK_EN	RW	gpio0_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[7]	GPIO1_CLK_EN	RW	gpio1_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[6]	GPIO2_CLK_EN	RW	gpio2_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[5]	I2C0_CLK_EN	RW	i2c0_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	I2C1_CLK_EN	RW	i2c1_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[3]	I2C2_CLK_EN	RW	i2c2_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[2]	I2C3_CLK_EN	RW	i2c3_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[1]	I2C4_CLK_EN	RW	i2c4_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

Bits	Field Name	Access	Description
[0]	I2C5_CLK_EN	RW	i2c5_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

4.4.2.2.53 CTRL_CLK_CFG

- Description: CTRL_CLK configuration register
- Offset: 0x208
- Default Value: 0x7ff

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10]	SPINLOCK_HCLK_EN	RW	spinlock_hclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[9]	CHIP_DBG_CLK_EN	RW	chip_dbg_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[8]	DMAC_CPUSYS_CLK_EN	RW	dmac_cpusys_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[7]	MBOX0_PCLK_EN	RW	mbox0_pclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[6]	MBOX1_PCLK_EN	RW	mbox1_pclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

Bits	Field Name	Access	Description
[5]	MBOX2_PCLK_EN	RW	mbox2_pclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	MBOX3_PCLK_EN	RW	mbox3_pclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[3]	WDT0_PCLK_EN	RW	wdt0's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[2]	WDT1_PCLK_EN	RW	wdt1's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[1]	TIMER0_CLK_EN	RW	ddr_cclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[0]	TIMER1_CLK_EN	RW	c910_cnt_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

4.4.2.2.54 SRAM_AXI_CLK_CFG

- Description: SRAM_AXI_CLK configuration register
- Offset: 0x20c
- Default Value: 0x1e

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	SRAM_AXI_ACLK_0_EN	RW	sram_axi_aclk_0's gate enable signal 0: Gate clock. 1: Open clock.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[3]	SRAM_AXI_ACLK_1_EN	RW	sram_axi_aclk_1's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[2]	SRAM_AXI_ACLK_2_EN	RW	sram_axi_aclk_2's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[1]	SRAM_AXI_ACLK_3_EN	RW	sram_axi_aclk_3's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[0]	RESERVED_1	-	

4.4.2.2.55 UART_SCLK_CFG

- Description: uart_aclk REE configuration register
- Offset: 0x210
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	UART_SCLK_SWITCH_SEL	RW	uart_ SCLK select 0: 100MHz 1: 24MHz Value After Reset: 0x0

4.4.2.2.56 SUBSYS_CLK_CFG

- Description: Subsystem REE configuration register
- Offset: 0x220
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	VOSYS_CLK_EN	RW	vosys_clk_en

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[1]	VISYS_CLK_EN	RW	visys_clk_en Value After Reset: 0x0
[0]	DSPSYS_CLK_EN	RW	dspsys_clk_en Value After Reset: 0x0

4.4.2.2.57 BOOT_CLK_SEL_CFG

- Description:
- Offset: 0x280
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	REG_BOOT_PAD_SEL	RW	Reserved, software can't write this field. Value After Reset: 0x0

4.4.2.2.58 TEST_CLK_CFG

- Description: TEST_CLK configuration register
- Offset: 0x300
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	TEST_CLK_SAMPLE_EN	RW	test_clk's sample enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x0
[4:0]	TEST_CLK_SEL	RW	test_clk[0]: Reserved test_clk[1]: apb3_cpusys_pclk test_clk[2]: axi4_cpusys2_aclk test_clk[3]: ahb2_cpusys_hclk test_clk[4]: axi4_cpusys1_aclk test_clk[5]: cfg_axi_aclk test_clk[6]: teesys_hclk test_clk[7]: 1'b0

Bits	Field Name	Access	Description
			test_clk[8]: perisys_ahb_hclk test_clk[9]: perisys_apb_pclk test_clk[10]: npu_cclk test_clk[11]: cfg_apb_pclk test_clk[12]: peri2sys_apb_pclk test_clk[13]: venc_cclk test_clk[14]: c910_core0_clk_div_monitor;(c910_cclk/128) test_clk[15]: c910_core1_clk_div_monitor;(c910_cclk/128) test_clk[16]: c910_core2_clk_div_monitor;(c910_cclk/128) test_clk[17]: c910_core3_clk_div_monitor;(c910_cclk/128) test_clk[18]: peri_i2s_src_clk test_clk[19]: vosys_aclk_m test_clk[20]: visys_aclk_m test_clk[21]: visys_ahb_hclk test_clk[22]: vpsys_apb_pclk test_clk[23]: vpsys_axi_aclk test_clk[24]: dpu0_pll_div_clk test_clk[25]: dpu1_pll_div_clk test_clk[31:26]: 'd0 Value After Reset: 0x0

4.4.2.2.59 TEST_CLK_STS

- Description: TEST_CLK status register
- Offset: 0x304
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	TEST_CLK_FREQ_STAT	RO	Read test clock frequency, unit: kHz Value After Reset: 0x0

4.4.2.2.60 BOOT_OSC_EN

- Description: Reserved
- Offset: 0x308
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	PAD_OSC_BOOT_EN	RO	Indicate the boot clock state. 1'b1: Boot with OSC clock. 1'b0: Boot with PLL clock. Value After Reset: 0x0

4.4.2.2.61 RESERVED_REG_0

- Description: RESERVED_REG_0
- Offset: 0x310
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_0	RW	Reserved Value After Reset: 0x0

4.4.2.2.62 RESERVED_REG_1

- Description: RESERVED_REG_1
- Offset: 0x314
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_1	RW	Reserved Value After Reset: 0x0

4.4.2.2.63 RESERVED_REG_2

- Description: RESERVED_REG_2
- Offset: 0x318
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_2	RW	Reserved Value After Reset: 0x0

4.4.2.2.64 RESERVED_REG_3

- Description: RESERVED_REG_3
- Offset: 0x31c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_3	RW	Reserved Value After Reset: 0x0

4.4.2.2.65 CPU_PLL0_TEECFG0

- Description: CPU PLL0 TEE configuration register 0
- Offset: 0x1000
- Default Value: 0x2507d01

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	
[26:24]	CPU_PLL0_POSTDIV2	RW	CPU PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x2
[23]	RESERVED_2	-	
[22:20]	CPU_PLL0_POSTDIV1	RW	CPU PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x5
[19:8]	CPU_PLL0_FBDIV	RW	CPU PLL feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode) Value After Reset: 0x7D
[7:6]	RESERVED_1	-	
[5:0]	CPU_PLL0_REFDIV	RW	CPU PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.2.66 CPU_PLL0_TEECFG1

- Description: CPU PLL0 TEE configuration register 1
- Offset: 0x1004
- Default Value: 0x3000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	
[30]	CPU_PLL0_BYPASS	RW	CPU PLL FREF is bypassed to FOUTPOSTDIV. Value After Reset: 0x0
[29]	CPU_PLL0_RST	RW	CPU PLL VCO rate output clock power down Value After Reset: 0x0

Bits	Field Name	Access	Description
[28]	CPU_PLL0_FOUTPOSTDIVPD	RW	CPU PLL post divide power down Value After Reset: 0x0
[27]	CPU_PLL0_FOUT4PHASEPD	RW	CPU PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	
[25]	CPU_PLL0_DACPD	RW	Power down noise cancelling DAC in FRAC mode 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x1
[24]	CPU_PLL0_DSMPD	RW	CPU PLL power down Delta-Sigma modulator 0x1: Integer mode, DSM is powered down. 0x0: Fractional mode, DSM is active. Value After Reset: 0x1
[23:0]	CPU_PLL0_FRAC	RW	CPU PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.2.67 CPU_PLL0_TEECFG2

- Description: CPU PLL0 TEE configuration register 2
- Offset: 0x1008
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	CPU_PLL0_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0
[29]	CPU_PLL0_DSKEWCALBYP	RW	Anti-skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	CPU_PLL0_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled.

Bits	Field Name	Access	Description
			1: Enable skew calibration. Value After Reset: 0x0
[27]	CPU_PLL0_DSKEWFASTCAL	RW	Anti-skew quick calibration enable Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0
[26:24]	CPU_PLL0_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default value of 3'd2. Value After Reset: 0x2
[23:12]	CPU_PLL0_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration sequence. Value After Reset: 0x0
[11:0]	CPU_PLL0_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.2.68 CPU_PLL0_TEECFG3

- Description: CPU PLL0 TEE configuration register 3
- Offset: 0x100c
- Default Value: 0x7fff400

Bits	Field Name	Access	Description
[31:12]	CPU_PLL0_CALLOCK_CNT	RW	Offset calibration lock count, received from register, quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	

Bits	Field Name	Access	Description
[10]	CPU_PLL0_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1
[9]	CPU_PLL0_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit. Value After Reset: 0x0
[8]	CPU_PLL0_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the calibration circuit can be bypassed. Value After Reset: 0x0
[7]	CPU_PLL0_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	
[3:0]	CPU_PLL0_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.2.69 CPU_PLL1_TEECFG0

- Description: CPU PLL1 TEE configuration register 0
- Offset: 0x1010
- Default Value: 0x2507d01

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	
[26:24]	CPU_PLL1_POSTDIV2	RW	CPU PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x2
[23]	RESERVED_2	-	
[22:20]	CPU_PLL1_POSTDIV1	RW	CPU PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x5
[19:8]	CPU_PLL1_FBDIV	RW	CPU PLL feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode) Value After Reset: 0x7D
[7:6]	RESERVED_1	-	
[5:0]	CPU_PLL1_REFDIV	RW	CPU PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.2.70 CPU_PLL1_TEECFG1

- Description: CPU PLL1 TEE configuration register 1
- Offset: 0x1014
- Default Value: 0x3000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	
[30]	CPU_PLL1_BYPASS	RW	CPU PLL FREF is bypassed to FOUTPOSTDIV. Value After Reset: 0x0
[29]	CPU_PLL1_RST	RW	CPU PLL clock power down control, active high Value After Reset: 0x0
[28]	CPU_PLL1_FOUTPOSTDIVPD	RW	CPU PLL post divide power down Value After Reset: 0x0
[27]	CPU_PLL1_FOUT4PHASEPD	RW	CPU PLL phase-shifter clock power-down control

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[26]	RESERVED_1	-	
[25]	CPU_PLL1_DACPD	RW	Power down noise cancelling DAC in FRAC mode 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x1
[24]	CPU_PLL1_DSMPD	RW	CPU PLL power down Delta-Sigma modulator 0x1: Integer mode, DSM is powered down. 0x0: Fractional mode, DSM is active. Value After Reset: 0x1
[23:0]	CPU_PLL1_FRAC	RW	CPU PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.2.71 CPU_PLL1_TEECFG2

- Description: CPU PLL1 TEE configuration register 2
- Offset: 0x1018
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	CPU_PLL1_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0
[29]	CPU_PLL1_DSKEWCALBYP	RW	Anti-skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	CPU_PLL1_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled. 1: Enable skew calibration. Value After Reset: 0x0
[27]	CPU_PLL1_DSKEWFASTCAL	RW	Anti-skew quick calibration enable

Bits	Field Name	Access	Description
			Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0
[26:24]	CPU_PLL1_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default value of 3'd2. Value After Reset: 0x2
[23:12]	CPU_PLL1_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration sequence. Value After Reset: 0x0
[11:0]	CPU_PLL1_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.2.72 CPU_PLL1_TEECFG3

- Description: CPU PLL1 TEE configuration register 3
- Offset: 0x101c
- Default Value: 0x7fff400

Bits	Field Name	Access	Description
[31:12]	CPU_PLL1_CALLOCK_CNT	RW	Offset calibration lock count, received from register, quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	CPU_PLL1_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the

Bits	Field Name	Access	Description
			counting method to determine whether the calibration is locked. Value After Reset: 0x1
[9]	CPU_PLL1_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit. Value After Reset: 0x0
[8]	CPU_PLL1_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the calibration circuit can be bypassed. Value After Reset: 0x0
[7]	CPU_PLL1_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	
[3:0]	CPU_PLL1_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.2.73 GMAC_PLL_TEECFG0

- Description: GMAC PLL TEE configuration register 0
- Offset: 0x1020
- Default Value: 0x1307d01

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	
[26:24]	GMAC_PLL_POSTDIV2	RW	GMAC PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x1
[23]	RESERVED_2	-	
[22:20]	GMAC_PLL_POSTDIV1	RW	GMAC PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x3
[19:8]	GMAC_PLL_FBDIV	RW	GMAC PLL feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode) Value After Reset: 0x7D
[7:6]	RESERVED_1	-	
[5:0]	GMAC_PLL_REFDIV	RW	GMAC PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.2.74 GMAC_PLL_TEECFG1

- Description: GMAC PLL TEE configuration register 1
- Offset: 0x1024
- Default Value: 0x3000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	
[30]	GMAC_PLL_BYPASS	RW	GMAC PLL clock power down control, active high Value After Reset: 0x0
[29]	GMAC_PLL_RST	RW	GMAC PLL VCO rate output clock power down Value After Reset: 0x0
[28]	GMAC_PLL_FOUTPOSTDIVPD	RW	GMAC PLL post divide power down Value After Reset: 0x0
[27]	GMAC_PLL_FOUT4PHASEPD	RW	GMAC PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	
[25]	GMAC_PLL_DACPD	RW	Power down noise cancelling DAC in FRAC mode 0: DAC is active. (default mode)

Bits	Field Name	Access	Description
			1: DAC is not active. (test mode only) Value After Reset: 0x1
[24]	GMAC_PLL_DSMPD	RW	CPU PLL power down Delta-Sigma modulator 0x1: Integer mode, DSM is powered down. 0x0: Fractional mode, DSM is active. Value After Reset: 0x1
[23:0]	GMAC_PLL_FRAC	RW	GMAC PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.2.75 GMAC_PLL_TEECFG2

- Description: GMAC PLL TEE configuration register 2
- Offset: 0x1028
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	GMAC_PLL_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0
[29]	GMAC_PLL_DSKEWCALBYP	RW	Anti-skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	GMAC_PLL_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled. 1: Enable skew calibration. Value After Reset: 0x0
[27]	GMAC_PLL_DSKEWFASTCAL	RW	Anti-skew quick calibration enable Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0
[26:24]	GMAC_PLL_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew

Bits	Field Name	Access	Description
			calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default value of 3'd2. Value After Reset: 0x2
[23:12]	GMAC_PLL_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration sequence. Value After Reset: 0x0
[11:0]	GMAC_PLL_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.2.76 GMAC_PLL_TEECFG3

- Description: GMAC PLL TEE configuration register 3
- Offset: 0x102c
- Default Value: 0x7fff400

Bits	Field Name	Access	Description
[31:12]	GMAC_PLL_CALLOCK_CNT	RW	Offset calibration lock count, received from register, quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	GMAC_PLL_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1
[9]	GMAC_PLL_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal

Bits	Field Name	Access	Description
			synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit. Value After Reset: 0x0
[8]	GMAC_PLL_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the calibration circuit can be bypassed. Value After Reset: 0x0
[7]	GMAC_PLL_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	
[3:0]	GMAC_PLL_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.2.77 VIDEO_PLL_TEECFG0

- Description: Video PLL TEE configuration register 0
- Offset: 0x1030
- Default Value: 0x1306301

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	
[26:24]	VIDEO_PLL_POSTDIV2	RW	Video PLL post divide 2 setting (1 to 7)

Bits	Field Name	Access	Description
			Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x1
[23]	RESERVED_2	-	
[22:20]	VIDEO_PLL_POSTDIV1	RW	Video PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x3
[19:8]	VIDEO_PLL_FBDIV	RW	Video PLL feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode) Value After Reset: 0x63
[7:6]	RESERVED_1	-	
[5:0]	VIDEO_PLL_REFDIV	RW	Video PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.2.78 VIDEO_PLL_TEECFG1

- Description: Video PLL TEE configuration register 1
- Offset: 0x1034
- Default Value: 0x3000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	
[30]	VIDEO_PLL_BYPASS	RW	Video PLL clock power down control, active high Value After Reset: 0x0
[29]	VIDEO_PLL_RST	RW	Video PLL VCO rate output clock power down Value After Reset: 0x0
[28]	VIDEO_PLL_FOUTPOSTDIVPD	RW	Video PLL post divide power down Value After Reset: 0x0
[27]	VIDEO_PLL_FOUT4PHASEPD	RW	Video PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	
[25]	VIDEO_PLL_DACPD	RW	Power down noise cancelling DAC in FRAC mode 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x1

Bits	Field Name	Access	Description
[24]	VIDEO_PLL_DSMPD	RW	CPU PLL power down Delta-Sigma modulator 0x1: Integer mode, DSM is powered down. 0x0: Fractional mode, DSM is active. Value After Reset: 0x1
[23:0]	VIDEO_PLL_FRAC	RW	Video PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.2.79 VIDEO_PLL_TEECFG2

- Description: Video PLL TEE configuration register 2
- Offset: 0x1038
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	VIDEO_PLL_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0
[29]	VIDEO_PLL_DSKEWCALBYP	RW	Anti-skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	VIDEO_PLL_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled. 1: Enable skew calibration. Value After Reset: 0x0
[27]	VIDEO_PLL_DSKEWFASTCAL	RW	Anti-skew quick calibration enable Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0
[26:24]	VIDEO_PLL_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default

Bits	Field Name	Access	Description
			value of 3'd2. Value After Reset: 0x2
[23:12]	VIDEO_PLL_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration sequence. Value After Reset: 0x0
[11:0]	VIDEO_PLL_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.2.80 VIDEO_PLL_TEECFG3

- Description: Video PLL TEE configuration register 3
- Offset: 0x103c
- Default Value: 0x7fff400

Bits	Field Name	Access	Description
[31:12]	VIDEO_PLL_CALLOCK_CNT	RW	Offset calibration lock count, received from register, quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	VIDEO_PLL_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1
[9]	VIDEO_PLL_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[8]	VIDEO_PLL_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the calibration circuit can be bypassed. Value After Reset: 0x0
[7]	VIDEO_PLL_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	
[3:0]	VIDEO_PLL_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.2.81 DPU0_PLL_TEECFG0

- Description: DPU0 PLL TEE configuration register 0
- Offset: 0x1040
- Default Value: 0x1206301

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	
[26:24]	DPU0_PLL_POSTDIV2	RW	DPU0 PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x1
[23]	RESERVED_2	-	

Bits	Field Name	Access	Description
[22:20]	DPU0_PLL_POSTDIV1	RW	DPU0 PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x2
[19:8]	DPU0_PLL_FBDIV	RW	DPU0 PLL feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode) Value After Reset: 0x63
[7:6]	RESERVED_1	-	
[5:0]	DPU0_PLL_REFDIV	RW	DPU0 PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.2.82 DPU0_PLL_TEECFG1

- Description: DPU0 PLL TEE configuration register 1
- Offset: 0x1044
- Default Value: 0x3000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	
[30]	DPU0_PLL_BYPASS	RW	DPU0 PLL clock power down control, active high Value After Reset: 0x0
[29]	DPU0_PLL_RST	RW	DPU0 PLL VCO rate output clock power down, active high Value After Reset: 0x0
[28]	DPU0_PLL_FOUTPOSTDIVPD	RW	DPU0 PLL post divide power down Value After Reset: 0x0
[27]	DPU0_PLL_FOUT4PHASEPD	RW	DPU0 PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	
[25]	DPU0_PLL_DACPD	RW	Power down noise cancelling DAC in FRAC mode. 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x1
[24]	DPU0_PLL_DSMPD	RW	CPU PLL power down Delta-Sigma modulator 0x1: Integer mode, DSM is powered down. 0x0: Fractional mode, DSM is active.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[23:0]	DPU0_PLL_FRAC	RW	DPU0 PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.2.83 DPU0_PLL_TEECFG2

- Description: DPU0 PLL TEE configuration register 2
- Offset: 0x1048
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	DPU0_PLL_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0
[29]	DPU0_PLL_DSKEWCALBYP	RW	Anti-skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	DPU0_PLL_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled. 1: Enable skew calibration. Value After Reset: 0x0
[27]	DPU0_PLL_DSKEWFASTCAL	RW	Anti-skew quick calibration enable Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0
[26:24]	DPU0_PLL_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default value of 3'd2. Value After Reset: 0x2

Bits	Field Name	Access	Description
[23:12]	DPU0_PLL_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration sequence. Value After Reset: 0x0
[11:0]	DPU0_PLL_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.2.84 DPU0_PLL_TEECFG3

- Description: DPU0 PLL TEE configuration register 3
- Offset: 0x104c
- Default Value: 0x7fff400

Bits	Field Name	Access	Description
[31:12]	DPU0_PLL_CALLOCK_CNT	RW	Offset calibration lock count, received from register, quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	DPU0_PLL_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1
[9]	DPU0_PLL_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit. Value After Reset: 0x0

Bits	Field Name	Access	Description
[8]	DPU0_PLL_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the calibration circuit can be bypassed. Value After Reset: 0x0
[7]	DPU0_PLL_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	
[3:0]	DPU0_PLL_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.2.85 DPU1_PLL_TEECFG0

- Description: DPU1 PLL TEE configuration register 0
- Offset: 0x1050
- Default Value: 0x1206301

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	
[26:24]	DPU1_PLL_POSTDIV2	RW	DPU1 PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x1
[23]	RESERVED_2	-	
[22:20]	DPU1_PLL_POSTDIV1	RW	DPU1 PLL post divide 1 setting (1 to 7)

Bits	Field Name	Access	Description
			Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x2
[19:8]	DPU1_PLL_FBDIV	RW	DPU1 PLL feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode) Value After Reset: 0x63
[7:6]	RESERVED_1	-	
[5:0]	DPU1_PLL_REFDIV	RW	DPU1 PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.2.86 DPU1_PLL_TEECFG1

- Description: DPU1 PLL TEE configuration register 1
- Offset: 0x1054
- Default Value: 0x3000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	
[30]	DPU1_PLL_BYPASS	RW	DPU1 PLL clock power down control, active high Value After Reset: 0x0
[29]	DPU1_PLL_RST	RW	DPU1 PLL VCO rate output clock power down Value After Reset: 0x0
[28]	DPU1_PLL_FOUTPOSTDIVPD	RW	DPU1 PLL post divide power down Value After Reset: 0x0
[27]	DPU1_PLL_FOUT4PHASEPD	RW	DPU1 PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	
[25]	DPU1_PLL_DACPD	RW	Power down noise cancelling DAC in FRAC mode 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x1
[24]	DPU1_PLL_DSMPD	RW	CPU PLL power down Delta-Sigma modulator 0x1: Integer mode, DSM is powered down. 0x0: Fractional mode, DSM is active. Value After Reset: 0x1
[23:0]	DPU1_PLL_FRAC	RW	DPU1 PLL fractional portion of feedback divide value

Bits	Field Name	Access	Description
			Value After Reset: 0x0

4.4.2.2.87 DPU1_PLL_TEECFG2

- Description: DPU1 PLL TEE configuration register 2
- Offset: 0x1058
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	DPU1_PLL_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0
[29]	DPU1_PLL_DSKEWCALBYP	RW	Anti-skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	DPU1_PLL_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled. 1: Enable skew calibration. Value After Reset: 0x0
[27]	DPU1_PLL_DSKEWFASTCAL	RW	Anti-skew quick calibration enable Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0
[26:24]	DPU1_PLL_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default value of 3'd2. Value After Reset: 0x2
[23:12]	DPU1_PLL_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration

Bits	Field Name	Access	Description
			sequence. Value After Reset: 0x0
[11:0]	DPU1_PLL_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.2.88 DPU1_PLL_TEECFG3

- Description: DPU1 PLL TEE configuration register 3
- Offset: 0x105c
- Default Value: 0x7fff400

Bits	Field Name	Access	Description
[31:12]	DPU1_PLL_CALLOCK_CNT	RW	Offset calibration lock count, received from register, quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	DPU1_PLL_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1
[9]	DPU1_PLL_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit. Value After Reset: 0x0
[8]	DPU1_PLL_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control

Bits	Field Name	Access	Description
			the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the calibration circuit can be bypassed. Value After Reset: 0x0
[7]	DPU1_PLL_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	
[3:0]	DPU1_PLL_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.2.89 TEE_PLL_TEECFG0

- Description: TEE PLL TEE configuration register 0
- Offset: 0x1060
- Default Value: 0x1306301

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	
[26:24]	TEE_PLL_POSTDIV2	RW	TEE PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x1
[23]	RESERVED_2	-	
[22:20]	TEE_PLL_POSTDIV1	RW	TEE PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x3
[19:8]	TEE_PLL_FBDIV	RW	TEE PLL feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode)

Bits	Field Name	Access	Description
			Value After Reset: 0x63
[7:6]	RESERVED_1	-	
[5:0]	TEE_PLL_REFDIV	RW	TEE PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.2.90 TEE_PLL_TEECFG1

- Description: TEE PLL TEE configuration register 1
- Offset: 0x1064
- Default Value: 0x63000000

Bits	Field Name	Access	Description
[31]	RESERVED_2	-	
[30]	TEE_PLL_BYPASS	RW	TEE PLL clock power down control, active high Value After Reset: 0x1
[29]	TEE_PLL_RST	RW	TEE PLL VCO rate output clock power down Value After Reset: 0x1
[28]	TEE_PLL_FOUTPOSTDIVPD	RW	TEE PLL post divide power down Value After Reset: 0x0
[27]	TEE_PLL_FOUT4PHASEPD	RW	TEE PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	
[25]	TEE_PLL_DACPD	RW	Power down noise cancelling DAC in FRAC mode 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x1
[24]	TEE_PLL_DSMPD	RW	CPU PLL power down Delta-Sigma modulator 0x1: Integer mode, DSM is powered down. 0x0: Fractional mode, DSM is active. Value After Reset: 0x1
[23:0]	TEE_PLL_FRAC	RW	TEE PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.2.91 TEE_PLL_TEECFG2

- Description: TEE PLL TEE configuration register 2

- Offset: 0x1068
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	TEE_PLL_DSKEWCALLOCK	RO	When dskewcalen is set to 1, the signal is pulled high to indicate phase locking. Value After Reset: 0x0
[29]	TEE_PLL_DSKEWCALBYP	RW	Anti-skew calibration bypass 0: Use the skew calibration output to correct the phase. (when dskewcalen is 1) 1: Use the value of dskewcalin[11:0] to correct the phase. (when dskewcalen is 1) Value After Reset: 0x0
[28]	TEE_PLL_DSKEWCALEN	RW	The anti-skew enable signal is used to adjust the input skew. 0: Skew calibration is not enabled. 1: Enable skew calibration. Value After Reset: 0x0
[27]	TEE_PLL_DSKEWFASTCAL	RW	Anti-skew quick calibration enable Set to 1 for initial calibration if the initial value is unknown. Set to 0 in normal working mode. Value After Reset: 0x0
[26:24]	TEE_PLL_DSKEWCALCNT	RW	Programmable counter for anti-skew calibration ring Wait for several PFD edges after each anti-skew calibration, with a count of 2**DSKEWCALCNT+5 (if DSKEWCALCNT is 3'd5, then 1024 PFD cycles will be waited before starting a new setup), with a default value of 3'd2. Value After Reset: 0x2
[23:12]	TEE_PLL_DSKEWCALIN	RW	If DSKEWCALEN is 1, a skew correction value can be forced into the calibration logic based on the previously read DSKEWCALOUT[11:0]; If DSKEWCALEN is 0, the value is the initial state of the calibration sequence. Value After Reset: 0x0
[11:0]	TEE_PLL_DSKEWCALOUT	RO	Skew calibration circuit (dskewcalbyp = 0) or dskewcalin[11:0] cache (dskewcalbyp = 1) output. It can be used to read out the phase calibration status

Bits	Field Name	Access	Description
			and bypass the skew calibration as the value of dskewcalin[11:0]. Value After Reset: 0x0

4.4.2.2.92 TEE_PLL_TEECFG3

- Description: TEE PLL TEE configuration register 3
- Offset: 0x106c
- Default Value: 0x7fff500

Bits	Field Name	Access	Description
[31:12]	TEE_PLL_CALLOCK_CNT	RW	Offset calibration lock count, received from register, quasi-static signal, default is 20 'b7fff. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	TEE_PLL_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the calllock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1
[9]	TEE_PLL_DSKEWCAL_PULSE	W1S	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default. When the offset calibration software enable is invalid, write 1 to start the PLL calibration circuit. Value After Reset: 0x0
[8]	TEE_PLL_DSKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. When used for frequency modulation, if the PFD is changed (for example, the PFD is too small), resulting in the unavailability of the calibration circuit, the

Bits	Field Name	Access	Description
			calibration circuit can be bypassed. Value After Reset: 0x1
[7]	TEE_PLL_DSKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	
[3:0]	TEE_PLL_DSKEWCAL_STAT	RO	Hardware calibration state machine state, used for debugging. 0: IDLE 1: START 2: LOCK 3: CALIN 4: DISABLE Value After Reset: 0x0

4.4.2.2.93 PLL_TEESTS

- Description: All PLLs' status register
- Offset: 0x1080
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10]	TEE_PLL_LOCK	RO	TEE PLL frequency locked status Value After Reset: 0x0
[9]	DPU1_PLL_LOCK	RO	DPU1 PLL frequency locked status Value After Reset: 0x0
[8]	DPU0_PLL_LOCK	RO	DPU0 PLL frequency locked status Value After Reset: 0x0
[7]	VIDEO_PLL_LOCK	RO	Video PLL frequency locked status Value After Reset: 0x0
[6]	SYS_PLL_LOCK	RO	System PLL frequency locked status Value After Reset: 0x0
[5]	AUDIO_PLL_LOCK	RO	Audio PLL frequency locked status Value After Reset: 0x0

Bits	Field Name	Access	Description
[4]	CPU_PLL1_LOCK	RO	CPU PLL1 frequency locked status Value After Reset: 0x0
[3]	GMAC_PLL_LOCK	RO	GMAC PLL frequency locked status Value After Reset: 0x0
[2]	DDR_PLL_LOCK	RO	DDR PLL frequency locked status Value After Reset: 0x0
[1]	CPU_PLL0_LOCK	RO	CPU PLL0 frequency locked status Value After Reset: 0x0
[0]	ALL_PLL_LOCK	RO	All PLLs' frequency locked status Value After Reset: 0x0

4.4.2.2.94 C910_CLK_TEECFG

- Description: C910 clock configuration register
- Offset: 0x1100
- Default Value: 0x9f0

Bits	Field Name	Access	Description
[31:12]	RESERVED_2	-	
[11]	C910_BUS_CLK_SYNC	RW	c910_bus_clk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[10:8]	C910_BUS_CLK_RATIO	RW	c910_bus_clk's divider ratio 3'd1: 1:2 3'd2: 1:3 ..... 3'd7: 1:8 Value After Reset: 0x1
[7]	C910_BUS_CLK_EN	RW	c910_bus_clk's gate enable signal 0: Gate clock. 1: Open clock.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[6]	C910_CLK_EN	RW	c910_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[5]	BMU_C910_CLK_EN	RW	bmu_c910_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	C910_BROM_HCLK_EN	RW	c910_brom_hclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[3:2]	RESERVED_1	-	
[1]	C910_CCLK_I0_SWITCH_SEL	RW	c910_cclk_i0 clock select 0: PLL0 1: OSC_CLK Value After Reset: 0x0
[0]	C910_CCLK_SWITCH_SEL	RW	c910_cclk clock select 0: c910_cclk_i0 1: PLL1 Value After Reset: 0x0

4.4.2.2.95 C910_CORE_CLK_TEECFG

- Description: C910 core clock configuration register
- Offset: 0x1104
- Default Value: 0x30303030

Bits	Field Name	Access	Description
[31:30]	RESERVED_4	-	
[29]	C910_CORE3_CLK_EN	RW	c910_core3_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

Bits	Field Name	Access	Description
[28]	C910_CORE3_CLK_DIV_EN	RW	c910_core3_clk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[27:24]	C910_CORE3_CLK_DIV_NUM	RW	c910_core3_clk's divider ratio 3'd0: 1:1 3'd1: 1:2 ..... 3'd6: 1:7 3'd7: 1:8 Value After Reset: 0x0
[23:22]	RESERVED_3	-	
[21]	C910_CORE2_CLK_EN	RW	c910_core2_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[20]	C910_CORE2_CLK_DIV_EN	RW	c910_core2_clk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[19:16]	C910_CORE2_CLK_DIV_NUM	RW	c910_core2_clk's divider ratio 3'd0: 1:1 3'd1: 1:2 ..... 3'd6: 1:7 3'd7: 1:8 Value After Reset: 0x0
[15:14]	RESERVED_2	-	

Bits	Field Name	Access	Description
[13]	C910_CORE1_CLK_EN	RW	c910_core1_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[12]	C910_CORE1_CLK_DIV_EN	RW	c910_core1_clk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[11:8]	C910_CORE1_CLK_DIV_NUM	RW	c910_core1_clk's divider ratio 3'd0: 1:1 3'd1: 1:2 ..... 3'd6: 1:7 3'd7: 1:8 Value After Reset: 0x0
[7:6]	RESERVED_1	-	
[5]	C910_CORE0_CLK_EN	RW	c910_core0_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	C910_CORE0_CLK_DIV_EN	RW	c910_core0_clk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3:0]	C910_CORE0_CLK_DIV_NUM	RW	c910_core0_clk's divider ratio 3'd0: 1:1 3'd1: 1:2 .....

Bits	Field Name	Access	Description
			3'd6: 1:7 3'd7: 1:8 Value After Reset: 0x0

4.4.2.2.96 AHB2_CPUSYS_HCLK_TEECFG

- Description: AHB2_CPUSYS_HCLK configuration register
- Offset: 0x1120
- Default Value: 0xd4

Bits	Field Name	Access	Description
[31:8]	RESERVED_2	-	
[7]	X2H_CPUSYS_CLK_EN	RW	Reserved, software can't write this field. Value After Reset: 0x1
[6]	AHB2_CPUSYS_HCLK_EN	RW	Reserved, software can't write this field. Value After Reset: 0x1
[5]	AHB2_CPUSYS_HCLK_SWITCH_SEL	RW	ahb2_cpusys_hclk clock select 0: PLL 1: OSC_CLK Value After Reset: 0x0
[4]	AHB2_CPUSYS_HCLK_DIV_EN	RW	ahb2_cpusys_hclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3]	RESERVED_1	-	
[2:0]	AHB2_CPUSYS_HCLK_DIV_NUM	RW	ahb2_cpusys_hclk's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x4

4.4.2.2.97 APB3_CPUSYS_PCLK_TEECFG

- Description: APB3_CPUSYS_PCLK configuration register
- Offset: 0x1130
- Default Value: 0x18

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	APB3_CPUSYS_HCLK_EN	RW	Reserved, software can't write this field. Value After Reset: 0x1
[3]	APB3_CPUSYS_PCLK_CDE_SYNC	RW	apb3_cpusys_hclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[2:0]	APB3_CPUSYS_PCLK_CDE_RATIO	RW	apb3_cpusys_hclk's divider ratio 3'd1: 1:2 3'd2: 1:3 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.2.98 AXI4_CPUSYS_ACLK_TEECFG

- Description: AXI4_CPUSYS2_ACLK configuration register
- Offset: 0x1134
- Default Value: 0x1b2

Bits	Field Name	Access	Description
[31:9]	RESERVED_3	-	
[8]	AON2CPU_A2X_CLK_EN	RW	aon2cpu_a2x_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[7]	X2X_CPUSYS_CLK_EN	RW	x2x_cpusys_clk's gate enable signal 0: Gate clock.

Bits	Field Name	Access	Description
			1: Open clock. Value After Reset: 0x1
[6]	RESERVED_2	-	
[5]	AXI4_CPUSYS2_CLK_EN	RW	Reserved, software can't write this field. Value After Reset: 0x1
[4]	AXI4_CPUSYS2_ACLK_DIV_EN	RW	axi4_cpusys2_clk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3]	RESERVED_1	-	
[2:0]	AXI4_CPUSYS2_ACLK_DIV_NUM	RW	axi4_cpusys2_clk's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.99 CFG_AXI_ACLK_TEECFG

- Description: CFG_AXI_ACLK configuration register
- Offset: 0x1138
- Default Value: 0x112

Bits	Field Name	Access	Description
[31:9]	RESERVED_2	-	
[8]	CPU2AON_X2H_CLK_EN	RW	cpu2aon_x2h_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[7:6]	RESERVED_1	-	
[5]	CFG_AXI_ACLK_SWITCH_SEL	RW	cfg_axi_aclk clock choose 0: PLL 1: OSC_CLK

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[4]	CFG_AXI_ACLK_DIV_EN	RW	cfg_axi_aclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3:0]	CFG_AXI_ACLK_DIV_NUM	RW	cfg_axi_aclk's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.100 PERISYS_AHB_HCLK_TEECFG

- Description: PERISYS_AHB_HCLK configuration register
- Offset: 0x1140
- Default Value: 0x258

Bits	Field Name	Access	Description
[31:10]	RESERVED_2	-	
[9]	CPU2PERI_X2H_CLK_EN	RW	cpu2peri_x2h_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[8:7]	RESERVED_1	-	
[6]	PERISYS_AHB_HCLK_EN	RW	perisys_ahb_hclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[5]	PERISYS_AHB_HCLK_SWITCH_SEL	RW	perisys_ahb_hclk clock choose 0: PLL 1: OSC_CLK Value After Reset: 0x0
[4]	PERISYS_AHB_HCLK_DIV_EN	RW	perisys_ahb_hclk's divider enable. To enable

Bits	Field Name	Access	Description
			frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3:0]	PERISYS_AHB_HCLK_DIV_NUM	RW	perisys_ahb_hclk's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x8

4.4.2.2.101 PERISYS_APB_PCLK_TEECFG

- Description: PERISYS PCLK configuration register
- Offset: 0x1150
- Default Value: 0x1f28

Bits	Field Name	Access	Description
[31:13]	RESERVED_2	-	
[12]	PERISYS_APB4_HCLK_EN	RW	perisys_apb4_hclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[11]	PERISYS_APB3_HCLK_EN	RW	perisys_apb3_hclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[10]	PERISYS_APB2_HCLK_EN	RW	perisys_apb2_hclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[9]	PERISYS_APB1_HCLK_EN	RW	perisys_apb1_hclk's gate enable signal 0: Gate clock. 1: Open clock.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[8]	PERI2SYS_APB_PCLK_DIV_EN	RW	peri2sys_apb_pclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[7]	RESERVED_1	-	
[6:4]	PERI2SYS_APB_PCLK_DIV_NUM	RW	peri2sys_apb_pclk's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2
[3]	PERISYS_APB_PCLK_CDE_SYNC	RW	perisys_pclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[2:0]	PERISYS_APB_PCLK_CDE_RATIO	RW	perisys_pclk's divider ratio 3'd3: 1:4 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.2.102 CLK_OUT_1_TEECFG

- Description: Sensor clock configuration register
- Offset: 0x11b4
- Default Value: 0x2a

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	

Bits	Field Name	Access	Description
[5]	CLK_OUT_1_CLK_EN	RW	Sensor clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	CLK_OUT_1_MUX_SEL	RW	Sensor clock select 0: 24MHz 1: 12MHz divider Value After Reset: 0x0
[3]	CLK_OUT_1_DIV_EN	RW	Sensor clock's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[2:0]	CLK_OUT_1_DIV_NUM	RW	sensor clock 's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.103 CLK_OUT_2_TEECFG

- Description: Sensor clock configuration register
- Offset: 0x11b8
- Default Value: 0x2a

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	CLK_OUT_2_CLK_EN	RW	Sensor clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	CLK_OUT_2_MUX_SEL	RW	Sensor clock select 0: 24MHz 1: 12MHz divider

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[3]	CLK_OUT_2_DIV_EN	RW	Sensor clock's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[2:0]	CLK_OUT_2_DIV_NUM	RW	Sensor clock's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.104 CLK_OUT_3_TEECFG

- Description: Sensor clock configuration register
- Offset: 0x11bc
- Default Value: 0x2a

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	CLK_OUT_3_CLK_EN	RW	Sensor clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	CLK_OUT_3_MUX_SEL	RW	Sensor clock select 0: 24MHz 1: 12MHz divider Value After Reset: 0x0
[3]	CLK_OUT_3_DIV_EN	RW	Sensor clock's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[2:0]	CLK_OUT_3_DIV_NUM	RW	Sensor clock's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.105 CLK_OUT_4_TEECFG

- Description: Sensor clock configuration register
- Offset: 0x11c0
- Default Value: 0x2a

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	CLK_OUT_4_CLK_EN	RW	Sensor clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	CLK_OUT_4_MUX_SEL	RW	Sensor clock select 0: 24MHz 1: 12MHz divider Value After Reset: 0x0
[3]	CLK_OUT_4_DIV_EN	RW	Sensor clock's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[2:0]	CLK_OUT_4_DIV_NUM	RW	Sensor clock's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.106 CFG_APB_PCLK_TEECFG

- Description: cfg_apb_pclk TEE configuration register
- Offset: 0x11c4
- Default Value: 0x34

Bits	Field Name	Access	Description
[31:8]	RESERVED_2	-	
[7]	CFG_APB_PCLK_SWITCH_SEL	RW	cfg_apb_pclk_switch_sel Value After Reset: 0x0
[6]	RESERVED_1	-	
[5]	APB_CPU2CFG_HCLK_EN	RW	apb_cpu2cfg_hclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	CFG_APB_PCLK_DIV_EN	RW	cfg_apb_pclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3:0]	CFG_APB_PCLK_DIV_NUM	RW	cfg_apb_pclk's divider ratio 4'd4: 1:4 ..... 4'd15: 1:15 Value After Reset: 0x4

4.4.2.2.107 NPU_CCLK_TEECFG

- Description: npu_cclk TEE configuration register
- Offset: 0x11c8
- Default Value: 0xb

Bits	Field Name	Access	Description
[31:7]	RESERVED_1	-	
[6]	NPU_CCLK_SWITCH_SEL	RW	0: 1000M 1: The maximum frequency is 792. Can be changed by configuring bit [3:0].

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[5]	NPU_AXI_ACLK_EN	RW	npu_axi_aclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x0
[4]	NPU_CORE_CLK_EN	RW	npu_core_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x0
[3]	NPU_CCLK_DIV_EN	RW	npu_cclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[2:0]	NPU_CCLK_DIV_NUM	RW	npu_cclk's divider ratio 3'd3: 1:3 ..... 3'd7: 1:7 Value After Reset: 0x3

4.4.2.2.108 TEESYS_CLK_TEECFG

- Description: teesys_clk TEE configuration register
- Offset: 0x11cc
- Default Value: 0x3003414

Bits	Field Name	Access	Description
[31:26]	RESERVED_3	-	
[25]	TEESYS_CCLK_EN	RW	teesys_cclk_en Value After Reset: 0x1
[24]	CFG2TEE_X2H_CLK_EN	RW	cfg2tee_x2h_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

Bits	Field Name	Access	Description
[23:14]	RESERVED_2	-	
[13]	TEESYS_HCLK_SWITCH_SEL	RW	teesys_hclk clock select 0: tee_pll_foutpostdiv 1: video_pll_foutpostdiv Value After Reset: 0x1
[12]	TEESYS_I1_HCLK_DIV_EN	RW	teesys_i1_hclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[11:8]	TEESYS_I1_HCLK_DIV_NUM	RW	teesys_i1_hclk's divider ratio 3'd2: 1:2 ..... 3'd7: :7 Value After Reset: 0x4
[7:5]	RESERVED_1	-	
[4]	TEESYS_I0_HCLK_DIV_EN	RW	teesys_i0_hclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3:0]	TEESYS_I0_HCLK_DIV_NUM	RW	Teesys_I0_Hclk frequency division factor 4'd2: 1:2 .... 4'd15: 1:15 Value After Reset: 0x4

4.4.2.2.109 VISYS_CLK_TEECFG

- Description: visys_clk TEE configuration register
- Offset: 0x11d0
- Default Value: 0x330016

Bits	Field Name	Access	Description
[31:22]	RESERVED_2	-	
[21]	CPU2VI_X2H_CLK_EN	RW	cpu2vi_x2h_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[20]	VISYS_ACLK_M_DIV_EN	RW	visys_aclk_m's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[19:16]	VISYS_ACLK_M_DIV_NUM	RW	visys_aclk_m's divider ratio 3'd3: 1:3 ..... 3'd7: 1:7 Value After Reset: 0x3
[15:5]	RESERVED_1	-	
[4]	VISYS_AHB_HCLK_DIV_EN	RW	visys_ahb_hclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3:0]	VISYS_AHB_HCLK_DIV_NUM	RW	visys_ahb_hclk's divider ratio 4'd6: 1:6 ..... 4'd15: 1:15 Value After Reset: 0x6

4.4.2.2.110 VOSYS_PCLK_TEECFG

- Description: vosys_pclk TEE configuration register
- Offset: 0x11d8
- Default Value: 0x16

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VOSYS_PCLK_DIV_EN	RW	vosys_pclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3:0]	VOSYS_PCLK_DIV_NUM	RW	Vosys_PCLK frequency division factor 4'd6: 1:6 .... 4'd12: 1:12 Value After Reset: 0x6

4.4.2.2.111 VOSYS_ACLK_TEECFG

- Description: vosys_aclk TEE configuration register
- Offset: 0x11dc
- Default Value: 0x33

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	VOSYS_AXI_ACLK_EN	RW	vosys_axi_aclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	VOSYS_ACLK_M_DIV_EN	RW	vosys_aclk_m's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3:0]	VOSYS_ACLK_M_DIV_NUM	RW	vosys_aclk_m's divider ratio 3'd3: 1:3 .....

Bits	Field Name	Access	Description
			3'd7: 1:7 Value After Reset: 0x3

4.4.2.2.112 VPSYS_CLK_TEECFG

- Description: VPSYS_ACLK configuration register
- Offset: 0x11e0
- Default Value: 0xb312

Bits	Field Name	Access	Description
[31:16]	RESERVED_4	-	
[15]	VPSYS_AXI_ACLK_EN	RW	vpsys_axi_aclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[14]	RESERVED_3	-	
[13]	CPU2VP_X2P_CLK_EN	RW	cpu2vp_x2p_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[12]	VPSYS_AXI_ACLK_DIV_EN	RW	vpsys_axi_aclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[11:8]	VPSYS_AXI_ACLK_DIV_NUM	RW	vpsys_axi_aclk's divider ratio 3'd3: 1:3 ..... 3'd7: 1:7 Value After Reset: 0x3
[7:5]	RESERVED_2	-	
[4]	VPSYS_APB_PCLK_DIV_EN	RW	vpsys_apb_pclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level.

Bits	Field Name	Access	Description
			2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3]	RESERVED_1	-	
[2:0]	VPSYS_APB_PCLK_DIV_NUM	RW	vpsys_apb_pclk's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.113 VENC_CCLK_TEECFG

- Description: VENC CCLK configuration register
- Offset: 0x11e4
- Default Value: 0x32

Bits	Field Name	Access	Description
[31:6]	RESERVED_2	-	
[5]	VENC_CCLK_EN	RW	VENC cclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	VENC_CCLK_DIV_EN	RW	vpsys_vend_cclk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[3]	RESERVED_1	-	
[2:0]	VENC_CCLK_DIV_NUM	RW	vpsys_venc_cclk's divider ratio 3'd2: 1:2 ..... 3'd7: 1:7 Value After Reset: 0x2

4.4.2.2.114 DPU0_PLL_DIV_TEECFG

- Description: dpu0_pll_div TEE configuration register
- Offset: 0x11e8
- Default Value: 0x102

Bits	Field Name	Access	Description
[31:9]	RESERVED_1	-	
[8]	DPU0_PLL_DIV_CLK_DIV_EN	RW	dpu0_pll_div_clk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[7:0]	DPU0_PLL_DIV_CLK_DIV_NUM	RW	dpu0_pll_div_clk's divider ratio 8'd2: 1:2 ..... 8'd7: 1:7 ..... Value After Reset: 0x2

4.4.2.2.115 DPU1_PLL_DIV_TEECFG

- Description: dpu1_pll_div TEE configuration register
- Offset: 0x11ec
- Default Value: 0x102

Bits	Field Name	Access	Description
[31:9]	RESERVED_1	-	
[8]	DPU1_PLL_DIV_CLK_DIV_EN	RW	dpu1_pll_div_clk's divider enable. To enable frequency division, the configuration steps are as follows: 1. Configure enabling div_EN to be low level. 2. Delay 1us. 3. Configure div_Num. 4. Configure enabling div_EN to be high level. Value After Reset: 0x1
[7:0]	DPU1_PLL_DIV_CLK_DIV_NUM	RW	dpu1_pll_div_clk's divider ratio 8'd2: 1:2

Bits	Field Name	Access	Description
			..... 8'd7: 1:7 ..... Value After Reset: 0x2

4.4.2.2.116 PERI_I2S_SRC_CLK_TEECFG

- Description: PERI_I2S_SRC_CLK configuration register
- Offset: 0x11f0
- Default Value: 0x2

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	PERI_I2S_CLK_EN	RW	peri_i2s_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[0]	PERI_I2S_SRC_CLK_MUX_SEL	RW	perisys i2s source clock select 0: 294.912MHz 1: 135.4752MHz Value After Reset: 0x0

4.4.2.2.117 PERI_CLK_TEECFG

- Description: Peripheral clock gate control register
- Offset: 0x1204
- Default Value: 0x55ffffff

Bits	Field Name	Access	Description
[31]	RESERVED_4	-	
[30]	EMMC_SDIO_REF_CLK_EN	RW	eMMC SDIO reference clock enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[29]	RESERVED_3	-	
[28]	RESERVED_REG_PERI	RW	reserved_reg_peri Value After Reset: 0x1

Bits	Field Name	Access	Description
[27]	RESERVED_2	-	
[26]	GMAC1_CLK_EN	RW	GMAC1 clock's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[25]	RESERVED_1	-	
[24]	PADCTRL1_APSYS_PCLK_EN	RW	PADCTRL1 clock's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[23]	DSMART_CLK_EN	RW	dsmart_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[22]	PADCTRL0_APSYS_PCLK_EN	RW	PADCTRL0 clock's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[21]	GMAC_AXI_CLK_EN	RW	GMAC axi4_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[20]	GPIO3_CLK_EN	RW	gpio3_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[19]	GMAC0_CLK_EN	RW	gmac_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[18]	PWM_CLK_EN	RW	pwm_clk's gate enable signal 0: Gate clock. 1: Open clock.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[17]	QSPI0_CLK_EN	RW	qspi0_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[16]	QSPI1_CLK_EN	RW	qspi1_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[15]	SPI_CLK_EN	RW	spi_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[14]	UART0_CLK_EN	RW	uart0_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[13]	UART1_CLK_EN	RW	uart1_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[12]	UART2_CLK_EN	RW	uart2_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[11]	UART3_CLK_EN	RW	uart3_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[10]	UART4_CLK_EN	RW	uart4_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

Bits	Field Name	Access	Description
[9]	UART5_CLK_EN	RW	uart5_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[8]	GPIO0_CLK_EN	RW	gpio0_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[7]	GPIO1_CLK_EN	RW	gpio1_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[6]	GPIO2_CLK_EN	RW	gpio2_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[5]	I2C0_CLK_EN	RW	i2c0_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	I2C1_CLK_EN	RW	i2c1_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[3]	I2C2_CLK_EN	RW	i2c2_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[2]	I2C3_CLK_EN	RW	i2c3_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[1]	I2C4_CLK_EN	RW	i2c4_clk's gate enable signal 0: Gate clock.

Bits	Field Name	Access	Description
			1: Open clock. Value After Reset: 0x1
[0]	I2C5_CLK_EN	RW	i2c5_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

4.4.2.2.118 CTRL_CLK_TEECFG

- Description: CTRL_CLK configuration register
- Offset: 0x1208
- Default Value: 0x7ff

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10]	SPINLOCK_HCLK_EN	RW	spinlock_hclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[9]	CHIP_DBG_CLK_EN	RW	chip_dbg_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[8]	DMAC_CPUSYS_CLK_EN	RW	dmac_cpusys_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[7]	MBOX0_PCLK_EN	RW	mbox0_pclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[6]	MBOX1_PCLK_EN	RW	mbox1_pclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

Bits	Field Name	Access	Description
[5]	MBOX2_PCLK_EN	RW	mbox2_pclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	MBOX3_PCLK_EN	RW	mbox3_pclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[3]	WDT0_PCLK_EN	RW	wdt0's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[2]	WDT1_PCLK_EN	RW	wdt1's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[1]	TIMER0_CLK_EN	RW	ddr_cclk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[0]	TIMER1_CLK_EN	RW	c910_cnt_clk's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

4.4.2.2.119 SRAM_AXI_CLK_TEECFG

- Description: SRAM_AXI_CLK configuration register
- Offset: 0x120c
- Default Value: 0x1e

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	SRAM_AXI_ACLK_0_EN	RW	sram_axi_aclk_0's gate enable signal 0: Gate clock. 1: Open clock.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[3]	SRAM_AXI_ACLK_1_EN	RW	sram_axi_aclk_1's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[2]	SRAM_AXI_ACLK_2_EN	RW	sram_axi_aclk_2's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[1]	SRAM_AXI_ACLK_3_EN	RW	sram_axi_aclk_3's gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[0]	RESERVED_1	-	

4.4.2.2.120 UART_SCLK_TEECFG

- Description: uart_aclk TEE configuration register
- Offset: 0x1210
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	UART_SCLK_SWITCH_SEL	RW	uart_ SCLK select 0: 100MHz 1: 24MHz Value After Reset: 0x0

4.4.2.2.121 SUBSYS_CLK_TEECFG

- Description: Subsystem TEE configuration register
- Offset: 0x1220
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	VOSYS_CLK_EN	RW	vosys_clk_en

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[1]	VISYS_CLK_EN	RW	visys_clk_en Value After Reset: 0x0
[0]	DSPSYS_CLK_EN	RW	dspsys_clk_en Value After Reset: 0x0

4.4.2.2.122 BOOT_CLK_SEL_TEECFG

- Description:
- Offset: 0x1280
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	REG_BOOT_PAD_SEL	RW	Reserved, software can't write this field. Value After Reset: 0x0

4.4.2.2.123 TEST_CLK_TEECFG

- Description: TEST_CLK configuration register
- Offset: 0x1300
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	TEST_CLK_SAMPLE_EN	RW	test_clk's sample enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x0
[4:0]	TEST_CLK_SEL	RW	test_clk[0]: Reserved test_clk[1]: apb3_cpusys_pclk test_clk[2]: axi4_cpusys2_aclk test_clk[3]: ahb2_cpusys_hclk test_clk[4]: axi4_cpusys1_aclk test_clk[5]: cfg_axi_aclk test_clk[6]: teesys_hclk test_clk[7]: 1'b0

Bits	Field Name	Access	Description
			test_clk[8]: perisys_ahb_hclk test_clk[9]: perisys_apb_pclk test_clk[10]: npu_cclk test_clk[11]: cfg_apb_pclk test_clk[12]: peri2sys_apb_pclk test_clk[13]: venc_cclk test_clk[14]: c910_core0_clk_div_monitor (c910_cclk/128) test_clk[15]: c910_core1_clk_div_monitor (c910_cclk/128) test_clk[16]: c910_core2_clk_div_monitor (c910_cclk/128) test_clk[17]: c910_core3_clk_div_monitor (c910_cclk/128) test_clk[18]: peri_i2s_src_clk test_clk[19]: vosys_aclk_m test_clk[20]: visys_aclk_m test_clk[21]: visys_ahb_hclk test_clk[22]: vpsys_apb_pclk test_clk[23]: vpsys_axi_aclk test_clk[24]: dpu0_pll_div_clk test_clk[25]: dpu1_pll_div_clk test_clk[31:26]: 'd0 Value After Reset: 0x0

4.4.2.2.124 TEST_CLK_TEESTS

- Description: TEST_CLK status register
- Offset: 0x1304
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	TEST_CLK_FREQ_STAT	RO	Read test clock frequency, unit: kHz Value After Reset: 0x0

4.4.2.2.125 BOOT_OSC_EN_TEE

- Description: Invalid register, software do not use
- Offset: 0x1308

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	PAD_OSC_BOOT_EN	RO	Indicate the boot clock state. 1'b1: Boot with OSC clock. 1'b0: Boot with PLL clock. Value After Reset: 0x0

4.4.2.2.126 RESERVED_TEEREG_0

- Description: RESERVED_REG_0
- Offset: 0x1310
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_0	RW	Reserved Value After Reset: 0x0

4.4.2.2.127 RESERVED_TEEREG_1

- Description: RESERVED_REG_1
- Offset: 0x1314
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_1	RW	Reserved Value After Reset: 0x0

4.4.2.2.128 RESERVED_TEEREG_2

- Description: RESERVED_REG_2
- Offset: 0x1318
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_2	RW	Reserved Value After Reset: 0x0

4.4.2.2.129 RESERVED_TEEREG_3

- Description: RESERVED_REG_3
- Offset: 0x131c

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_3	RW	Reserved Value After Reset: 0x0

4.4.2.2.130 CFG_LOCK_0

- Description: TEE side register domain write lock register
- Offset: 0x1800
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	CPU0_PLL_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[30]	CPU1_PLL_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[29]	GMAC_PLL_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[28]	VEDIO_PLL_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[27]	DPU0_PLL_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[26]	DPU1_PLL_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[25]	TEE_PLL_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[24]	C910_CORE0_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[23]	C910_CORE1_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[22]	C910_CORE2_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[21]	C910_CORE3_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[20]	C910_CFG_LOCK	RW	Write lock

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[19]	AHB2_CPUSYS_HCLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[18]	APB3_CPUSYS_PCLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[17]	AXI4_CPUSYS_ACLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[16]	CFG_AXI_ACLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[15]	PERISYS_AHB_HCLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[14]	PERISYS_APB_PCLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[13]	SENSOR_CLK_OUT_1_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[12]	SENSOR_CLK_OUT_2_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[11]	SENSOR_CLK_OUT_3_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[10]	SENSOR_CLK_OUT_4_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[9]	CFG_APB_PCLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[8]	NPU_CCLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[7]	VISYS_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[6]	VOSYS_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[5]	VPSYS_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[4]	VENC_CCLK_CFG_LOCK	RW	Write lock

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[3]	DPU0_PLL_DIV_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[2]	DPU1_PLL_DIV_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[1]	PERI_I2S_SRC_CCLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[0]	RESERVED_1	-	

4.4.2.2.131 CFG_LOCK_1

- Description: TEE side register domain write lock register
- Offset: 0x1804
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	
[30]	DSPSYS_CLK_CFG_LOCK	RW	dspsys_clk_cfg_write lock Value After Reset: 0x0
[29]	EMMC_SDIO_REF_CLK_EN_LOCK	RW	Write lock Value After Reset: 0x0
[28]	GMAC1_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[27]	PADCTRL1_APSYS_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[26]	EMMC_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[25]	SDIO0_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[24]	SDIO1_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[23]	DSMART_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[22]	PADCTRL0_APSYS_CLK_CFG_LO	RW	Write lock

Bits	Field Name	Access	Description
	CK		Value After Reset: 0x0
[21]	GMAC_AXI_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[20]	GPIO3_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[19]	GMAC0_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[18]	PWM_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[17]	QSPI0_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[16]	QSPI1_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[15]	SPI_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[14]	UART0_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[13]	UART1_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[12]	UART2_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[11]	UART3_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[10]	UART4_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[9]	UART5_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[8]	GPIO0_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[7]	GPIO1_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[6]	GPIO2_CLK_CFG_LOCK	RW	Write lock

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[5]	I2C0_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[4]	I2C1_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[3]	I2C2_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[2]	I2C3_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[1]	I2C4_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[0]	I2C5_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0

4.4.2.2.132 CFG_LOCK_2

- Description: TEE side register domain write lock register
- Offset: 0x1808
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:23]	RESERVED_2	-	
[22]	UART_SCLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[21]	SPINLOCK_HCLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[20]	CHIP_DBG_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[19]	DMAC_CPUSYS_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[18]	MBOX0_PCLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[17]	MBOX1_PCLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0

Bits	Field Name	Access	Description
[16]	MBOX2_PCLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[15]	MBOX3_PCLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[14]	WDT0_PCLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[13]	WDT1_PCLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[12]	TIMER0_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[11]	TIMER1_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[10]	SRAM_AXI_ACLK_0_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[9]	SRAM_AXI_ACLK_1_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[8]	SRAM_AXI_ACLK_2_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[7]	SRAM_AXI_ACLK_3_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[6]	RESERVED_1	-	
[5]	BOOT_CLK_SEL_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[4]	TEST_CLK_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[3]	RESERVED_REG_0_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[2]	RESERVED_REG_1_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[1]	RESERVED_REG_2_CFG_LOCK	RW	Write lock Value After Reset: 0x0
[0]	RESERVED_REG_3_CFG_LOCK	RW	Write lock

Bits	Field Name	Access	Description
			Value After Reset: 0x0

4.4.2.2.133 CPU_PLL0_MNT_TEECFG

- Description: cpu_pll0_foutpostdiv frequency monitor configuration register
- Offset: 0x1C00
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	CPU_PLL0_FOUTPOSTDIV_CFG_LOCK	RW	cpu_pll0_foutpostdiv monitor register domain latch, cannot write to other domains when this bit is 1. Value After Reset: 0x0
[30]	CPU_PLL0_FOUTPOSTDIV_MNT_EN	RW	cpu_pll0_foutpostdiv monitoring enable. When cpu_pll0_foutpostdiv_cfg_lock is 1, this bit cannot be written. cpu_pll0_foutpostdiv_cfg_lock needs to be set to 0 before it can be written. Value After Reset: 0x0
[29:20]	CPU_PLL0_FOUTPOSTDIV_MNT_THH	RW	Upper limit of cpu_pll0_foutpostdiv monitoring frequency. When cpu_pll0_foutpostdiv_cfg_lock is 1, this bit cannot be written. cpu_pll0_foutpostdiv_cfg_lock needs to be set to 0 before it can be written. Value After Reset: 0x0
[19:10]	CPU_PLL0_FOUTPOSTDIV_MNT_THL	RW	Lower limit of cpu_pll0_foutpostdiv monitoring frequency. When cpu_pll0_foutpostdiv_cfg_lock is 1, this bit cannot be written. cpu_pll0_foutpostdiv_cfg_lock needs to be set to 0 before it can be written. Value After Reset: 0x0
[9:0]	CPU_PLL0_FOUTPOSTDIV_MNTEDCLK_DIVFACTOR	RW	cpu_pll0_foutpostdiv monitoring clock frequency division coefficient 0,1: Illegal 2: 2 frequency division 3: 3 frequency division ... Value After Reset: 0x0

4.4.2.2.134 CPU_PLL1_MNT_TEECFG

- Description: cpu_pll1_foutpostdiv frequency monitor configuration register

- Offset: 0x1C04
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	CPU_PLL1_FOUTPOSTDIV_CFG_LOCK	RW	cpu_pll1_foutpostdiv monitor register domain latch, cannot write to other domains when this bit is 1. Value After Reset: 0x0
[30]	CPU_PLL1_FOUTPOSTDIV_MNT_EN	RW	cpu_pll1_foutpostdiv monitoring enable. When cpu_pll1_foutpostdiv_cfg_lock is 1, this bit cannot be written. cpu_pll1_foutpostdiv_cfg_lock needs to be set to 0 before it can be written. Value After Reset: 0x0
[29:20]	CPU_PLL1_FOUTPOSTDIV_MNT_THH	RW	Upper limit of cpu_pll1_foutpostdiv monitoring frequency. When cpu_pll1_foutpostdiv_cfg_lock is 1, this bit cannot be written. cpu_pll1_foutpostdiv_cfg_lock needs to be set to 0 before it can be written. Value After Reset: 0x0
[19:10]	CPU_PLL1_FOUTPOSTDIV_MNT_THL	RW	Lower limit of cpu_pll1_foutpostdiv monitoring frequency. When cpu_pll1_foutpostdiv_cfg_lock is 1, this bit cannot be written. cpu_pll1_foutpostdiv_cfg_lock needs to be set to 0 before it can be written. Value After Reset: 0x0
[9:0]	CPU_PLL1_FOUTPOSTDIV_MNTEDCLK_DIVFACTOR	RW	cpu_pll1_foutpostdiv monitoring clock frequency division coefficient 0,1: Illegal 2: 2 frequency division 3: 3 frequency division ... Value After Reset: 0x0

4.4.2.2.135 TEESYS_HCLK_MNT_TEECFG

- Description: teesys_hclk frequency monitor configuration register
- Offset: 0x1C08
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	TEESYS_HCLK_CFG_LOCK	RW	Teesys_Hclk monitor register domain latch, cannot write to other domains when this bit is 1.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[30]	TEESYS_HCLK_MNT_EN	RW	Teesys_Hclk monitoring enable. When teesys_Hclk_Cfg_lock is 1, this bit cannot be written. Teesys_Hclk_Cfg_Lock needs to be set to 0 before it can be written. Value After Reset: 0x0
[29:20]	TEESYS_HCLK_MNT_THH	RW	Upper limit of Teesys_ hclk monitoring frequency. When teesys_Hclk_ Cfg_ lock is 1, this bit cannot be written. teesys_Hclk_Cfg_Lock needs to be set to 0 before it can be written. Value After Reset: 0x0
[19:10]	TEESYS_HCLK_MNT_THL	RW	Lower limit of Teesys_hclk monitoring frequency. When teesys_Hclk_Cfg_lock is 1, this bit cannot be written. teesys_Hclk_Cfg_Lock needs to be set to 0 before it can be written. Value After Reset: 0x0
[9:0]	TEESYS_HCLK_MNTEDCLK_DIVFACTOR	RW	teesys_Hclk monitoring clock frequency division coefficient 0,1: Illegal 2: 2 frequency division 3: 3 frequency division ... Value After Reset: 0x0

4.4.2.3 DDR_SUBSYS

4.4.2.3.1 DDR_CFG1

- Description: Clock auto gate configuration
- Offset: 0x4
- Default Value: 0xa011f

Bits	Field Name	Access	Description
[31:22]	RESERVED_3	-	
[21:16]	RG_DDRC_AUTO_SR_DLY	RW	Will remove DDR core clock after the threshold of DDRC in AUTO SR mode. Value After Reset: 0xA
[15:9]	RESERVED_2	-	

Bits	Field Name	Access	Description
[8]	RG_DDRC_CK_FREE	RW	0: DDRC core clock will be removed when DDRC stay in SW AUTO SR mode for rg_ddrc_auto_sr_dly cycles. 1: DDRC core clock will be free on. Value After Reset: 0x1
[7:5]	RESERVED_1	-	
[4:0]	RG_AXI_CLK_FREE_EN	RW	5 AXI port clock gating control 0: AXI clock will be removed when no transaction finished. 1: AXI clock will always free on. Value After Reset: 0x1F

4.4.2.3.2 DDR_PLL_CFG0

- Description: DDR PLL configuration 0
- Offset: 0x08
- Default Value: 0x1408501

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	
[26:24]	DDR_PLL_POSTDIV2	RW	DDR SoC PLL post divide 2 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x1
[23]	RESERVED_2	-	
[22:20]	DDR_PLL_POSTDIV1	RW	DDR SoC PLL post divide 1 setting (1 to 7) Total post divide is POSTDIV1*POSTDIV2. Value After Reset: 0x4
[19:8]	DDR_PLL_FBDIV	RW	DDR SoC feedback divide value (16 to 3200 in integer mode, 20 to 320 in fractional mode) Value After Reset: 0x85
[7:6]	RESERVED_1	-	
[5:0]	DDR_PLL_REFDIV	RW	DDR SoC PLL reference divide value (1 to 63) Value After Reset: 0x1

4.4.2.3.3 DDR_PLL_CFG1

- Description: DDR PLL configuration 1
- Offset: 0x0c

- Default Value: 0x3000000

Bits	Field Name	Access	Description
[31]	DDR_PLL_BYPASS	RW	DDR SoC PLL FREF is bypassed to FOUTPOSTDIV. Value After Reset: 0x0
[30]	DDR_PLL_RST	RW	DDR SoC PLL clock power down control, active high Value After Reset: 0x0
[29]	RESERVED_2	-	
[28]	DDR_PLL_FOUTPOSTDIVPD	RW	DDR SoC PLL post divide power down, active high Value After Reset: 0x0
[27]	DDR_PLL_FOUT4PHASEPD	RW	DDR SoC PLL phase-shifter clock power-down control Value After Reset: 0x0
[26]	RESERVED_1	-	
[25]	DDR_PLL_DACPD	RW	Power down noise cancelling DAC in FRAC mode, active high 0: DAC is active. (default mode) 1: DAC is not active. (test mode only) Value After Reset: 0x1
[24]	DDR_PLL_DSMPD	RW	Delta_Signal modulator power down control, active high 0x1: Integer mode 0x0: Fractional mode DDR SoC PLL power down Delta-Sigma modulator 0: DSM is active. 1: DSM is powered down. Value After Reset: 0x1
[23:0]	DDR_PLL_FRAC	RW	DDR SoC PLL fractional portion of feedback divide value Value After Reset: 0x0

4.4.2.3.4 DDR_PLL_CFG2

- Description: DDR PLL configuration 2
- Offset: 0x10
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31]	RESERVED_1	-	

Bits	Field Name	Access	Description
[30]	DDR_PLL_DSKEWCALLOCK	RO	Dskew calibration lock status Value After Reset: 0x0
[29]	DDR_PLL_DSKEWCALBYP	RW	Dskew calibration bypass configuration Value After Reset: 0x0
[28]	DDR_PLL_DSKEWCALEN	RW	Dskew calibration enable Value After Reset: 0x0
[27]	DDR_PLL_DSKEWFASTCAL	RW	Fast dskew calibration enable Value After Reset: 0x0
[26:24]	DDR_PLL_DSKEWCALCNT	RW	Dskew calibration lcnt Value After Reset: 0x2
[23:12]	DDR_PLL_DSKEWCALIN	RW	Dskew calibration input Value After Reset: 0x0
[11:0]	DDR_PLL_DSKEWCALOUT	RO	Dskew calibration output Value After Reset: 0x0

4.4.2.3.5 DDR_PLL_CFG3

- Description: DDR PLL configuration 3
- Offset: 0x14
- Default Value: 0x7fff400

Bits	Field Name	Access	Description
[31:12]	DDR_PLL_CALLOCK_CNT	RW	Offset calibration lock count. This signal is only available in PLL_callock_cnt_EN enabled. Value After Reset: 0x7FFF
[11]	RESERVED_2	-	
[10]	DDR_PLL_CALLOCK_CNT_EN	RW	Skew calibration lock count enable, connected to register, quasi-static signal, default to 1. When the signal is enabled, the PLL calibration circuit will ignore the callock output by the PLL and use the counting method to determine whether the calibration is locked. Value After Reset: 0x1
[9]	DDR_PLL_DESKEWCAL_PULSE	RW	When the offset calibration pulse is received in the register, it is required to write 1 clear 0, and the internal synchronization has been done, which is 0 by default.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[8]	DDR_PLL_DESKEWCAL_SW_EN	RW	The skew calibration software is enabled. It is connected to the register and quasi-static signal. The default is 0. When the signal is enabled, the PLL calibration circuit will be bypassed, and the software can directly control the calibration signal to calibrate the PLL according to the calibration timing. Value After Reset: 0x0
[7]	DDR_PLL_DESKEWCAL_RDY	RO	PLL calibration ready signal indicates that the call value of PLL is latched and connected to the register. Value After Reset: 0x0
[6:4]	RESERVED_1	-	
[3:0]	DDR_PLL_DSKEWCAL_STAT	RO	Dskew calibration status Value After Reset: 0x0

4.4.2.3.6 DDR_PLL_STS

- Description: PLL output configuration
- Offset: 0x18
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:17]	RESERVED_2	-	
[16]	RG_CTL_DDR_PLL_CLK_EN	RW	Enable DDR PLL output Value After Reset: 0x0
[15:1]	RESERVED_1	-	
[0]	RG_STA_DDR_PLL_LOCK	RO	DDR PLL lock indicator Value After Reset: 0x0

4.4.2.3.7 DDR_PLL_MON_STS

- Description: DDR clock monitor frequency indicator
- Offset: 0x20
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PLL_TEST_CLK_FREQ_STAT	RO	Monitor clock frequency indicator.

Bits	Field Name	Access	Description
			Value After Reset: 0x0

4.4.2.3.8 DDR_PLL_MON_CFG

- Description: Clock monitor configuration
- Offset: 0x24
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_2	-	
[7:4]	PLL_TEST_CLK_SEL	RW	Select clock frequency to monitor. [0]: postdiv [1]: 0 [2]: fout4 Others: Reserved Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	PLL_TEST_CLK_SAMPLE_EN	RW	Monitor clock enable Value After Reset: 0x0

4.4.2.4 MISC_SUBSYS

4.4.2.4.1 MISCSYS_BUS_CLK_CTRL

- Description: MISCSYS_BUS_CLK configuration register
- Offset: 0x100
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MISCSYS_ACLK_EN	RW	misc_subsys busclk gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

4.4.2.4.2 MISCSYS_USB_CLK_CTRL

- Description: MISCSYS_USB_CLK configuration register
- Offset: 0x104

- Default Value: 0xf

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	USB3_DRD_SUSPEND_CLK_EN	RW	USB suspend clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[2]	USB3_DRD_PHY_REF_CLK_EN	RW	USB PHY referece clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[1]	USB3_DRD_CTRL_REF_CLK_EN	RW	USB control reference clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[0]	USB3_DRD_CLK_EN	RW	USB AXI APB clk gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

4.4.2.4.3 MISCSYS_EMMC_CLK_CTRL

- Description: MISCSYS_EMMC_CLK configuration register
- Offset: 0x108
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	EMMC_CLK_EN	RW	eMMC clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

4.4.2.4.4 MISCSYS_SDIO0_CLK_CTRL

- Description: MISCSYS_SDIO0_CLK configuration register
- Offset: 0x10c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIO0_CLK_EN	RW	SDIO0 clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

4.4.2.4.5 MISCSYS_SDIO1_CLK_CTRL

- Description: MISCSYS_SDIO1_CLK configuration register
- Offset: 0x110
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIO1_CLK_EN	RW	SDIO1 clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

4.4.2.4.6 MISCSYS_BUS_CLK_CTRL_TEE

- Description: MISCSYS_BUS_CLK configuration register
- Offset: 0x1100
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MISCSYS_ACLK_EN	RW	misc_subsys busclk gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

4.4.2.4.7 MISCSYS_USB_CLK_CTRL_TEE

- Description: MISCSYS_USB_CLK configuration register
- Offset: 0x1104
- Default Value: 0xf

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	USB3_DRD_SUSPEND_CLK_EN	RW	USB suspend clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[2]	USB3_DRD_PHY_REF_CLK_EN	RW	USB PHY reference clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[1]	USB3_DRD_CTRL_REF_CLK_EN	RW	USB control reference clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[0]	USB3_DRD_CLK_EN	RW	USB AXI APB clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

4.4.2.4.8 MISCSYS_EMMC_CLK_CTRL_TEE

- Description: MISCSYS_EMMC_CLK configuration register
- Offset: 0x1108
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	EMMC_CLK_EN	RW	eMMC clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

4.4.2.4.9 MISCSYS_SDIO0_CLK_CTRL_TEE

- Description: MISCSYS_SDIO0_CLK configuration register
- Offset: 0x110c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIO0_CLK_EN	RW	SDIO0 clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

4.4.2.4.10 MISCSYS_SDIO1_CLK_CTRL_TEE

- Description: MISCSYS_SDIO1_CLK configuration register
- Offset: 0x1110
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIO1_CLK_EN	RW	SDIO1 clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

4.4.2.4.11 MISCSYS_TEE_CLK_CTRL_TEE

- Description: TEE subsystem clock reset configuration register
- Offset: 0x1120
- Default Value: 0x7ff

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10]	TEE_SYSREG_PCLK_EN	RW	TEE subsystem sysreg's clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[9]	EFUSE_PCLK_EN	RW	TEE subsystem eFuse's clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[8]	OCRAM_HCLK_EN	RW	TEE subsystem OCRAM's clock gate enable signal 0: Gate clock.

Bits	Field Name	Access	Description
			1: Open clock. Value After Reset: 0x1
[7]	EIP150B_HCLK_EN	RW	TEE subsystem EIP150B's clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[6]	TEE_DMAC_CLK_EN	RW	TEE subsystem DMA's clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[5]	EIP120SIII_CLK_EN	RW	TEE subsystem EIP120SIII's clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[4]	EIP120SII_CLK_EN	RW	TEE subsystem EIP120SII's clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[3]	EIP120SI_CLK_EN	RW	TEE subsystem EIP120SI's clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[2]	AXI4_TEESYS_ACLK_EN	RW	TEE subsystem AXI bus's clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[1]	APB3_TEESYS_HCLK_EN	RW	TEE subsystem APB bus's clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1
[0]	AHB2_TEESYS_HCLK_EN	RW	TEE subsystem AHB bus's clock gate enable signal 0: Gate clock. 1: Open clock. Value After Reset: 0x1

4.4.2.4.12 TEESYS_PCLK_MNT_TEECFG

- Description: TEE subsystem APB clock monitor register
- Offset: 0x1124
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	TEESYS_PCLK_CFG_LOCK	RW	TEE subsystem APB clock monitor register lock Value After Reset: 0x0
[30]	TEESYS_PCLK_MNT_EN	RW	TEE subsystem APB clock monitor enable Value After Reset: 0x0
[29:20]	TEESYS_PCLK_MNT_THH	RW	TEE subsystem APB clock monitor threshold high Value After Reset: 0x0
[19:10]	TEESYS_PCLK_MNT_THL	RW	TEE subsystem APB clock monitor threshold low Value After Reset: 0x0
[9:0]	TEESYS_PCLK_MNTEDCLK_DIVFACTOR	RW	TEE subsystem APB clock monitor divider factor Value After Reset: 0x0

4.4.2.5 VI_SUBSYS

4.4.2.5.1 VI_APB_PCLK_CFG

- Description: VISYS_PCLK configuration register
- Offset: 0x10
- Default Value: 0x9

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	VISYS_PCLK_CDE_SYNC	RW	vi_apb_pclk's divider enable, software needs to be pulled low and then pulled high. Value After Reset: 0x1
[2:0]	VISYS_PCLK_CDE_RATIO	RW	vi_apb_pclk's divider ratio 3'd1: 1:2, 396/2=198MHz 3'd2: 1:3, 396/3=132MHz ..... 3'd7: 1:8, 396/8=49.5MHz Value After Reset: 0x1

4.4.2.5.2 DW200_CLK_DWE_CFG

- Description: DEWARP's dewarp core clock configuration register
- Offset: 0x14
- Default Value: 0x13

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VISYS_DW200_CLK_DWE_DIV_EN	RW	visys_dw200_clk_dwe clock divider enable. Software needs to be pulled low and then pulled high. Value After Reset: 0x1
[3:0]	VISYS_DW200_CLK_DWE_DIV_NUM	RW	visys_dw200_clk_dwe's divider number dw200_clk_dwe's divider ratio 4'd3: 2376/3=792MHz, this is the maximum frequency, recommended for 1 4k@60fps or 1 path 4k@30fps+1 1080p60fps 4'd6, 2376/6=396MHz, recommended for 2 1080p60fps or 1 4k@30fps 4'd12, 2376/12=198MHz, recommended for 1 1080p60 fps Note: (1)clk_dwe>=axi_clk(must follow). (2)clk_vse>=clk_dwe when enable dewarp and scaler. Value After Reset: 0x3

4.4.2.5.3 DW200_CLK_VSE_CFG

- Description: DEWARP's scaler core clock configuration register
- Offset: 0x18
- Default Value: 0x13

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VISYS_DW200_CLK_VSE_DIV_EN	RW	visys_dw200_clk_vse clk divider enable. Software needs to be pulled low and then pulled high. Value After Reset: 0x1
[3:0]	VISYS_DW200_CLK_VSE_DIV_NUM	RW	visys_dw200_clk_vse's divider number dw200_clk_vse's divider ratio 4'd3: 1:4, 2376/3=792MHz, this is the maximum frequency, recommended for 1 4k@60fps or 1 path 4k@30fps+1 1080p60fps. 4'd6, 2376/6=396MHz, recommended for 2 1080p60fps

Bits	Field Name	Access	Description
			or 1 4k@30fps. 4'd12, 2376/12=198MHz, recommended for 1 1080p60 fps. Note: clk_vse>=clk_dwe when enable dewarp and scaler. Value After Reset: 0x3

4.4.2.5.4 ISP0_CLK_CFG

- Description: ISP core0 clock configuration register
- Offset: 0x24
- Default Value: 0x16

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VISYS_ISP0_CLK_DIV_EN	RW	isp_clk_0 divider enable. Software needs to be pulled low and then pulled high. Value After Reset: 0x1
[3:0]	VISYS_ISP0_CLK_DIV_NUM	RW	isp_clk_0's divider number isp0 core clock's divider ratio 4'd6, 2376/6=396MHz, this is the maximum frequency, recommended for 1 12M@30fps. 4'd8, 2376/8=297MHz, recommended for 1 8M@30 fps. 4'd12, 2376/12=198MHz, recommended for 1 5M@30 fps or 2M@60fps. for HDR: 2 exposure mode: 1/2mipi_csi0_pixelclk<= isp0_clk<=mipi_csi0_pixelclk 3 exposure mode: 1/3 mipi_csi0_pixelclk<= isp0_clk<=mipi_csi0_pixelclk Value After Reset: 0x6

4.4.2.5.5 ISP1_CLK_CFG

- Description: ISP core1 clock configuration register
- Offset: 0x28
- Default Value: 0x16

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VISYS_ISP1_CLK_DIV_EN	RW	isp_clk_1 divider enable. Software needs to be pulled low and then pulled high. Value After Reset: 0x1
[3:0]	VISYS_ISP1_CLK_DIV_NUM	RW	isp_clk_1's divider number isp1 core clk's divider ratio 4'd6, 2376/6=396MHz, this is the maximum frequency, recommended for 1 12M@30fps. 4'd8, 2376/8=297MHz, recommended for 1 8M@30 fps. 4'd12, 2376/12=198MHz, recommended for 1 5M@30 fps or 2M@60fps. for HDR: 2 exposure mode: 1/2mipi_csi0_pixelclk<= isp1_clk<=mipi_csi0_pixelclk 3 exposure mode: 1/3 mipi_csi0_pixelclk<= isp1_clk<=mipi_csi0_pixelclk Value After Reset: 0x6

4.4.2.5.6 ISP_RY_CLK_CFG

- Description: POST ISP clock configuration register
- Offset: 0x2c
- Default Value: 0x14

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VISYS_ISP_RY_CCLK_DIV_EN	RW	isp_ry_cclk divider enable. Software needs to be pulled low and then pulled high. Value After Reset: 0x1
[3:0]	VISYS_ISP_RY_CCLK_DIV_NUM	RW	isp_ry_cclk's divider number 4'd4, 2376/4=594MHz, this is the maximum frequency, recommended for 1 12M@30fps. 4'd6, 2376/6=396MHz, recommended for 1 8M@30 fps. 4'd8, 2376/8=297MHz, recommended for 1 5M@30 fps or 2M@60fps. Value After Reset: 0x4

4.4.2.5.7 MIPI_CSI0_PIXELCLK

- Description: MIPI CSI output pixel clock configuration register
- Offset: 0x30
- Default Value: 0x13

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VISYS_MIPI_CSI0_PIXELCLK_DIV_EN	RW	mipi_csi0 divider enable. Software needs to be pulled low and then pulled high. Value After Reset: 0x1
[3:0]	VISYS_MIPI_CSI0_PIXELCLK_DIV_NUM	RW	mipi_csi0 divider number mipi csi ipi's divider ratio 4'd3: 2376/3=792MHz, this is the maximum frequency, recommended for 4K&2160P sensor or sensor whose horizontal resolution is greater than or equal to 4096. 4'd6, 2376/6=396MHz: recommended for 2K&1080P sensor. 4'd12, 2376/12=198MHz, recommended for 720P&640P&320P sensor. Note: If there are more than 1 sensor in application, the clock must set as the highest one. Value After Reset: 0x3

4.4.2.5.8 VISYS_CLK_GATE_EN_0

- Description: VISYS_CLK_GATE_EN_0
- Offset: 0xa0
- Default Value: 0xff67bfff

Bits	Field Name	Access	Description
[31]	CLKCTRL_VIPRE_ACLK_EN	RW	vipre_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[30]	CLKCTRL_ISP_VENC_SHAKE_ACLK_EN	RW	isp_venc_shake_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[29]	CLKCTRL_ISP_VENC_SHAKE_PCL	RW	isp_venc_shake_pclk clock enable

Bits	Field Name	Access	Description
	K_EN		1: Clock on. 0: Clock off. Value After Reset: 0x1
[28]	CLKCTRL_VISYS_ACLK_EN	RW	visys_aclk clk enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[27]	CLKCTRL_DW200_ACLK_EN	RW	dw200_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[26]	CLKCTRL_AXI4_VISYS1_ACLK_EN	RW	axi4_visys1_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[25]	CLKCTRL_AXI4_VISYS2_ACLK_EN	RW	axi4_visys2_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[24]	CLKCTRL_AXI4_VISYS3_ACLK_EN	RW	axi4_visys3_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[23]	RESERVED_3	-	
[22]	CLKCTRL_ISP_RY_ACLK_EN	RW	isp_ry_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[21]	CLKCTRL_ISP_RY_CCLK_EN	RW	isp_ry_cclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[20:19]	RESERVED_2	-	

Bits	Field Name	Access	Description
[18]	CLKCTRL_MIPI_CSI0_PCLK_EN	RW	mipi_csi0_pclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[17]	CLKCTRL_MIPI_CSI1_PCLK_EN	RW	mipi_csi1_pclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[16]	CLKCTRL_MIPI_CSI2_PCLK_EN	RW	mipi_csi2_pclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[15]	CLKCTRL_VIPRE_PCLK_EN	RW	vipre_pclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[14]	RESERVED_1	-	
[13]	CLKCTRL_DW200_HCLK_EN	RW	dw200_hclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[12]	CLKCTRL_ISP_RY_HCLK_EN	RW	isp_ry_hclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[11]	CLKCTRL_MIPI_CSI0_PIXCLK_0IF_CLK_EN	RW	mipi_csi0_pixclk_0if_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[10]	CLKCTRL_MIPI_CSI1_PIXCLK_0IF_CLK_EN	RW	mipi_csi1_pixclk_0if_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1

Bits	Field Name	Access	Description
[9]	CLKCTRL_MIPI_CSI2_PIXCLK_0IF_CLK_EN	RW	mipi_csi2_pixclk_0if_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[8]	CLKCTRL_MIPI_CSI0_CFG_CLK_EN	RW	mipi_csi0_cfg_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[7]	CLKCTRL_MIPI_CSI1_CFG_CLK_EN	RW	mipi_csi1_cfg_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[6]	CLKCTRL_MIPI_CSI2_CFG_CLK_EN	RW	mipi_csi2_cfg_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[5]	CLKCTRL_DW200_CLK_VSE_CLK_EN	RW	dw200_clk_vse_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[4]	CLKCTRL_DW200_CLK_DWE_CLK_EN	RW	dw200_clk_dwe_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[3]	CLKCTRL_ISP0_ACLK_EN	RW	isp0_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[2]	CLKCTRL_ISP1_ACLK_EN	RW	isp1_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[1]	CLKCTRL_ISP0_HCLK_EN	RW	isp0_hclk clock enable 1: Clock on.

Bits	Field Name	Access	Description
			0: Clock off. Value After Reset: 0x1
[0]	CLKCTRL_ISP1_HCLK_EN	RW	isp1_hclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1

4.4.2.5.9 VISYS_CLK_GATE_EN_1

- Description: VISYS_CLK_GATE_EN_1
- Offset: 0xa4
- Default Value: 0xf0800000

Bits	Field Name	Access	Description
[31]	CLKCTRL_ISP0_CLK_EN	RW	isp0_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[30]	CLKCTRL_ISP1_CLK_EN	RW	isp1_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[29]	CLKCTRL_ISP0_PIXELCLK_EN	RW	isp0_pixelclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[28]	CLKCTRL_ISP1_PIXELCLK_EN	RW	isp1_pixelclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[27:24]	RESERVED_2	-	
[23]	CLKCTRL_VIPRE_PIXELCLK_EN	RW	vipre_pixelclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1

Bits	Field Name	Access	Description
[22:0]	RESERVED_1	-	

4.4.2.5.10 TEST_CLK_FREQ_STAT

- Description: TEST_CLK_FREQ_STAT
- Offset: 0x108
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	TEST_CLK_FREQ_STAT	RO	clk_calc output freq_stat Value After Reset: 0x0

4.4.2.5.11 TEST_CLK_CFG

- Description: TEST_CLK_CFG
- Offset: 0x10c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_2	-	
[7:4]	TEST_CLK_SEL	RW	clk_calc clock select [0]: visys_dw200_clk_dwe [1]: visys_dw200_clk_vse [2]: visys_isp0_clk [3]: visys_isp1_clk [4]: visys_isp_ry_cclk [5]: visys_mipi_csi0_pixelclk [6]: visys_pclk Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	TEST_CLK_SAMPLE_EN	RW	clk_calc sample enable Value After Reset: 0x0

4.4.2.5.12 VI_APB_PCLK_CFG_TEE

- Description: VISYS_PCLK configuration register
- Offset: 0x1010
- Default Value: 0x9

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	VISYS_PCLK_CDE_SYNC	RW	vi_apb_pclk's divider enable. Software needs to be pulled low and then pulled high. Value After Reset: 0x1
[2:0]	VISYS_PCLK_CDE_RATIO	RW	vi_apb_pclk's divider ratio 3'd1: 1:2, 396/2=198MHz 3'd2: 1:3, 396/3=132MHz ..... 3'd7: 1:8, 396/8=49.5MHz Value After Reset: 0x1

4.4.2.5.13 DW200_CLK_DWE_CFG_TEE

- Description: DEWARP's dewarp core clock configuration register
- Offset: 0x1014
- Default Value: 0x13

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VISYS_DW200_CLK_DWE_DIV_EN	RW	visys_dw200_clk_dwe clock divider enable. Software needs to be pulled low and then pulled high. Value After Reset: 0x1
[3:0]	VISYS_DW200_CLK_DWE_DIV_NUM	RW	visys_dw200_clk_dwe's divider number dw200_clk_dwe's divider ratio 4'd3: 2376/3=792MHz, this is the maximum frequency, recommended for 1 4k@60fps or 1 path 4k@30fps+1 1080p60fps. 4'd6, 2376/6=396MHz, recommended for 2 1080p60fps or 1 4k@30fps. 4'd12, 2376/12=198MHz, recommended for 1 1080p60 fps. Note: (1) clk_dwe>=axi_clk(must follow). (2) clk_vse>=clk_dwe when enable dewarp and scaler. Value After Reset: 0x3

4.4.2.5.14 DW200_CLK_VSE_CFG_TEE

- Description: DEWARP's scaler core clock configuration register
- Offset: 0x1018

- Default Value: 0x13

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VISYS_DW200_CLK_VSE_DIV_EN	RW	visys_dw200_clk_vse clock divider enable. Software needs to be pulled low and then pulled high. Value After Reset: 0x1
[3:0]	VISYS_DW200_CLK_VSE_DIV_NUM	RW	visys_dw200_clk_vse's divider number dw200_clk_vse's divider ratio 4'd3: 1:4, 2376/3=792MHz, this is the maximum frequency, recommended for 1 4k@60fps or 1 path 4k@30fps+1 1080p60fps. 4'd6, 2376/6=396MHz, recommended for 2 1080p60fps or 1 4k@30fps. 4'd12, 2376/12=198MHz, recommended for 1 1080p60fps. Note: clk_vse>=clk_dwe when enable dewarp and scaler. Value After Reset: 0x3

4.4.2.5.15 ISP0_CLK_CFG_TEE

- Description: ISP core0' clock configuration register
- Offset: 0x1024
- Default Value: 0x16

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VISYS_ISP0_CLK_DIV_EN	RW	isp_clk_0 divider enable. Software needs to be pulled low and then pulled high. Value After Reset: 0x1
[3:0]	VISYS_ISP0_CLK_DIV_NUM	RW	isp_clk_0's divider number isp0 core clk's divider ratio 4'd6, 2376/6=396MHz, this is the maximum frequency, recommended for 12M@30fps. 4'd8, 2376/8=297MHz, recommended for 1 8M@30fps. 4'd12, 2376/12=198MHz, recommended for 1 5M@30 fps or 2M@60fps. for HDR: 2 exposure mode: 1/2mipi_csi0_pixelclk<=

Bits	Field Name	Access	Description
			isp0_clk<=mipi_csi0_pixelclk 3 exposure mode: 1/3 mipi_csi0_pixelclk<= isp0_clk<=mipi_csi0_pixelclk Value After Reset: 0x6

4.4.2.5.16 ISP1_CLK_CFG_TEE

- Description: ISP core1' clock configuration register
- Offset: 0x1028
- Default Value: 0x16

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VISYS_ISP1_CLK_DIV_EN	RW	isp_clk_1 divider enable. Software needs to be pulled low and then pulled high. Value After Reset: 0x1
[3:0]	VISYS_ISP1_CLK_DIV_NUM	RW	isp_clk_1's divider number isp1 core clk's divider ratio 4'd6, 2376/6=396MHz, this is the maximum frequency, recommended for 1 12M@30fps. 4'd8, 2376/8=297MHz, recommended for 1 8M@30fps. 4'd12, 2376/12=198MHz, recommended for 1 5M@30 fps or 2M@60fps. for HDR: 2 exposure mode: 1/2mipi_csi0_pixelclk<= isp1_clk<=mipi_csi0_pixelclk 3 exposure mode: 1/3 mipi_csi0_pixelclk<= isp1_clk<=mipi_csi0_pixelclk Value After Reset: 0x6

4.4.2.5.17 ISP_RY_CLK_CFG_TEE

- Description: POST ISP clock configuration register
- Offset: 0x102c
- Default Value: 0x14

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VISYS_ISP_RY_CCLK_DIV_EN	RW	isp_ry_cclk divider enable. Software needs to be pulled low and then pulled high.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[3:0]	VISYS_ISP_RY_CCLK_DIV_NUM	RW	isp_ry_cclk's divider number 4'd4, 2376/4=594MHz, this is the maximum frequency, recommended for 1 12M@30fps. 4'd6, 2376/6=396MHz, recommended for 1 8M@30fps. 4'd8, 2376/8=297MHz, recommended for 1 5M@30 fps or 2M@60fps. Value After Reset: 0x4

4.4.2.5.18 MIPI_CSI0_PIXELCLK_TEE

- Description: MIPI CSI output pixel clock configuration register
- Offset: 0x1030
- Default Value: 0x13

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VISYS_MIPI_CSI0_PIXELCLK_DIV_EN	RW	mipi_csi0 divider enable. Software needs to be pulled low and then pulled high. Value After Reset: 0x1
[3:0]	VISYS_MIPI_CSI0_PIXELCLK_DIV_NUM	RW	mipi_csi0 divider number mipi csi ipi's divider ratio 4'd3: 2376/3=792MHz, this is the maximum frequency, recommended for 4K&2160P sensor or sensor whose horizontal resolution is greater than or equal to 4096. 4'd6, 2376/6=396MHz, recommended for 2K&1080P sensor. 4'd12, 2376/12=198MHz, recommended for 720P&640P&320P sensor. Note: If there are more than 1 sensor in application, the clock must set as the highest one. Value After Reset: 0x3

4.4.2.5.19 VISYS_CLK_GATE_EN_0_TEE

- Description: VISYS_CLK_GATE_EN_0
- Offset: 0x10a0
- Default Value: 0xff67bfff

Bits	Field Name	Access	Description
[31]	CLKCTRL_VIPRE_ACLK_EN	RW	vipre_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[30]	CLKCTRL_ISP_VENC_SHAKE_ACLK_EN	RW	isp_venc_shake_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[29]	CLKCTRL_ISP_VENC_SHAKE_PCLK_EN	RW	isp_venc_shake_pclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[28]	CLKCTRL_VISYS_ACLK_EN	RW	visys_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[27]	CLKCTRL_DW200_ACLK_EN	RW	dw200_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[26]	CLKCTRL_AXI4_VISYS1_ACLK_EN	RW	axi4_visys1_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[25]	CLKCTRL_AXI4_VISYS2_ACLK_EN	RW	axi4_visys2_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[24]	CLKCTRL_AXI4_VISYS3_ACLK_EN	RW	axi4_visys3_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[23]	RESERVED_3	-	

Bits	Field Name	Access	Description
[22]	CLKCTRL_ISP_RY_ACLK_EN	RW	isp_ry_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[21]	CLKCTRL_ISP_RY_CCLK_EN	RW	isp_ry_cclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[20:19]	RESERVED_2	-	
[18]	CLKCTRL_MIPI_CSI0_PCLK_EN	RW	mipi_csi0_pclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[17]	CLKCTRL_MIPI_CSI1_PCLK_EN	RW	mipi_csi1_pclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[16]	CLKCTRL_MIPI_CSI2_PCLK_EN	RW	mipi_csi2_pclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[15]	CLKCTRL_VIPRE_PCLK_EN	RW	vipre_pclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[14]	RESERVED_1	-	
[13]	CLKCTRL_DW200_HCLK_EN	RW	dw200_hclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[12]	CLKCTRL_ISP_RY_HCLK_EN	RW	isp_ry_hclk clock enable 1: Clock on. 0: Clock off.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[11]	CLKCTRL_MIPI_CSI0_PIXCLK_0IF_CLK_EN	RW	mipi_csi0_pixclk_0if_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[10]	CLKCTRL_MIPI_CSI1_PIXCLK_0IF_CLK_EN	RW	mipi_csi1_pixclk_0if_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[9]	CLKCTRL_MIPI_CSI2_PIXCLK_0IF_CLK_EN	RW	mipi_csi2_pixclk_0if_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[8]	CLKCTRL_MIPI_CSI0_CFG_CLK_EN	RW	mipi_csi0_cfg_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[7]	CLKCTRL_MIPI_CSI1_CFG_CLK_EN	RW	mipi_csi1_cfg_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[6]	CLKCTRL_MIPI_CSI2_CFG_CLK_EN	RW	mipi_csi2_cfg_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[5]	CLKCTRL_DW200_CLK_VSE_CLK_EN	RW	dw200_clk_vse_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[4]	CLKCTRL_DW200_CLK_DWE_CLK_EN	RW	dw200_clk_dwe_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1

Bits	Field Name	Access	Description
[3]	CLKCTRL_ISP0_ACLK_EN	RW	isp0_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[2]	CLKCTRL_ISP1_ACLK_EN	RW	isp1_aclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[1]	CLKCTRL_ISP0_HCLK_EN	RW	isp0_hclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[0]	CLKCTRL_ISP1_HCLK_EN	RW	isp1_hclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1

4.4.2.5.20 VISYS_CLK_GATE_EN_1_TEE

- Description: VISYS_CLK_GATE_EN_1
- Offset: 0x10a4
- Default Value: 0xf0800000

Bits	Field Name	Access	Description
[31]	CLKCTRL_ISP0_CLK_EN	RW	isp0_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[30]	CLKCTRL_ISP1_CLK_EN	RW	isp1_clk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[29]	CLKCTRL_ISP0_PIXELCLK_EN	RW	isp0_pixelclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1

Bits	Field Name	Access	Description
[28]	CLKCTRL_ISP1_PIXELCLK_EN	RW	isp1_pixelclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[27:24]	RESERVED_2	-	
[23]	CLKCTRL_VIPRE_PIXELCLK_EN	RW	vipre_pixelclk clock enable 1: Clock on. 0: Clock off. Value After Reset: 0x1
[22:0]	RESERVED_1	-	

4.4.2.5.21 TEST_CLK_FREQ_STAT_TEE

- Description: TEST_CLK_FREQ_STAT
- Offset: 0x1108
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	TEST_CLK_FREQ_STAT	RO	clk_calc output freq_stat Value After Reset: 0x0

4.4.2.5.22 TEST_CLK_CFG_TEE

- Description: TEST_CLK_CFG
- Offset: 0x110c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_2	-	
[7:4]	TEST_CLK_SEL	RW	clk_calc clock select [0]: visys_dw200_clk_dwe [1]: visys_dw200_clk_vse [2]: visys_isp0_clk [3]: visys_isp1_clk [4]: visys_isp_ry_cclk [5]: visys_mipi_csi0_pixelclk [6]: visys_pclk Value After Reset: 0x0

Bits	Field Name	Access	Description
[3:1]	RESERVED_1	-	
[0]	TEST_CLK_SAMPLE_EN	RW	clk_calc sample enable Value After Reset: 0x0

4.4.2.5.23 CFG_CLK_LOCK_TEE

- Description: VI clock registers TEE lock
- Offset: 0x1200
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_6	-	
[30]	VI_SUBSYS_CLKCFG_LOCK	RW	vi_subsys_clkcfg_lock Value After Reset: 0x0
[29]	VI_SUBSYS1_CLKCFG_LOCK	RW	vi_subsys1_clkcfg_lock Value After Reset: 0x0
[28]	VI_SUBSYS2_CLKCFG_LOCK	RW	vi_subsys2_clkcfg_lock Value After Reset: 0x0
[27]	VI_SUBSYS3_CLKCFG_LOCK	RW	vi_subsys3_clkcfg_lock Value After Reset: 0x0
[26:25]	RESERVED_5	-	
[24]	DW200_CLKCFG_LOCK	RW	dw200_clkcfg_lock Value After Reset: 0x0
[23:19]	RESERVED_4	-	
[18]	ISP0_CLKCFG_LOCK	RW	isp0_clkcfg_lock Value After Reset: 0x0
[17]	ISP1_CLKCFG_LOCK	RW	isp1_clkcfg_lock Value After Reset: 0x0
[16]	ISP_RY_CLKCFG_LOCK	RW	isp_ry_clkcfg_lock Value After Reset: 0x0
[15]	RESERVED_3	-	
[14]	MIPI_CSI0_CLKCFG_LOCK	RW	mipi_csi0_clkcfg_lock Value After Reset: 0x0
[13]	MIPI_CSI1_CLKCFG_LOCK	RW	mipi_csi1_clkcfg_lock

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[12]	MIPI_CSI2_CLKCFG_LOCK	RW	mipi_csi2_clkcfg_lock Value After Reset: 0x0
[11:10]	RESERVED_2	-	
[9]	ISP_VENC_SHAKE_CLKCFG_LOCK	RW	isp_venc_shake_clkcfg_lock Value After Reset: 0x0
[8]	VIPRE_CLKCFG_LOCK	RW	vipre_clkcfg_lock Value After Reset: 0x0
[7:1]	RESERVED_1	-	
[0]	TEST_CLK_CFG_LOCK	RW	test_clk_cfg_lock Value After Reset: 0x0

4.4.2.6 VO_SUBSYS

4.4.2.6.1 VOSYS_CLK_GATE

- Description: Clock gate register
- Offset: 0x50
- Default Value: 0xfbfffc01

Bits	Field Name	Access	Description
[31]	CLKCTRL_MIPIDSI1_PIXCLK_EN	RW	MIPI_DSI1 pixel clk clkctrl_mipidsi1_pixclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[30]	CLKCTRL_MIPIDSI0_PIXCLK_EN	RW	MIPI_DSI0 pixel clk clkctrl_mipidsi0_pixclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[29]	CLKCTRL_IOPMP_GPU_ACLK_EN	RW	IOPMP_GPU aclk clkctrl_iopmp_gpu_aclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[28]	CLKCTRL_IOPMP_DPU_ACLK_EN	RW	IOPMP_DPU aclk clkctrl_iopmp_dpu_aclk_en 0: Clock gate.

Bits	Field Name	Access	Description
			1: Clock open. Value After Reset: 0x1
[27]	CLKCTRL_IOPMP_DPU1_ACLK_EN	RW	IOPMP_DPU1 aclk clkctrl_iopmp_dpu1_aclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[26]	RESERVED_2	-	
[25]	CLKCTRL_IOPMP_VOSYS_GPU_PCLK_EN	RW	IOPMP_GPU pclk clkctrl_iopmp_vosys_gpu_pclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[24]	CLKCTRL_IOPMP_VOSYS_DPU1_PCLK_EN	RW	IOPMP_DPU1 pclk clkctrl_iopmp_vosys_dpu1_pclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[23]	CLKCTRL_IOPMP_VOSYS_DPU_PCLK_EN	RW	IOPMP_DPU pclk clkctrl_iopmp_vosys_dpu_pclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[22]	CLKCTRL_AXI4_VO_PCLK_EN	RW	VO_CFG bus pclk clkctrl_axi4_vo_pclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[21]	CLKCTRL_X2H_DPU_ACLK_EN	RW	VO_CFG bus pclk clkctrl_axi4_vo_pclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[20]	CLKCTRL_X2H_DPU1_ACLK_EN	RW	X2H for DPU 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[19]	CLKCTRL_HDMI_I2S_CLK_EN	RW	X2H for DPU1 0: Clock gate.

Bits	Field Name	Access	Description
			1: Clock open. Value After Reset: 0x1
[18]	CLKCTRL_MIPI_DSI1_REFCLK_EN	RW	MIPI_DSI1 reference clock clkctrl_mipi_dsi1_refclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[17]	CLKCTRL_MIPI_DSI0_REFCLK_EN	RW	MIPI_DSI0 reference clock clkctrl_mipi_dsi0_refclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[16]	CLKCTRL_MIPI_DSI1_CFG_CLK_EN	RW	MIPI_DSI1 configuration clock clkctrl_mipi_dsi1_cfg_clk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[15]	CLKCTRL_MIPI_DSI0_CFG_CLK_EN	RW	MIPI_DSI0 configuration clock clkctrl_mipi_dsi0_cfg_clk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[14]	CLKCTRL_MIPI_DSI1_PCLK_EN	RW	MIPI_DSI1 pclk clkctrl_mipi_dsi1_pclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[13]	CLKCTRL_MIPI_DSI0_PCLK_EN	RW	MIPI_DSI0 pclk clkctrl_mipi_dsi0_pclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[12]	CLKCTRL_HDMI_CEC_CLK_EN	RW	HDMI iec clk clkctrl_hdmi_cec_clk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[11]	CLKCTRL_HDMI_PCLK_EN	RW	HDMI pclk clkctrl_hdmi_pclk_en 0: Clock gate.

Bits	Field Name	Access	Description
			1: Clock open. Value After Reset: 0x1
[10]	CLKCTRL_HDMI_SFR_CLK_EN	RW	HDMI sfr clk clkctrl_hdmi_sfr_clk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[9]	CLKCTRL_DPU_CCLK_EN	RW	DPU cclk clkctrl_dpu_cclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x0
[8]	CLKCTRL_DPU_ACLK_EN	RW	DPU aclk clkctrl_dpu_aclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x0
[7]	CLKCTRL_DPU_HCLK_EN	RW	DPU hclk clkctrl_dpu_hclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x0
[6]	CLKCTRL_DPU_PIXELCLK1_EN	RW	DPU pixel clock1 clkctrl_dpu_pixelclk1_en 0: Clock gate. 1: Clock open. Value After Reset: 0x0
[5]	CLKCTRL_DPU_PIXELCLK0_EN	RW	DPU pixel clock0 clkctrl_dpu_pixelclk0_en 0: Clock gate. 1: Clock open. Value After Reset: 0x0
[4]	CLKCTRL_GPU_CFG_ACLK_EN	RW	GPU config aclk clkctrl_gpu_cfg_aclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x0
[3]	CLKCTRL_GPU_CORE_CLK_EN	RW	GPU core clk clkctrl_gpu_core_clk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x0

Bits	Field Name	Access	Description
[2]	CLKCTRL_GPU_MEM_CLK_EN	RW	Reserved Value After Reset: 0x0
[1]	RESERVED_1	-	
[0]	CLKCTRL_AXI4_VO_ACLK_EN	RW	AXI_VO bus aclk clkctrl_axi4_vo_aclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1

4.4.2.6.2 VOSYS_CLK_GATE1

- Description: HDMI pixclk gate register
- Offset: 0x54
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	CLKCTRL_HDMI_PIXCLK_EN	RW	HDMI pixclk clkctrl_hdmi_pixclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1

4.4.2.6.3 VOSYS_DPU_CCLK_CFG

- Description: DPU core clock divider register
- Offset: 0x64
- Default Value: 0x13

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VOSYS_DPU_CCLK_DIV_EN	RW	DPU core clock divider enable, software needs to be pulled low and then pulled high. Value After Reset: 0x1
[3:0]	VOSYS_DPU_CCLK_DIV_NUM	RW	DPU core clock divider ratio 4'd1: 1:1 4'd2: 1:2 4'd3: 1:3, 792Mhz .....

Bits	Field Name	Access	Description
			4'd15: 1:15 Value After Reset: 0x3

4.4.2.6.4 TEST_CLK_FREQ_STAT

- Description: Clock frequency register
- Offset: 0xc4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	TEST_CLK_FREQ_STAT	RO	clk_calc output freq_stat

4.4.2.6.5 TEST_CLK_CFG

- Description: Clock sample control register
- Offset: 0xc8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:4]	TEST_CLK_SEL	RW	0: vosys_dpu_cclk 1: vosys_apb pclk
[3:1]	RESERVED_1	-	
[0]	TEST_CLK_SAMPLE_EN	RW	clk_calc sample enable

4.4.2.6.6 VOSYS_CLK_GATE_TEE

- Description: Clock enable TEE register
- Offset: 0x1050
- Default Value: 0xfbfffc01

Bits	Field Name	Access	Description
[31]	CLKCTRL_MIPIDSI1_PIXCLK_EN	RW	MIPI_DSI1 pixel clock clkctrl_mipidsi1_pixclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[30]	CLKCTRL_MIPIDSI0_PIXCLK_EN	RW	MIPI_DSI0 pixel clock clkctrl_mipidsi0_pixclk_en 0: Clock gate. 1: Clock open.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[29]	CLKCTRL_IOPMP_GPU_ACLK_EN	RW	IOPMP_GPU aclk clkctrl_iopmp_gpu_aclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[28]	CLKCTRL_IOPMP_DPU_ACLK_EN	RW	IOPMP_DPU aclk clkctrl_iopmp_dpu_aclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[27]	CLKCTRL_IOPMP_DPU1_ACLK_EN	RW	IOPMP_DPU1 aclk clkctrl_iopmp_dpu1_aclk_en 0: Clock gate. 1: Cock open. Value After Reset: 0x1
[26]	RESERVED_2	-	
[25]	CLKCTRL_IOPMP_VOSYS_GPU_PCLK_EN	RW	IOPMP_GPU pclk clkctrl_iopmp_vosys_gpu_pclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[24]	CLKCTRL_IOPMP_VOSYS_DPU1_PCLK_EN	RW	IOPMP_DPU1 pclk clkctrl_iopmp_vosys_dpu1_pclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[23]	CLKCTRL_IOPMP_VOSYS_DPU_PCLK_EN	RW	IOPMP_DPU pclk clkctrl_iopmp_vosys_dpu_pclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[22]	CLKCTRL_AXI4_VO_PCLK_EN	RW	VO_CFG bus pclk clkctrl_axi4_vo_pclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[21]	CLKCTRL_X2H_DPU_ACLK_EN	RW	X2H for DPU 0: Clock gate. 1: Clock open.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[20]	CLKCTRL_X2H_DPU1_ACLK_EN	RW	X2H for DPU1 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[19]	CLKCTRL_HDMI_I2S_CLK_EN	RW	HDMI I2S clock clkctrl_hdmi_i2s_clk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[18]	CLKCTRL_MIPI_DSI1_REFCLK_EN	RW	MIPI_DSI1 ref clk clkctrl_mipi_dsi1_refclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[17]	CLKCTRL_MIPI_DSI0_REFCLK_EN	RW	MIPI_DSI0 reference clock clkctrl_mipi_dsi0_refclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[16]	CLKCTRL_MIPI_DSI1_CFG_CLK_EN	RW	MIPI_DSI1 configuration clock clkctrl_mipi_dsi1_cfg_clk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[15]	CLKCTRL_MIPI_DSI0_CFG_CLK_EN	RW	MIPI_DSI0 configuration clock clkctrl_mipi_dsi0_cfg_clk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[14]	CLKCTRL_MIPI_DSI1_PCLK_EN	RW	MIPI_DSI1 pclk clkctrl_mipi_dsi1_pclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[13]	CLKCTRL_MIPI_DSI0_PCLK_EN	RW	MIPI_DSI0 pclk clkctrl_mipi_dsi0_pclk_en 0: Clock gate. 1: Clock open.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[12]	CLKCTRL_HDMI_CEC_CLK_EN	RW	HDMI CEC clock clkctrl_hdmi_cec_clk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[11]	CLKCTRL_HDMI_PCLK_EN	RW	HDMI pclk clkctrl_hdmi_pclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[10]	CLKCTRL_HDMI_SFR_CLK_EN	RW	HDMI SFR clock clkctrl_hdmi_sfr_clk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1
[9]	CLKCTRL_DPU_CCLK_EN	RW	DPU cclk clkctrl_dpu_cclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x0
[8]	CLKCTRL_DPU_ACLK_EN	RW	DPU aclk clkctrl_dpu_aclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x0
[7]	CLKCTRL_DPU_HCLK_EN	RW	DPU hclk clkctrl_dpu_hclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x0
[6]	CLKCTRL_DPU_PIXELCLK1_EN	RW	DPU pixel clock1 clkctrl_dpu_pixelclk1_en 0: Clock gate. 1: Clock open. Value After Reset: 0x0
[5]	CLKCTRL_DPU_PIXELCLK0_EN	RW	DPU pixel clock0 clkctrl_dpu_pixelclk0_en 0: Clock gate. 1: Clock open. Value After Reset: 0x0

Bits	Field Name	Access	Description
[4]	CLKCTRL_GPU_CFG_ACLK_EN	RW	GPU configuration aclk clkctrl_gpu_cfg_aclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x0
[3]	CLKCTRL_GPU_CORE_CLK_EN	RW	GPU core clock clkctrl_gpu_core_clk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x0
[2]	CLKCTRL_GPU_MEM_CLK_EN	RW	GPU memclk clkctrl_gpu_mem_clk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x0
[1]	RESERVED_1	-	
[0]	CLKCTRL_AXI4_VO_ACLK_EN	RW	AXI_VO bus aclk clkctrl_axi4_vo_aclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1

4.4.2.6.7 VOSYS_CLK_GATE1_TEE

- Description: HDMI pixel clock enable TEE register
- Offset: 0x1054
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	CLKCTRL_HDMI_PIXCLK_EN	RW	HDMI pixclk clkctrl_hdmi_pixclk_en 0: Clock gate. 1: Clock open. Value After Reset: 0x1

4.4.2.6.8 VOSYS_DPU_CCLK_CFG_TEE

- Description: DPU core clock divider TEE register
- Offset: 0x1064
- Default Value: 0x13

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VOSYS_DPU_CCLK_DIV_EN	RW	DPU core clock divider enable, software needs to be pulled low and then pulled high. Value After Reset: 0x1
[3:0]	VOSYS_DPU_CCLK_DIV_NUM	RW	DPU core clock divider ratio 4'd1: 1:1 4'd2: 1:2 ..... 4'd15: 1:15 Value After Reset: 0x3

4.4.2.6.9 TEST_CLK_FREQ_STAT_TEE

- Description: Clock frequency TEE register
- Offset: 0x10c4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	TEST_CLK_FREQ_STAT	RO	clk_calc output freq_stat

4.4.2.6.10 TEST_CLK_CFG_TEE

- Description: Clock sample control TEE register
- Offset: 0x10c8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:4]	TEST_CLK_SEL	RW	0: vosys_dpu_cclk 1: vosys_apb pclk
[3:1]	RESERVED_1	-	
[0]	TEST_CLK_SAMPLE_EN	RW	clk_calc sample enable

4.4.2.6.11 CFG_LOCK_TEE

- Description: Configure lock TEE register
- Offset: 0x1a00
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7]	DPU_ADDR_REMAP_LOCK	RW	DPU address remap lock Value After Reset: 0x0
[6]	VO_SUBSYS_CFG_LOCK	RW	VO subsystem bus configuration lock Value After Reset: 0x0
[5]	TEST_CLK_CFG_LOCK	RW	test_clk configuration lock for clk_calc module Value After Reset: 0x0
[4]	MIPI_DSI1_CFG_LOCK	RW	MIPI_DSI1 module configuration lock Value After Reset: 0x0
[3]	MIPI_DSI0_CFG_LOCK	RW	MIPI_DSI0 module configuration lock Value After Reset: 0x0
[2]	HDMI_CFG_LOCK	RW	HDMI module configuration lock Value After Reset: 0x0
[1]	GPU_CFG_LOCK	RW	GPU module configuration lock Value After Reset: 0x0
[0]	DPU_CFG_LOCK	RW	DPU module configuration lock Value After Reset: 0x0

4.4.2.7 VP_SUBSYS

4.4.2.7.1 VPSYS_CK_CFG

- Description: VPSYS_CK_CFG
- Offset: 0x20
- Default Value: 0x3ff

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9]	VPSYS_VENC_PCLK_EN	RW	VENC APB clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[8]	VPSYS_VENC_CCLK_EN	RW	vENC core clock enable 1: Clock enable. 0: Clock disable.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[7]	VPSYS_VENC_ACLK_EN	RW	VENC AXI clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[6]	VPSYS_VDEC_PCLK_EN	RW	VDEC APB clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[5]	VPSYS_VDEC_CCLK_EN	RW	VDEC core clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[4]	VPSYS_VDEC_ACLK_EN	RW	VDEC AXI clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[3]	VPSYS_G2D_CLK_EN	RW	G2D clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[2]	VPSYS_FCE_CLK_EN	RW	FCE clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[1]	VPSYS_AXI_ACLK_EN	RW	VPSYS AXI clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[0]	VPSYS_CLK_EN	RW	VPSYS all clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1

4.4.2.7.2 VPSYS_VDEC_CCLK_CFG

- Description: VPSYS_VDEC_CCLK_CFG
- Offset: 0x24
- Default Value: 0x14

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VPSYS_VDEC_CCLK_DIV_EN	RW	Video PLL FOUTVCO divider enable, software needs to be pulled low then high. Value After Reset: 0x1
[3:0]	VPSYS_VDEC_CCLK_DIV_NUM	RW	Video PLL FOUTVCO clock's divider ratio, for VDEC 4'd4: 1:4 ..... 4'd15: 1:15 Value After Reset: 0x4

4.4.2.7.3 VPSYS_FCE_CCLK_CFG

- Description: VPSYS_FCE_CCLK_CFG
- Offset: 0x2c
- Default Value: 0x13

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VPSYS_FCE_CCLK_DIV_EN	RW	Video PLL FOUTVCO divider enable, software needs to be pulled low then high. Value After Reset: 0x1
[3:0]	VPSYS_FCE_CCLK_DIV_NUM	RW	Video PLL FOUTVCO clock's divider ratio, for FCE 4'd3: 1:3 ..... 4'd15: 1:15 Value After Reset: 0x3

4.4.2.7.4 VPSYS_G2D_CCLK_CFG

- Description: VPSYS_G2D_CCLK_CFG
- Offset: 0x30
- Default Value: 0x13

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VPSYS_G2D_CCLK_DIV_EN	RW	Video PLL FOUTVCO divider enable, software needs to be pulled low then high. Value After Reset: 0x1
[3:0]	VPSYS_G2D_CCLK_DIV_NUM	RW	Video PLL FOUTVCO clock's divider ratio, for G2D 4'd3: 1:3 ..... 4'd15: 1:15 Value After Reset: 0x3

4.4.2.7.5 VPSYS_FREQM_CFG

- Description: VPSYS_FREQM_CFG
- Offset: 0x50
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	TEST_CLK_SAMPLE_EN	RW	Frequency meter enable Value After Reset: 0x0
[3:0]	TEST_CLK_SEL	RW	Select clock source to frequency monitor 'd0: FCE clock 'd1: G2D core clock 'd2: VDEC core clock 'd3: VPSYS AXI clock 'd4: VPSYS APB pclk Value After Reset: 0x0

4.4.2.7.6 VPSYS_FREQ_STS

- Description: VPSYS_FREQ_STS
- Offset: 0x54
- Default Value: 0x8

Bits	Field Name	Access	Description
[31:0]	TEST_CLK_FREQ_STAT	RO	Frequency indicator Value After Reset: 0x0

4.4.2.7.7 VPSYS_CK_TEECFG

- Description: VPSYS_CK_TEECFG
- Offset: 0x1020
- Default Value: 0x3ff

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9]	VPSYS_VENC_PCLK_EN	RW	VENC APB clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[8]	VPSYS_VENC_CCLK_EN	RW	VENC core clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[7]	VPSYS_VENC_ACLK_EN	RW	VENC AXI clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[6]	VPSYS_VDEC_PCLK_EN	RW	VDEC APB clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[5]	VPSYS_VDEC_CCLK_EN	RW	VDEC core clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[4]	VPSYS_VDEC_ACLK_EN	RW	VDEC AXI clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[3]	VPSYS_G2D_CLK_EN	RW	G2d clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1

Bits	Field Name	Access	Description
[2]	VPSYS_FCE_CLK_EN	RW	FCE clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[1]	VPSYS_AXI_ACLK_EN	RW	VPSYS AXI clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1
[0]	VPSYS_CLK_EN	RW	VPSYS all clock enable 1: Clock enable. 0: Clock disable. Value After Reset: 0x1

4.4.2.7.8 VPSYS_VDEC_CCLK_TEECFG

- Description: VPSYS_VDEC_CCLK_TEECFG
- Offset: 0x1024
- Default Value: 0x14

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VPSYS_VDEC_CCLK_DIV_EN	RW	Video PLL FOUTVCO divider enable, software needs to be pulled low then high. Value After Reset: 0x1
[3:0]	VPSYS_VDEC_CCLK_DIV_NUM	RW	Video PLL FOUTVCO clock's divider ratio, for VDEC 4'd4: 1:4 ..... 4'd15: 1:15 Value After Reset: 0x4

4.4.2.7.9 VPSYS_FCE_CCLK_TEECFG

- Description: VPSYS_FCE_CCLK_TEECFG
- Offset: 0x102c
- Default Value: 0x13

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	

Bits	Field Name	Access	Description
[4]	VPSYS_FCE_CCLK_DIV_EN	RW	Video PLL FOUTVCO divider enable, software needs to be pulled low then high. Value After Reset: 0x1
[3:0]	VPSYS_FCE_CCLK_DIV_NUM	RW	Video PLL FOUTVCO clock's divider ratio, for FCE 4'd3: 1:3 ..... 4'd15: 1:15 Value After Reset: 0x3

4.4.2.7.10 VPSYS_G2D_CCLK_TEECFG

- Description: VPSYS_G2D_CCLK_TEECFG
- Offset: 0x1030
- Default Value: 0x13

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VPSYS_G2D_CCLK_DIV_EN	RW	Video PLL FOUTVCO divider enable, software needs to be pulled low then high. Value After Reset: 0x1
[3:0]	VPSYS_G2D_CCLK_DIV_NUM	RW	Video PLL FOUTVCO clock's divider ratio, for G2D 4'd3: 1:3 ..... 4'd15: 1:15 Value After Reset: 0x3

4.4.2.7.11 VPSYS_FREQM_TEECFG

- Description: VPSYS_FREQM_TEECFG
- Offset: 0x1050
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	TEST_CLK_SAMPLE_EN	RW	Frequency meter enable Value After Reset: 0x0
[3:0]	TEST_CLK_SEL	RW	Select clock source to frequency monitor 'd0: FCE clock

Bits	Field Name	Access	Description
			'd1: G2D core clock 'd2: VDEC core clock 'd3: VPSYS AXI clcok 'd4: VPSYS APB pclk Value After Reset: 0x0

4.4.2.7.12 VPSYS_FREQ_TEESTS

- Description: VPSYS_FREQ_TEESTS
- Offset: 0x1054
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	TEST_CLK_FREQ_STAT	RO	Frequency indicator Value After Reset: 0x0

4.4.2.7.13 VPSYS_ADDR_TEESEL

- Description: VPSYS_ADDR_TEESEL
- Offset: 0x1060
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_2	-	
[9]	G2D_RANK_SEL	RW	1: G2D access rank1: 4~(8GB-6MB) 0: G2D access rank0: 0~(4GB-6MB) Value After Reset: 0x0
[8]	G2D_REMAP_EN	RW	1: G2D address remap enable. 0: G2D address remap disable. Value After Reset: 0x0
[7:0]	RESERVED_1	-	

4.4.2.8 DSP_SUBSYS

4.4.2.8.1 DSP0_CLK_CFG

- Description: DSP0 clock configuration register
- Offset: 0x0
- Default Value: 0x10

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	DSPSYS_DSP0_CCLK_CDE_SYNC	RW	dsp0_cclk's divider enable, software needs to be pulled low and then pulled high. (dsp0_cclk is from dsp clk and gmac_pll_foutpostdiv) Value After Reset: 0x1
[3]	RESERVED_1	-	
[2:0]	DSPSYS_DSP0_CCLK_CDE_RATIO	RW	dsp0_sclk's divider ratio 3'd0: 1:1 (1Ghz if dspsys_dsp0_clk_switch_switch_ sel=0, 792Mhz if dspsys_dsp0_clk_switch_switch_sel =1) 3'd1: 1:2 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.8.2 DSP1_CLK_CFG

- Description: DSP1 clock configuration register
- Offset: 0x4
- Default Value: 0x10

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	DSPSYS_DSP1_CCLK_CDE_SYNC	RW	dsp1_cclk's divider enable, software needs to be pulled low and then pulled high. (dsp1_cclk is from dsp clk and gmac_pll_foutpostdiv) Value After Reset: 0x1
[3]	RESERVED_1	-	
[2:0]	DSPSYS_DSP1_CCLK_CDE_RATIO	RW	dsp1_sclk's divider ratio 3'd0: 1:1 (1Ghz if dspsys_dsp1_clk_switch_switch_ sel=0, 792Mhz if dspsys_dsp1_clk_switch_switch_sel =1) 3'd1: 1:2 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.8.3 DSP_CLK_CFG

- Description: DSP clock configuration register
- Offset: 0x8
- Default Value: 0x7

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	DSPSYS_DSP_CLK_DIV_EN	RW	DSP clock's divider enable. Software needs to be pulled low and then pulled high. (DSP clock is from video_pll_foutvco(2376Mhz divided by 3)) Value After Reset: 0x1
[1:0]	DSPSYS_DSP_CLK_DIV_NUM	RW	DSP clock's divider ratio of video_pll_foutvco 2'd3: 1:3, 792Mhz ..... Value After Reset: 0x3

4.4.2.8.4 DSP0_BUS_SCLK_CFG

- Description: DSP0 slave bus clock configuration register
- Offset: 0xc
- Default Value: 0x8

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSPSYS_DSP0_SCLK_CDE_SYNC	RW	dsp0_sclk's divider enable, software needs to be pulled low and then pulled high. Value After Reset: 0x1
[2:0]	DSPSYS_DSP0_SCLK_CDE_RATIO	RW	dsp0_sclk's divider ratio 3'd0: 1:1 3'd1: 1:2 3'd2: 1:3 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.8.5 DSP0_BUS_MCLK_CFG

- Description: DSP0 master bus clock configuration register
- Offset: 0x10
- Default Value: 0x8

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSPSYS_DSP0_MCLK_CDE_SYNC	RW	dsp0_mclk's divider enable, software needs to be pulled low and then pulled high. Value After Reset: 0x1
[2:0]	DSPSYS_DSP0_MCLK_CDE_RATIO	RW	dsp0_mclk's divider ratio 3'd0: 1:1 3'd1: 1:2 3'd2: 1:3 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.8.6 DSP1_BUS_SCLK_CFG

- Description: DSP1 slave bus clock configuration register
- Offset: 0x14
- Default Value: 0x8

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSPSYS_DSP1_SCLK_CDE_SYNC	RW	dsp1_sclk's divider enable, software needs to be pulled low and then pulled high. Value After Reset: 0x1
[2:0]	DSPSYS_DSP1_SCLK_CDE_RATIO	RW	dsp1_sclk's divider ratio 3'd0: 1:1 3'd1: 1:2 3'd2: 1:3 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.8.7 DSP1_BUS_MCLK_CFG

- Description: DSP1 master bus clock configuration register
- Offset: 0x18
- Default Value: 0x8

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSPSYS_DSP1_MCLK_CDE_SYNC	RW	dsp1_mclk's divider enable, software needs to be pulled low and then pulled high. Value After Reset: 0x1
[2:0]	DSPSYS_DSP1_MCLK_CDE_RATIO	RW	dsp1_mclk's divider ratio 3'd0: 1:1 3'd1: 1:2 3'd2: 1:3 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.8.8 DSP0_BUS_CLK_CFG1

- Description: DSP0 clock switch register
- Offset: 0x1c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	DSPSYS_DSP0_CLK_SWITCH_SWITCH_SEL	RW	dsp0_clk_switch select 0: Select gmac_pll_foutpostdiv (1Ghz) 1: dspsys_dsp_clk (792Mhz) Value After Reset: 0x0

4.4.2.8.9 DSP1_BUS_CLK_CFG1

- Description: DSP1 clock switch register
- Offset: 0x20
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	DSPSYS_DSP1_CLK_SWITCH_SWITCH_SEL	RW	dsp1_clk_switch select 0: Select gmac_pll_foutpostdiv (1Ghz) 1: dspsys_dsp_clk (792Mhz) Value After Reset: 0x0

4.4.2.8.10 DSPSYS_CLK_GATE_EN_1

- Description: DSP subsystem clock enable register
- Offset: 0x24
- Default Value: 0x1b000f0

Bits	Field Name	Access	Description
[31:25]	RESERVED_3	-	
[24]	CLKCTRL_AXI4_DSPSYS_PCLK_EN	RW	axi4_dspsys bus pclk enable, active high Value After Reset: 0x1
[23]	CLKCTRL_AXI4_DSPSYS_ACLK_EN	RW	axi4_dspsys bus aclk enable, active high Value After Reset: 0x1
[22]	RESERVED_2	-	
[21]	CLKCTRL_AXI4_DSPSYS_SLV_PCLK_EN	RW	axi4_dspsys_slv bus pclk enable, active high Value After Reset: 0x1
[20]	CLKCTRL_AXI4_DSPSYS_SLV_ACLK_EN	RW	axi4_dspsys_slv bus aclk enable, active high Value After Reset: 0x1
[19:8]	RESERVED_1	-	
[7]	CLKCTRL_X2X_X4_DSPSLV_DSP0_ACLK_M_EN	RW	x2x_x4_dspslv_dsp0 bus aclk enable, active high Value After Reset: 0x1
[6]	CLKCTRL_X2X_X4_DSPSLV_DSP1_ACLK_M_EN	RW	x2x_x4_dspslv_dsp1 bus aclk enable, active high Value After Reset: 0x1
[5]	CLKCTRL_X2X_DSP0_ACLK_S_EN	RW	x2x_dsp0 aclk enable, active high Value After Reset: 0x1
[4]	CLKCTRL_X2X_DSP2_ACLK_S_EN	RW	x2x_dsp2 aclk enable, active high Value After Reset: 0x1
[3]	CLKCTRL_DSP0_CCLK_EN	RW	DSP0 cclk enable, active high Value After Reset: 0x0
[2]	CLKCTRL_DSP1_CCLK_EN	RW	DSP1 cclk enable, active high Value After Reset: 0x0
[1]	CLKCTRL_DSP1_PCLK_EN	RW	DSP1 pclk enable, active high Value After Reset: 0x0
[0]	CLKCTRL_DSP0_PCLK_EN	RW	DSP0 pclk enable, active high Value After Reset: 0x0

4.4.2.8.11 TEST_CLK_FREQ_STAT

- Description: Clock frequency register
- Offset: 0x2c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	TEST_CLK_FREQ_STAT	RO	clk_calc output freq_stat

4.4.2.8.12 TEST_CLK_CFG

- Description: Clock sample control register
- Offset: 0x30
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:4]	TEST_CLK_SEL	RW	clk_calc clock select 0: dspsys_dsp0_cde 1: dspsys_dsp0_mclk_cde 2: dspsys_dsp0_sclk_cde 3: dspsys_dsp1_cde 4: dspsys_dsp1_mclk_cde 5: dspsys_dsp1_sclk_cde
[3:1]	RESERVED_1	-	
[0]	TEST_CLK_SAMPLE_EN	RW	clk_calc sample enable

4.4.2.8.13 DSP0_CLK_CFG_TEE

- Description: DSP0 clock configuration TEE register
- Offset: 0x1000
- Default Value: 0x10

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	DSPSYS_DSP0_CCLK_CDE_SYNC	RW	dsp0_cclk's divider enable. Software needs to be pulled low and then pulled high. (dsp0_cclk is from dsp clk and gmac_pll_foutpostdiv) Value After Reset: 0x1
[3]	RESERVED_1	-	

Bits	Field Name	Access	Description
[2:0]	DSPSYS_DSP0_CCLK_CDE_RATIO	RW	dsp0_sclk's divider ratio 3'd0: 1:1 (1Ghz if dspsys_dsp0_clk_switch_switch_ Sel = 0, 792Mhz if dspsys_dsp0_clk_switch_switch_sel = 1) 3'd1: 1:2 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.8.14 DSP1_CLK_CFG_TEE

- Description: DSP1 clock configuration TEE register
- Offset: 0x1004
- Default Value: 0x10

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	DSPSYS_DSP1_CCLK_CDE_SYNC	RW	dsp1_cclk's divider enable. Software needs to be pulled low and then pulled high. (dsp1_cclk is from DSP clock and gmac_pll_foutpostdiv) Value After Reset: 0x1
[3]	RESERVED_1	-	
[2:0]	DSPSYS_DSP1_CCLK_CDE_RATIO	RW	dsp1_sclk's divider ratio 3'd0: 1:1 (1Ghz if dspsys_dsp1_clk_switch_switch_ Sel = 0, 792Mhz dspsys_dsp1_clk_switch_switch_sel = 1) 3'd1: 1:2 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.8.15 DSP_CLK_CFG_TEE

- Description: DSP clock configuration TEE register
- Offset: 0x1008
- Default Value: 0x7

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	

[2]	DSPSYS_DSP_CLK_DIV_EN	RW	DSP clock's divider enable. Software needs to be pulled low and then pulled high. (DSP clock is from video_pll_foutvco (2376Mhz divided by 3)) Value After Reset: 0x1
[1:0]	DSPSYS_DSP_CLK_DIV_NUM	RW	DSP clock's divider ratio of video_pll_foutvco 2'd3: 1:3, 792Mhz ..... Value After Reset: 0x3

4.4.2.8.16 DSP0_BUS_SCLK_CFG_TEE

- Description: DSP0 slave bus clock configuration TEE register
- Offset: 0x100c
- Default Value: 0x8

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSPSYS_DSP0_SCLK_CDE_SYNC	RW	dsp0_sclk's divider enable, software needs to be pulled low and then pulled high. Value After Reset: 0x1
[2:0]	DSPSYS_DSP0_SCLK_CDE_RATIO	RW	dsp0_sclk's divider ratio 3'd0: 1:1 3'd1: 1:2 3'd2: 1:3 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.8.17 DSP0_BUS_MCLK_CFG_TEE

- Description: DSP0 master bus clock configuration TEE register
- Offset: 0x1010
- Default Value: 0x8

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSPSYS_DSP0_MCLK_CDE_SYNC	RW	dsp0_mclk's divider enable, software needs to be pulled low and then pulled high. Value After Reset: 0x1
[2:0]	DSPSYS_DSP0_MCLK_CDE_RATI	RW	dsp0_mclk's divider ratio

Bits	Field Name	Access	Description
	O		3'd0: 1:1 3'd1: 1:2 3'd2: 1:3 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.8.18 DSP1_BUS_SCLK_CFG_TEE

- Description: DSP1 slave bus clock configuration TEE register
- Offset: 0x1014
- Default Value: 0x8

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSPSYS_DSP1_SCLK_CDE_SYNC	RW	dsp1_sclk's divider enable, software needs to be pulled low and then pulled high. Value After Reset: 0x1
[2:0]	DSPSYS_DSP1_SCLK_CDE_RATIO	RW	dsp1_sclk's divider ratio 3'd0: 1:1 3'd1: 1:2 3'd2: 1:3 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.8.19 DSP1_BUS_MCLK_CFG_TEE

- Description: DSP1 master bus clock configuration TEE register
- Offset: 0x1018
- Default Value: 0x8

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSPSYS_DSP1_MCLK_CDE_SYNC	RW	dsp1_mclk's divider enable, software needs to be pulled low and then pulled high. Value After Reset: 0x1
[2:0]	DSPSYS_DSP1_MCLK_CDE_RATI	RW	dsp1_mclk's divider ratio

Bits	Field Name	Access	Description
	O		3'd0: 1:1 3'd1: 1:2 3'd2: 1:3 ..... 3'd7: 1:8 Value After Reset: 0x0

4.4.2.8.20 DSP0_BUS_CLK_CFG1_TEE

- Description: DSP0 clock switch TEE register
- Offset: 0x101c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	DSPSYS_DSP0_CLK_SWITCH_SWITCH_SEL	RW	dsp0_clk_switch select 0: Select gmac_pll_foutpostdiv 1: dspsys_dsp_isp_clk Value After Reset: 0x0

4.4.2.8.21 DSP1_BUS_CLK_CFG1_TEE

- Description: DSP1 clock switch TEE register
- Offset: 0x1020
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	DSPSYS_DSP1_CLK_SWITCH_SWITCH_SEL	RW	dsp1_clk_switch select 0: Select gmac_pll_foutpostdiv 1: dspsys_dsp_isp_clk Value After Reset: 0x0

4.4.2.8.22 DSPSYS_CLK_GATE_EN_1_TEE

- Description: DSP subsystem clock enable TEE register
- Offset: 0x1024
- Default Value: 0x7b000f0

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	
[26]	CLKCTRL_IOPMP_DSP0_PCLK_EN	RW	IOPMP DSP0 bus pclk enable Value After Reset: 0x1
[25]	CLKCTRL_IOPMP_DSP1_PCLK_EN	RW	IOPMP DSP1 bus pclk enable Value After Reset: 0x1
[24]	CLKCTRL_AXI4_DSPSYS_PCLK_EN	RW	axi4_dspsys bus pclk enable Value After Reset: 0x1
[23]	CLKCTRL_AXI4_DSPSYS_ACLK_EN	RW	axi4_dspsys bus aclk enable Value After Reset: 0x1
[22]	RESERVED_2	-	
[21]	CLKCTRL_AXI4_DSPSYS_SLV_PCLK_EN	RW	axi4_dspsys_slv bus pclk enable Value After Reset: 0x1
[20]	CLKCTRL_AXI4_DSPSYS_SLV_ACLK_EN	RW	axi4_dspsys_slv bus aclk enable Value After Reset: 0x1
[19:8]	RESERVED_1	-	
[7]	CLKCTRL_X2X_X4_DSPSLV_DSP0_ACLK_M_EN	RW	x2x_x4_dspslv_dsp0 bus aclk enable Value After Reset: 0x1
[6]	CLKCTRL_X2X_X4_DSPSLV_DSP1_ACLK_M_EN	RW	x2x_x4_dspslv_dsp1 bus aclk enable Value After Reset: 0x1
[5]	CLKCTRL_X2X_DSP0_ACLK_S_EN	RW	x2x_dsp0 aclk enable Value After Reset: 0x1
[4]	CLKCTRL_X2X_DSP2_ACLK_S_EN	RW	x2x_dsp2 aclk enable Value After Reset: 0x1
[3]	CLKCTRL_DSP0_CCLK_EN	RW	DSP0 cclk enable Value After Reset: 0x0
[2]	CLKCTRL_DSP1_CCLK_EN	RW	DSP1 cclk enable Value After Reset: 0x0
[1]	CLKCTRL_DSP1_PCLK_EN	RW	DSP0 pclk enable Value After Reset: 0x0
[0]	CLKCTRL_DSP0_PCLK_EN	RW	DSP1 pclk enable Value After Reset: 0x0

4.4.2.8.23 TEST_CLK_FREQ_STAT_TEE

- Description: Clock frequency TEE register
- Offset: 0x102c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	TEST_CLK_FREQ_STAT	RO	clk_calc output freq_stat

4.4.2.8.24 TEST_CLK_CFG_TEE

- Description: Clock sample control TEE register
- Offset: 0x1030
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:4]	TEST_CLK_SEL	RW	clk_calc clock select 0: dspsys_dsp0_cde 1: dspsys_dsp0_mclk_cde 2: dspsys_dsp0_sclk_cde 3: dspsys_dsp1_cde 4: dspsys_dsp1_mclk_cde 5: dspsys_dsp1_sclk_cde
[3:1]	RESERVED_1	-	
[0]	TEST_CLK_SAMPLE_EN	RW	clk_calc sample enable

4.4.2.8.25 RESERVED_REG_0_TEE

- Description: Reserved TEE register
- Offset: 0x1100
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_0	RW	Reserved Value After Reset: 0x0

4.4.2.8.26 RESERVED_REG_1_TEE

- Description: Reserved TEE register
- Offset: 0x1104
- Default Value: 0xffffffff

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_1	RW	Reserved Value After Reset: 0xFFFFFFFF

4.4.2.8.27 CFG_CLK_LOCK_TEE

- Description: Clock lock TEE register
- Offset: 0x1140
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_4	-	
[30]	DSP_SUBSYS_CLKCFG_LOCK	RW	dsp_subsys_clkcfg_lock Value After Reset: 0x0
[29:26]	RESERVED_3	-	
[25]	DSP_SUBSYS_SLV_CLKCFG_LOCK	RW	dsp_subsys_slv_clkcfg_lock Value After Reset: 0x0
[24:7]	RESERVED_2	-	
[6]	DSPSYS_CLKCFG_LOCK	RW	dspsys_clkcfg_lock Value After Reset: 0x0
[5]	DSP0_CLKCFG_LOCK	RW	dsp0_clkcfg_lock Value After Reset: 0x0
[4]	DSP1_CLKCFG_LOCK	RW	dsp1_clkcfg_lock Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	TEST_CLK_CFG_LOCK	RW	test_clk_cfg_lock Value After Reset: 0x0

4.4.2.8.28 CFG_RST_LOCK_TEE

- Description: Reset lock TEE register
- Offset: 0x1144
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_4	-	
[30]	DSP_SUBSYS_RSTCFG_LOCK	RW	dsp_subsys_rstcfg_lock

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[29:26]	RESERVED_3	-	
[25]	DSP_SUBSYS_SLV_RSTCFG_LOCK	RW	dsp_subsys_slv_rstcfg_lock Value After Reset: 0x0
[24:6]	RESERVED_2	-	
[5]	DSP0_RSTCFG_LOCK	RW	dsp0_rstcfg_lock Value After Reset: 0x0
[4]	DSP1_RSTCFG_LOCK	RW	dsp1_rstcfg_lock Value After Reset: 0x0
[3:0]	RESERVED_1	-	

4.4.2.8.29 CFG_DSPSYS_LOCK_TEE

- Description: DSP subsystem lock TEE register
- Offset: 0x1148
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_1	-	
[8]	DSP1_DDR_CH_SEL_LOCK	RW	dsp1_ddr_ch_sel_lock Value After Reset: 0x0
[7]	DSP0_DDR_CH_SEL_LOCK	RW	dsp0_ddr_ch_sel_lock Value After Reset: 0x0
[6]	DSP1_REMAP_LOCK	RW	dsp1_remap_lock Value After Reset: 0x0
[5]	DSP0_REMAP_LOCK	RW	dsp0_remap_lock Value After Reset: 0x0
[4]	DSPSYS_BUS_CFG_LOCK	RW	dspsys_bus_cfg_lock Value After Reset: 0x0
[3]	RESERVED_REG0_LOCK	RW	reserved_reg0_lock Value After Reset: 0x0
[2]	RESERVED_REG1_LOCK	RW	reserved_reg1_lock Value After Reset: 0x0
[1]	DSP0_BUS_CFG_LOCK	RW	dsp0_bus_cfg_lock

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[0]	DSP1_BUS_CFG_LOCK	RW	dsp1_bus_cfg_lock Value After Reset: 0x0

4.4.2.9 AUDIO_SUBSYS

4.4.2.9.1 SYS_CLK_DIV_REG

- Description: System clock divide select register
- Offset: 0x0
- Default Value: 0x124008

Bits	Field Name	Access	Description
[31:24]	RESERVED_3	-	
[23:20]	DMA_DIV	RW	DMA bus clock divider configuration, DMA clock frequency cannot exceed 410MHz. 0: No frequency division 1: 2 frequency division 2: 3 frequency division 3: 4 frequency division .. 15: 16 frequency division Value After Reset: 0x1
[19]	LPMD_APBCLK_CG	RW	APB bus clock CG control after preconfiguration system switches to LPMD. 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[18:16]	APB_DIV	RW	APB clock divider configuration, only supports even frequency division. 0: No frequency division 1: 2 frequency division 2: 4 frequency division 3: 6 frequency division .. 7: 14 frequency division Value After Reset: 0x2

Bits	Field Name	Access	Description
[15]	LPMD_AHBCLK_CG	RW	AHB bus clock CG control after preconfiguration system switches to LPMD. 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[14:12]	AHB_DIV	RW	AHB clock divider configuration, only supports even frequency division. 0: No frequency division 1: 2 frequency division 2: 4 frequency division 3: 6 frequency division .. 7: 14 frequency division Value After Reset: 0x4
[11]	RESERVED_2	-	
[10:8]	SYS_DIV	RW	AXI bus clock divider configuration 0: No frequency division 1: 2 frequency division 2: 3 frequency division 3: 4 frequency division .. 7: 14 frequency division Value After Reset: 0x0
[7]	RESERVED_1	-	
[6:4]	CPU_DIV	RW	CPU clock divider configuration 0: No frequency division 1: 2 frequency division 2: 3 frequency division 3: 4 frequency division .. 7: 8 frequency division Value After Reset: 0x0
[3]	LPMD_IOPMPCLK_CG	RW	IOPMP clock CG control after preconfiguration system switches to LPMD. 0: Clock off.

Bits	Field Name	Access	Description
			1: Turn on the clock. Value After Reset: 0x1
[2:1]	LPMD_SYSCLK_SEL	RW	System clock select after preconfiguration system switches to LPMD. 0: sys_clk uses 24MHz, clock on. 1: AXI bus and SRAM clock off. (In this configuration, CPU/SYS/DMA divider clock off) 2/3: Clock select and clock gate not change. Value After Reset: 0x0
[0]	SYS_CLK_SEL	RW	CPU clock source select. If source clock automatically switches to 24MHz in LPMD, the value will be automatically changed to 0. 0: 24MHz 1: cp_sys_clk Value After Reset: 0x0

4.4.2.9.2 PERI_DIV_SEL_REG

- Description: Peripheral working clock divider select register
- Offset: 0x4
- Default Value: 0x3f0725f

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	
[26:24]	GPIO_CLK_SEL	RW	GPIO debounce clock divider select 0: 1024kHz 1: 512Hz 2: 256Hz 3: 170Hz 4: 128Hz 5: 102Hz 6: 85Hz 7: 73Hz Value After Reset: 0x3
[23:20]	VAD_DIV	RW	VAD MCLK clock divider configuration 0: No frequency division 1: 2 frequency division

Bits	Field Name	Access	Description
			2: 3 frequency division 3: 4 frequency division ... 15: 16 frequency division Value After Reset: 0xF
[19:18]	RESERVED_2	-	
[17]	AUDIO_DIV1_CG	RW	AUDIO_DIVCLK1 clock divider CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[16:12]	AUDIO_DIV1	RW	AUDIO_DIVCLK1 clock divider configuration. This clock is one of source clocks of the audio interface working clock. 0: No frequency division 1: 2 frequency division 2: 3 frequency division 3: 4 frequency division ... 31: 32 frequency division Value After Reset: 0x7
[11:10]	RESERVED_1	-	
[9]	AUDIO_DIV0_CG	RW	AUDIO_DIVCLK0 clock divider CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x1
[8:4]	AUDIO_DIV0	RW	AUDIO_DIVCLK0 clock divider configuration. This clock is one of source clocks of the audio interface working clock. 0: No frequency division 1: 2 frequency division 2: 3 frequency division 3: 4 frequency division ... 31: 32 frequency division Value After Reset: 0x5

Bits	Field Name	Access	Description
[3:0]	UART_DIV	RW	UART working clock divider configuration 0: No frequency division 1: 2 frequency division 2: 3 frequency division 3: 4 frequency division ... 15: 16 frequency division Value After Reset: 0xF

4.4.2.9.3 PERI_CLK_SEL_REG

- Description: Audio peripheral clock source select register
- Offset: 0x8
- Default Value: 0x2000000

Bits	Field Name	Access	Description
[31:26]	RESERVED_7	-	
[25:24]	SPDIF_SRC_SEL	RW	SPDIF src_clk clock source select 0: CP_AUDIO_PLL 1: AUDIO_DIVCLK1 2: AUDIO_DIVCLK0 3: Reserved Value After Reset: 0x2
[23:22]	RESERVED_6	-	
[21:20]	VAD_MCLK_SEL	RW	VAD MCLK clock source select 0: AUDIO_DIVCLK 1: 24MHz 2~3: Reserved Value After Reset: 0x0
[19:18]	RESERVED_5	-	
[17:16]	TDM_SRC_SEL	RW	TDM src_clk clock source select 0: AUDIO_DIVCLK 1: 24MHz 2~3: Reserved Value After Reset: 0x0
[15:14]	RESERVED_4	-	

Bits	Field Name	Access	Description
[13:12]	I2S8CH_SRC_SEL	RW	I2S-8CH src_clk clock source select 0: AUDIO_DIVCLK 1: 24MHz 2~3: Reserved Value After Reset: 0x0
[11:10]	RESERVED_3	-	
[9:8]	I2S2_SRC_SEL	RW	I2S2 src_clk clock source select 0: AUDIO_DIVCLK 1: 24MHz 2~3: Reserved Value After Reset: 0x0
[7:6]	RESERVED_2	-	
[5:4]	I2S1_SRC_SEL	RW	I2S1 src_clk clock source select 0: AUDIO_DIVCLK 1: 24MHz 2~3: Reserved Value After Reset: 0x0
[3:2]	RESERVED_1	-	
[1:0]	I2S0_SRC_SEL	RW	I2S0 src_clk clock source select 0: AUDIO_DIVCLK 1: 24MHz 2~3: Reserved Value After Reset: 0x0

4.4.2.9.4 IP_CG_REG

- Description: Module CG control register
- Offset: 0x10
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:27]	RESERVED_2	-	
[26]	IOMUX_CG	RW	IOMUX clock CG control 0: Clock off. 1: Turn on the clock.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[25]	VAD_CG	RW	VAD clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[24]	SPDIF1_CG	RW	SPDIF1 clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[23]	SPDIF0_CG	RW	SPDIF0 clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[22]	GPIO_CG	RW	GPIO clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[21]	TDM_CG	RW	TDM clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[20]	I2S8CH_CG	RW	I2S-IN clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[19]	I2S2_CG	RW	I2S2 clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[18]	I2S1_CG	RW	I2S1 clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0

Bits	Field Name	Access	Description
[17]	I2S0_CG	RW	I2S0 clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[16]	UART_CG	RW	UART clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[15]	I2C1_CG	RW	I2C1 clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[14]	I2C0_CG	RW	I2C0 clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[13]	WDT_CG	RW	WDT clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[12]	TIMER_CNT4_CG	RW	TIMER counter 4 clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[11:0]	RESERVED_1	-	

4.4.2.9.5 TESTCLK_CTRL_REG

- Description: Test clock control register
- Offset: 0x98
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:23]	RESERVED_3	-	
[22]	M12_TESTCLK_CG	RW	12MHz test clock CG control

Bits	Field Name	Access	Description
			0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[21]	UART_TESTCLK_CG	RW	UART test clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[20]	AUDIO_TESTCLK_CG	RW	AUDIOCLK test clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[19]	AXI_TESTCLK_CG	RW	AXI bus test clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[18]	APB_TESTCLK_CG	RW	APB bus test clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[17]	AHB_TESTCLK_CG	RW	AHB bus test clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[16]	CPU_TESTCLK_CG	RW	CPU test clock CG control 0: Clock off. 1: Turn on the clock. Value After Reset: 0x0
[15:13]	RESERVED_2	-	
[12:8]	AHB_TESTCLK_DIV	RW	Clock configuration of AHB main frequency sent by CP to AP after frequency division. Frequency division factors: 8*(AHB_TESTCLK_DIV)+8 0: 8 frequency division 1: 16 frequency division

Bits	Field Name	Access	Description
			2: 24 frequency division ... 63: 512 frequency division Value After Reset: 0x0
[7:6]	RESERVED_1	-	
[5:0]	CPU_TESTCLK_DIV	RW	Clock configuration of C906 main frequency sent by CP to AP after frequency division. Frequency division factors: 8*(CPU_TESTCLK_DIV)+8 0: 8 frequency division 1: 16 frequency division 2: 24 frequency division ... 127: 1024 frequency division Value After Reset: 0x0

5 Reset

5.1 Overview

The reset management module is used to manage chip reset and reset of each function module, including:

- Management and control of power-on reset (POR)
- Control of system soft reset and function module soft reset
- Synchronizing reset signals to clock domains corresponding to each module
- Generating reset signals of each function module in the chip

5.2 Main Features

- Support POR reset.
- Support external reset.
- Support WDT reset.
- Support global soft reset and module soft reset.

5.3 Function Description

The system provides multiple reset modes. See Figure & Table 5-1 for source and application scope of each reset.

Figure & Table 5-1 Reset source

Reset Source	Description
POR Reset	After the chip is powered on, the reset output by POR module is asserted. When voltage of AONSYS core is detected to reach the threshold, reset is released. When voltage of AONSYS core is detected to be lower than the threshold, reset is asserted again, acting on the entire system.
External Reset	External key reset, acting on the entire system.
WDT Reset	WDT reset, acting on the entire system.
Software Reset	Software reset include global soft reset, abnormal reset, subsystem soft reset and module soft reset. Global soft reset and abnormal reset act on the entire system. Subsystem soft reset and module soft reset act on subsystems and modules.

5.3.1 POR

- Reset release power on detection threshold: DVDD18_AON 1.65V; DVDD08_AON 0.72V. Cannot be programmed with software.

- Reset assert power down detection threshold: DVDD18_AON 1.40V; DVDD08_AON 0.60V. Cannot be programmed with software.
- Reset delay time: The default is 2.56ms. Cannot be programmed with software.
- POR reset is multiplexed into IO for test in debug mode.
- POR reset bypass through the external pin POR_SEL.

5.3.2 External Reset

External reset refers to pin reset, which comes from external pin or PMIC. External reset of the chip comes from PMIC that will release reset after all power supplies are stable.

5.3.3 WDT Reset

There are four WDTs in the system. C910 TEE, C910 REE, C906, and E902 have one respectively. WDT reset acts on the entire system.

5.3.4 Software Reset

5.3.4.1 Global Soft Reset Request

The global soft reset request has the same priority with external reset, POR reset and WDT reset, and it will reset the entire chip. The global soft reset request can be masked. If the global soft reset request is not masked, software will pull it high to assert reset.

5.3.4.2 Subsystem and Module Soft Reset

Subsystem and module soft reset is used to reset subsystems and modules. Software needs to pull the reset signal low and then pull it high.
Soft reset control of each subsystem and module is shown in Figure & Table 5-2.

Figure & Table 5-2 Subsystem and module soft reset

SUBSYS	Module	SUBSYS Soft Reset 1	SUBSYS Soft Reset 2	Module Soft Reset 1	Module Soft Reset 2	Reset Name
AONSYS	RTC	N.A	N.A	SW_RTC_PRST_N	N.A	rstgen_rtc_prst_n
AONSYS	RTC	N.A	N.A	SW_RTC_CRST_N	N.A	rstgen_rtc_crst_n
AONSYS	AOGPIO	N.A	N.A	SW_AOGPIO_PRST_N	N.A	rstgen_aogpio_prst_n
AONSYS	AOGPIO	N.A	N.A	SW_AOGPIO_DBCLK_RST_N	N.A	rstgen_aogpio_dbclk_rst_n
AONSYS	AUDGPIO	N.A	N.A	SW_AUDGPIO_PRST_N	N.A	rstgen_gpio4_prst_n
AONSYS	AUDGPIO	N.A	N.A	SW_AUDGPIO_DBCLK_RST_N	N.A	rstgen_gpio4_dbrst_n
AONSYS	AOCPR	N.A	N.A	N.A	N.A	rstgen_aocpr_prst_n
AONSYS	AOAHB	N.A	N.A	N.A	N.A	rstgen_aoahb_hrst_n
AONSYS	AOSRAM	N.A	N.A	N.A	N.A	rstgen_aosram_hrst_n

SUBSYS	Module	SUBSYS Soft Reset 1	SUBSYS Soft Reset 2	Module Soft Reset 1	Module Soft Reset 2	Reset Name
AONSYS	E902	N.A	N.A	SW_E902_CRST_N	N.A	rstgen_e902_crst_n
AONSYS	E902	N.A	N.A	SW_E902_HAD_RST_N	N.A	rstgen_e902_had_rst_n
AONSYS	AOAPB	N.A	N.A	N.A	N.A	rstgen_aoapb_hrst_n
AONSYS	AOI2C	N.A	N.A	SW_AOI2C_PRST_N	N.A	rstgen_aoi2c_prst_n
AONSYS	PVTC	N.A	N.A	SW_PVTC_PRST_N	N.A	rstgen_pvtc_prst_n
AONSYS	AOTIMER	N.A	N.A	SW_AOTIMER_PRST_N	N.A	rstgen_aotimer_prst_n
AONSYS	AOTIMER	N.A	N.A	SW_AOTIMER_CRST_N	N.A	rstgen_aotimer_crst_n
AONSYS	AOWDT	N.A	N.A	SW_AOWDT_PRST_N	N.A	rstgen_aowdt_prst_n
AONSYS	ADC	N.A	N.A	SW_ADC_PRST_N	N.A	rstgen_adc_prst_n
AONSYS	AOUART	N.A	N.A	SW_AOUART_PRST_N	N.A	rstgen_aouart_prst_n
AONSYS	AOUART	N.A	N.A	SW_AOUART_S_RST_N	N.A	rstgen_aouart_s_rst_n
AUDIOSYS	AP2CP_BUS	N.A	sw_audio_rst_n	SW_AUDIO_SUBSYS_ARST_N_AP2CP	N.A	rstgen_audio_subsys_arst_n_ap2cp
AUDIOSYS	CP2AP_BUS	N.A	sw_audio_rst_n	SW_AUDIO_SUBSYS_ARST_N_CP2AP	N.A	rstgen_audio_subsys_arst_n_cp2ap
AUDIOSYS	CP2SRAM_BUS	N.A	sw_audio_rst_n	SW_AUDIO_SUBSYS_ARST_N_CP2SRAM	N.A	rstgen_audio_subsys_arst_n_cp2sram
AUDIOSYS	C906	N.A	sw_audio_rst_n	SW_AUDIO_SUBSYS_CRST_N	N.A	rstgen_audio_subsys_crst_n
AUDIOSYS	audio_subsys_iopmp	N.A	sw_audio_rst_n	SW_AUDIO_SUBSYS_IOPMP_CP_RST_N	N.A	rstgen_audio_subsys_iopmp_cp_rst_n
APSYS	SRAM_AXI	sw_apsys_rst_n	N.A	SW_SRAM_AXI_ARST_N_0	N.A	rstgen_sram_axi_arst_n_0
APSYS	SRAM_AXI	sw_apsys_rst_n	N.A	SW_SRAM_AXI_ARST_N_1	N.A	rstgen_sram_axi_arst_n_1
APSYS	SRAM_AXI	sw_apsys_rst_n	N.A	SW_SRAM_AXI_ARST_N_2	N.A	rstgen_sram_axi_arst_n_2
APSYS	SRAM_AXI	sw_apsys_rst_n	N.A	SW_SRAM_AXI_ARST_N_3	N.A	rstgen_sram_axi_arst_n_3
APSYS	SRAM_AXI	sw_apsys_rst_n	N.A	SW_SRAM_AXI_ARST_N_4	N.A	rstgen_sram_axi_arst_n_4
APSYS	SRAM_AXI	sw_apsys_rst_n	N.A	SW_SRAM_AXI_CORE_RST_N	N.A	rstgen_sram_axi_core_rst_n
CPUSYS	C910_BROM	sw_apsys_rst_n	N.A	SW_C910_BROM_HRST_N	N.A	rstgen_c910_brom_hrst_n
CPUSYS	C910 TOP	sw_apsys_rst_n	sw_c910_rst_n	I2C2_SCL	N.A	c910_cpu_rst_n
CPUSYS	C910 CORE0	sw_apsys_rst_n	sw_c910_rst_n	I2C2_SCL	SW_C910_CORE0_RST_N	c910_core0_rst_n
CPUSYS	C910 CORE1	sw_apsys_rst_n	sw_c910_rst_n	I2C2_SCL	SW_C910_CORE1_RST_N	c910_core1_rst_n
CPUSYS	C910 CORE2	sw_apsys_rst_n	sw_c910_rst_n	I2C2_SCL	SW_C910_CORE2_RST_N	c910_core2_rst_n
CPUSYS	C910 CORE3	sw_apsys_rst_n	sw_c910_rst_n	I2C2_SCL	SW_C910_CORE3_RST_N	c910_core3_rst_n
CPUSYS	CHIP_DBG	sw_apsys_rst_n	N.A	SW_CHIP_DBG_ARST_N	N.A	rstgen_chip_dbg_arst_n

SUBSYS	Module	SUBSYS Soft Reset 1	SUBSYS Soft Reset 2	Module Soft Reset 1	Module Soft Reset 2	Reset Name
CPUSYS	CHIP_DBG	sw_apsys_rst_n	N.A	SW_CHIP_DBG_CRST_N	N.A	rstgen_chip_dbg_crst_n
CPUSYS	AXI4_CPUSYS1	sw_apsys_rst_n	N.A	SW_AXI4_CPUSYS1_ARST_N	N.A	rstgen_axi4_cpusys1_arst_n
CPUSYS	AXI4_CPUSYS1	sw_apsys_rst_n	N.A	SW_AXI4_CPUSYS1_PRST_N	N.A	rstgen_axi4_cpusys1_prst_n
CPUSYS	AXI4_CPUSYS2	sw_apsys_rst_n	N.A	SW_AXI4_CPUSYS2_ARST_N	N.A	rstgen_axi4_cpusys2_arst_n
CPUSYS	AXI4_CPUSYS2	sw_apsys_rst_n	N.A	SW_AXI4_CPUSYS2_PRST_N	N.A	rstgen_axi4_cpusys2_prst_n
CPUSYS	X2X_CPUSYS	sw_apsys_rst_n	N.A	SW_X2X_CPUSYS_RST_N	N.A	rstgen_x2x_cpusys_arst_n
CPUSYS	X2H_CPUSYS	sw_apsys_rst_n	N.A	SW_X2H_CPUSYS_RST_N	N.A	rstgen_x2h_cpusys_arst_n
CPUSYS	X2H_CPUSYS	sw_apsys_rst_n	N.A	SW_X2H_CPUSYS_RST_N	N.A	rstgen_x2h_cpusys_mhrst_n
CPUSYS	AHB2_CPUSYS	sw_apsys_rst_n	N.A	SW_AHB2_CPUSYS_HRST_N	N.A	rstgen_ahb2_cpusys_hrst_n
CPUSYS	APB3_CPUSYS	sw_apsys_rst_n	N.A	SW_APB3_CPUSYS_HRST_N	N.A	rstgen_apb3_cpusys_hrst_n
CPUSYS	MBOX0	sw_apsys_rst_n	N.A	SW_MBOX0_PRST_N	N.A	rstgen_mbox0_prst_n
CPUSYS	MBOX1	sw_apsys_rst_n	N.A	SW_MBOX1_PRST_N	N.A	rstgen_mbox1_prst_n
CPUSYS	MBOX2	sw_apsys_rst_n	N.A	SW_MBOX2_PRST_N	N.A	rstgen_mbox2_prst_n
CPUSYS	MBOX3	sw_apsys_rst_n	N.A	SW_MBOX3_PRST_N	N.A	rstgen_mbox3_prst_n
CPUSYS	WDT0	sw_apsys_rst_n	N.A	SW_WDT0_PRST_N	N.A	rstgen_wdt0_prst_n
CPUSYS	WDT1	sw_apsys_rst_n	N.A	SW_WDT1_PRST_N	N.A	rstgen_wdt1_prst_n
CPUSYS	TIMER0	sw_apsys_rst_n	N.A	SW_TIMER0_PRST_N	N.A	rstgen_timer0_prst_n
CPUSYS	TIMER0	sw_apsys_rst_n	N.A	SW_TIMER0_CRST_N	N.A	rstgen_timer0_crst_n
CPUSYS	TIMER1	sw_apsys_rst_n	N.A	SW_TIMER1_PRST_N	N.A	rstgen_timer1_prst_n
CPUSYS	TIMER1	sw_apsys_rst_n	N.A	SW_TIMER1_CRST_N	N.A	rstgen_timer1_crst_n
CPUSYS	BMU_C910	sw_apsys_rst_n	N.A	SW_BMU_C910_ARST_N	N.A	rstgen_bmu_c910_arst_n
CPUSYS	BMU_C910	sw_apsys_rst_n	N.A	SW_BMU_C910_PRST_N	N.A	rstgen_bmu_c910_prst_n
CPUSYS	DMAC_CPUSYS	sw_apsys_rst_n	N.A	SW_DMAC_CPUSYS_ARST_N	N.A	rstgen_dmac_cpusys_arst_n
CPUSYS	DMAC_CPUSYS	sw_apsys_rst_n	N.A	SW_DMAC_CPUSYS_HRST_N	N.A	rstgen_dmac_cpusys_hrst_n
CPUSYS	SPINLOCK	sw_apsys_rst_n	N.A	SW_SPINLOCK_HRST_N	N.A	rstgen_spinlock_hrst_n
CPUSYS	iopmp_aon	sw_apsys_rst_n	N.A	SW_IOPMP_AON_ARST_N	N.A	rstgen_iopmp_aon_arst_n
CPUSYS	iopmp_aon	sw_apsys_rst_n	N.A	SW_IOPMP_AON_PRST_N	N.A	rstgen_iopmp_aon_prst_n
CPUSYS	iopmp_aud	sw_apsys_rst_n	N.A	SW_IOPMP_AUD_ARST_N	N.A	rstgen_iopmp_aud_arst_n
CPUSYS	iopmp_aud	sw_apsys_rst_n	N.A	SW_IOPMP_AUD_PRST_N	N.A	rstgen_iopmp_aud_prst_n

SUBSYS	Module	SUBSYS Soft Reset 1	SUBSYS Soft Reset 2	Module Soft Reset 1	Module Soft Reset 2	Reset Name
CPUSYS	iopmp_chip_dbg	sw_apsys_rst_n	N.A	SW_IOPMP_CHIP_DBG_ARST_N	N.A	rstgen_iopmp_chip_dbg_arst_n
CPUSYS	iopmp_chip_dbg	sw_apsys_rst_n	N.A	SW_IOPMP_CHIP_DBG_PRST_N	N.A	rstgen_iopmp_chip_dbg_prst_n
CPUSYS	iopmp_dmac_cpusys	sw_apsys_rst_n	N.A	SW_IOPMP_DMAC_CPUSYS_ARST_N	N.A	rstgen_iopmp_dmac_cpusys_arst_n
CPUSYS	iopmp_dmac_cpusys	sw_apsys_rst_n	N.A	SW_IOPMP_DMAC_CPUSYS_PRST_N	N.A	rstgen_iopmp_dmac_cpusys_prst_n
CPUSYS	c910_top_ds	sw_apsys_rst_n	N.A	SW_C910_TOP_DS_PRST_N	N.A	rstgen_c910_top_ds_prst_n
CPUSYS	c910_top_ds	sw_apsys_rst_n	N.A	SW_C910_TOP_CORE0_DS_RST_N	N.A	c910_top_core0_ds_rst_n
CPUSYS	c910_top_ds	sw_apsys_rst_n	N.A	SW_C910_TOP_CORE1_DS_RST_N	N.A	c910_top_core1_ds_rst_n
CPUSYS	c910_top_ds	sw_apsys_rst_n	N.A	SW_C910_TOP_CORE2_DS_RST_N	N.A	c910_top_core2_ds_rst_n
CPUSYS	c910_top_ds	sw_apsys_rst_n	N.A	SW_C910_TOP_CORE3_DS_RST_N	N.A	c910_top_core3_ds_rst_n
PERISYS	PERISYS_AHB	sw_apsys_rst_n	N.A	SW_PERISYS_AHB_HRST_N	N.A	rstgen_perisys_ahb_hrst_n
PERISYS	PERISYS_APB1	sw_apsys_rst_n	N.A	SW_PERISYS_APB1_HRST_N	N.A	rstgen_perisys_apb1_hrst_n
PERISYS	PERISYS_APB2	sw_apsys_rst_n	N.A	SW_PERISYS_APB2_HRST_N	N.A	rstgen_perisys_apb2_hrst_n
PERISYS	PERISYS_APB4	sw_apsys_rst_n	N.A	SW_PERISYS_APB4_HRST_N	N.A	rstgen_perisys_apb4_hrst_n
PERISYS	GMAC0	sw_apsys_rst_n	N.A	SW_GMAC0_ARST_N	N.A	rstgen_gmac0_arst_n
PERISYS	GMAC0	sw_apsys_rst_n	N.A	SW_GMAC0_GRST_N	N.A	rstgen_gmac0_grst_n
PERISYS	GMAC0	sw_apsys_rst_n	N.A	SW_GMAC0_HRST_N	N.A	rstgen_gmac0_hrst_n
PERISYS	GMAC0	sw_apsys_rst_n	N.A	SW_GMAC0_PRST_N	N.A	rstgen_gmac0_prst_n
PERISYS	GMAC1	sw_apsys_rst_n	N.A	SW_GMAC1_ARST_N	N.A	rstgen_gmac1_arst_n
PERISYS	GMAC1	sw_apsys_rst_n	N.A	SW_GMAC1_GRST_N	N.A	rstgen_gmac1_grst_n
PERISYS	GMAC1	sw_apsys_rst_n	N.A	SW_GMAC1_HRST_N	N.A	rstgen_gmac1_hrst_n
PERISYS	GMAC1	sw_apsys_rst_n	N.A	SW_GMAC1_PRST_N	N.A	rstgen_gmac1_prst_n
PERISYS	GMAC_AXI	sw_apsys_rst_n	N.A	SW_GMAC_AXI_PRST_N	N.A	rstgen_gmac_axi_prst_n
PERISYS	GMAC_AXI	sw_apsys_rst_n	N.A	SW_GMAC_AXI_ARST_N	N.A	rstgen_gmac_axi_arst_n
PERISYS	UART0	sw_apsys_rst_n	N.A	SW_UART0_PRST_N	N.A	rstgen_uart0_prst_n
PERISYS	UART0	sw_apsys_rst_n	N.A	SW_UART0_S_RST_N	N.A	rstgen_uart0_s_rst_n
PERISYS	UART1	sw_apsys_rst_n	N.A	SW_UART1_PRST_N	N.A	rstgen_uart1_prst_n
PERISYS	UART1	sw_apsys_rst_n	N.A	SW_UART1_S_RST_N	N.A	rstgen_uart1_s_rst_n

SUBSYS	Module	SUBSYS Soft Reset 1	SUBSYS Soft Reset 2	Module Soft Reset 1	Module Soft Reset 2	Reset Name
PERISYS	UART2	sw_apsys_rst_n	N.A	SW_UART2_PRST_N	N.A	rstgen_uart2_prst_n
PERISYS	UART2	sw_apsys_rst_n	N.A	SW_UART2_S_RST_N	N.A	rstgen_uart2_s_rst_n
PERISYS	UART3	sw_apsys_rst_n	N.A	SW_UART3_PRST_N	N.A	rstgen_uart3_prst_n
PERISYS	UART3	sw_apsys_rst_n	N.A	SW_UART3_S_RST_N	N.A	rstgen_uart3_s_rst_n
PERISYS	UART4	sw_apsys_rst_n	N.A	SW_UART4_PRST_N	N.A	rstgen_uart4_prst_n
PERISYS	UART4	sw_apsys_rst_n	N.A	SW_UART4_S_RST_N	N.A	rstgen_uart4_s_rst_n
PERISYS	UART5	sw_apsys_rst_n	N.A	SW_UART5_PRST_N	N.A	rstgen_uart5_prst_n
PERISYS	UART5	sw_apsys_rst_n	N.A	SW_UART5_S_RST_N	N.A	rstgen_uart5_s_rst_n
PERISYS	QSPI0	sw_apsys_rst_n	N.A	SW_QSPI0_PRST_N	N.A	rstgen_qspi0_prst_n
PERISYS	QSPI0	sw_apsys_rst_n	N.A	SW_QSPI0_SSI_RST_N	N.A	rstgen_qspi0_ssi_rst_n
PERISYS	QSPI1	sw_apsys_rst_n	N.A	SW_QSPI1_PRST_N	N.A	rstgen_qspi1_prst_n
PERISYS	QSPI1	sw_apsys_rst_n	N.A	SW_QSPI1_SSI_RST_N	N.A	rstgen_qspi1_ssi_rst_n
PERISYS	SPI	sw_apsys_rst_n	N.A	SW_SPI_PRST_N	N.A	rstgen_spi_prst_n
PERISYS	SPI	sw_apsys_rst_n	N.A	SW_SPI_SSI_RST_N	N.A	rstgen_spi_ssi_rst_n
PERISYS	I2C0	sw_apsys_rst_n	N.A	SW_I2C0_IC_RST_N	N.A	rstgen_i2c0_ic_rst_n
PERISYS	I2C0	sw_apsys_rst_n	N.A	SW_I2C0_PRST_N	N.A	rstgen_i2c0_prst_n
PERISYS	I2C1	sw_apsys_rst_n	N.A	SW_I2C1_IC_RST_N	N.A	rstgen_i2c1_ic_rst_n
PERISYS	I2C1	sw_apsys_rst_n	N.A	SW_I2C1_PRST_N	N.A	rstgen_i2c1_prst_n
PERISYS	I2C2	sw_apsys_rst_n	N.A	SW_I2C2_IC_RST_N	N.A	rstgen_i2c2_ic_rst_n
PERISYS	I2C2	sw_apsys_rst_n	N.A	SW_I2C2_PRST_N	N.A	rstgen_i2c2_prst_n
PERISYS	I2C3	sw_apsys_rst_n	N.A	SW_I2C3_IC_RST_N	N.A	rstgen_i2c3_ic_rst_n
PERISYS	I2C3	sw_apsys_rst_n	N.A	SW_I2C3_PRST_N	N.A	rstgen_i2c3_prst_n
PERISYS	I2C4	sw_apsys_rst_n	N.A	SW_I2C4_IC_RST_N	N.A	rstgen_i2c4_ic_rst_n
PERISYS	I2C4	sw_apsys_rst_n	N.A	SW_I2C4_PRST_N	N.A	rstgen_i2c4_prst_n
PERISYS	I2C5	sw_apsys_rst_n	N.A	SW_I2C5_IC_RST_N	N.A	rstgen_i2c5_ic_rst_n
PERISYS	I2C5	sw_apsys_rst_n	N.A	SW_I2C5_PRST_N	N.A	rstgen_i2c5_prst_n
PERISYS	GPIO0	sw_apsys_rst_n	N.A	SW_GPIO0_PRST_N	N.A	rstgen_gpio0_prst_n
PERISYS	GPIO0	sw_apsys_rst_n	N.A	SW_GPIO0_DBRST_N	N.A	rstgen_gpio0_dbrst_n
PERISYS	GPIO1	sw_apsys_rst_n	N.A	SW_GPIO1_PRST_N	N.A	rstgen_gpio1_prst_n
PERISYS	GPIO1	sw_apsys_rst_n	N.A	SW_GPIO1_DBRST_N	N.A	rstgen_gpio1_dbrst_n
PERISYS	GPIO2	sw_apsys_rst_n	N.A	SW_GPIO2_PRST_N	N.A	rstgen_gpio2_prst_n
PERISYS	GPIO2	sw_apsys_rst_n	N.A	SW_GPIO2_DBRST_N	N.A	rstgen_gpio2_dbrst_n
PERISYS	GPIO3	sw_apsys_rst_n	N.A	SW_GPIO3_DBRST_N	N.A	rstgen_gpio3_dbrst_n
PERISYS	PWM	sw_apsys_rst_n	N.A	SW_PWM_PRST_N	N.A	rstgen_pwm_prst_n

SUBSYS	Module	SUBSYS Soft Reset 1	SUBSYS Soft Reset 2	Module Soft Reset 1	Module Soft Reset 2	Reset Name
PERISYS	PWM	sw_apsys_rst_n	N.A	SW_PWM_CRST_N	N.A	rstgen_pwm_crst_n
PERISYS	I2S	sw_apsys_rst_n	N.A	SW_I2S_PRST_N	N.A	rstgen_i2s_prst_n
PERISYS	IOPMP_GMAC0	sw_apsys_rst_n	N.A	SW_IOPMP_GMAC0_ARST_N	N.A	rstgen_iopmp_gmac0_arst_n
PERISYS	IOPMP_GMAC0	sw_apsys_rst_n	N.A	SW_IOPMP_GMAC0_PRST_N	N.A	rstgen_iopmp_gmac0_prst_n
PERISYS	IOPMP_GMAC1	sw_apsys_rst_n	N.A	SW_IOPMP_GMAC1_ARST_N	N.A	rstgen_iopmp_gmac1_arst_n
PERISYS	IOPMP_GMAC1	sw_apsys_rst_n	N.A	SW_IOPMP_GMAC1_PRST_N	N.A	rstgen_iopmp_gmac1_prst_n
PERI2SYS	DSMART	sw_apsys_rst_n	N.A	SW_DSMART_PRST_N	N.A	rstgen_dsmart_presetn
PERI2SYS	PERI_APB3	sw_apsys_rst_n	N.A	SW_PERI_APB3_HRST_N	N.A	rstgen_peri2peri1_apb_hrst_n
PERI2SYS	GPIO3	sw_apsys_rst_n	N.A	SW_GPIO3_PRST_N	N.A	rstgen_gpio3_prst_n
PERI2SYS	P2P	sw_apsys_rst_n	N.A	SW_PERI2PERI1_APB_PRST_N	N.A	rstgen_peri2peri1_apb_prst_n
APSYS	PADCTRL0_APSYS	sw_apsys_rst_n	N.A	SW_PADCTRL0_APSYS_PRST_N	N.A	rstgen_padctrl0_apsys_prst_n
APSYS	PADCTRL1_APSYS	sw_apsys_rst_n	N.A	SW_PADCTRL1_APSYS_PRST_N	N.A	rstgen_padctrl1_apsys_prst_n
APSYS	CPU2PERI_X2H	sw_apsys_rst_n	N.A	SW_CPU2PERI_X2H_RST_N	N.A	rstgen_cpu2peri_x2h_arst_n
APSYS	CPU2PERI_X2H	sw_apsys_rst_n	N.A	SW_CPU2PERI_X2H_RST_N	N.A	rstgen_cpu2peri_x2h_mhrst_n
APSYS	AXI4_CFG_BUS	sw_apsys_rst_n	N.A	SW_AXI4_CFG_BUS_ARST_N	N.A	rstgen_axi4_cfg_bus_arst_n
APSYS	CPU2CFG_X2H	sw_apsys_rst_n	N.A	SW_CPU2CFG_X2H_RST_N	N.A	rstgen_cpu2cfg_x2h_arst_n
APSYS	CPU2CFG_X2H	sw_apsys_rst_n	N.A	SW_CPU2CFG_X2H_RST_N	N.A	rstgen_cpu2cfg_x2h_mhrst_n
APSYS	CPU2CFG_APB	sw_apsys_rst_n	N.A	SW_CPU2CFG_APB_RST_N	N.A	rstgen_apb_cpu2cfg_hrst_n
APSYS	CPU2CFG_X2X	sw_apsys_rst_n	N.A	SW_CPU2CFG_X2X_ARST_N	N.A	rstgen_cpu2cfg_x2x_arst_n
APSYS	CPU2AON_X2H	sw_apsys_rst_n	N.A	SW_CPU2AON_X2H_RST_N	N.A	rstgen_cpu2aon_x2h_arst_n
APSYS	CPU2AON_X2H	sw_apsys_rst_n	N.A	SW_CPU2AON_X2H_RST_N	N.A	rstgen_cpu2aon_x2h_mhrst_n
APSYS	AON2CPU_A2X	sw_apsys_rst_n	N.A	SW_AON2CPU_A2X_HRST_N	N.A	rstgen_aon2cpu_a2x_hrst_n
APSYS	AON2CPU_A2X	sw_apsys_rst_n	N.A	SW_AON2CPU_A2X_HRST_N	N.A	rstgen_aon2cpu_a2x_arst_n
APSYS	APSYS_SYSREG	sw_apsys_rst_n	N.A	N.A	N.A	rstgen_apsys_sysreg_prst_n

SUBSYS	Module	SUBSYS Soft Reset 1	SUBSYS Soft Reset 2	Module Soft Reset 1	Module Soft Reset 2	Reset Name
APSYS	APSYS_RSTGEN	sw_apsys_rst_n	N.A	N.A	N.A	rstgen_apsys_rstgen_prst_n
APSYS	APSYS_CLKGEN	sw_apsys_rst_n	N.A	N.A	N.A	rstgen_apsys_clkgen_prst_n
APSYS	NPUSYS_AXI	sw_apsys_rst_n	N.A	SW_NPUSYS_AXI_ARST_N	N.A	rstgen_npusys_axi_arst_n
APSYS	CPU2VP_X2P	sw_apsys_rst_n	N.A	SW_CPU2VP_X2P_RST_N	N.A	rstgen_cpu2vp_x2p_arst_n
APSYS	CPU2VP_X2P	sw_apsys_rst_n	N.A	SW_CPU2VP_X2P_RST_N	N.A	rstgen_cpu2vp_x2p_prst_n
APSYS	CPU2VI_X2H	sw_apsys_rst_n	N.A	SW_CPU2VI_X2H_RST_N	N.A	rstgen_cpu2vi_x2h_arst_n
APSYS	CPU2VI_X2H	sw_apsys_rst_n	N.A	SW_CPU2VI_X2H_RST_N	N.A	rstgen_cpu2vi_x2h_mhrst_n
APSYS	NPUSYS_AXI	sw_apsys_rst_n	N.A	SW_NPUSYS_AXI_PRST_N	N.A	rstgen_npusys_axi_prst_n
APSYS	VOSYS_AXI	sw_apsys_rst_n	N.A	SW_VOSYS_AXI_PRST_N	N.A	rstgen_vosys_axi_prst_n
APSYS	vp_subsys	sw_apsys_rst_n	N.A	SW_VP_SUBSYS_PRST_N	N.A	rstgen_vp_subsys_prst_n
APSYS	VO_AXI	sw_apsys_rst_n	N.A	SW_VOSYS_AXI_ARST_N	N.A	rstgen_vosys_axi_arst_n
APSYS	vobus2npubus	sw_apsys_rst_n	N.A	SW_VOBUS2NPUBUS_X2X_ARST_N	N.A	rstgen_vobus2npubus_x2x_arst_n
APSYS	misc2vp_x2x	sw_apsys_rst_n	N.A	SW_MISC2VP_X2X_ARST_N	N.A	rstgen_misc2vp_x2x_arst_n
TEESYS	CFG2TEE_X2H	sw_apsys_rst_n	N.A	SW_CFG2TEE_X2H_RST_N	N.A	rstgen_cfg2tee_x2h_arst_n
TEESYS	CFG2TEE_X2H	sw_apsys_rst_n	N.A	SW_CFG2TEE_X2H_RST_N	N.A	rstgen_cfg2tee_x2h_mhrst_n
NPUSYS	IMG_NNA	sw_apsys_rst_n	sw_npusys_rst_n	SW_IMG_NNA_RST_N	N.A	rstgen_img_nna_resetn
NPUSYS	IOPMP_NPU	sw_apsys_rst_n	sw_npusys_rst_n	SW_IOPMP_NPU_PRST_N	N.A	rstgen_iopmp_npu_prst_n
NPUSYS	NPU_SUBSYS_CLKGEN	sw_apsys_rst_n	sw_npusys_rst_n	N.A	N.A	rstgen_npu_subsys_clkgen_rst_n
DSPSYS	DSP	sw_apsys_rst_n	dsp_subsys_rst_n	SW_DSP0_CRST_N	N.A	rstgen_dsp0_crst_n
DSPSYS	DSP	sw_apsys_rst_n	dsp_subsys_rst_n	SW_DSP0_DRST_N	N.A	rstgen_dsp0_drst_n
DSPSYS	DSP	sw_apsys_rst_n	dsp_subsys_rst_n	SW_DSP0_PRST_N	N.A	rstgen_dsp0_prst_n
DSPSYS	DSP	sw_apsys_rst_n	dsp_subsys_rst_n	SW_DSP1_CRST_N	N.A	rstgen_dsp1_crst_n
DSPSYS	DSP	sw_apsys_rst_n	dsp_subsys_rst_n	SW_DSP1_DRST_N	N.A	rstgen_dsp1_drst_n
DSPSYS	DSP	sw_apsys_rst_n	dsp_subsys_rst_n	SW_DSP1_PRST_N	N.A	rstgen_dsp1_prst_n
DSPSYS	DSPSYS	sw_apsys_rst_n	dsp_subsys_rst_n	SW_AXI4_DSPSYS_ARST_N	N.A	rstgen_axi4_dspsys_arst_n

SUBSYS	Module	SUBSYS Soft Reset 1	SUBSYS Soft Reset 2	Module Soft Reset 1	Module Soft Reset 2	Reset Name
DSPSYS	DSPSYS_SLV	sw_apsys_rst_n	dsp_subsys_rst_n	SW_AXI4_DSPSYS_SLV_ARST_N	N.A	rstgen_axi4_dspsys_slv_arst_n
DSPSYS	DSPSYS	sw_apsys_rst_n	dsp_subsys_rst_n	SW_DSPSYS_PRESETN	N.A	rstgen_dspsys_presetn
DSPSYS	IOPMP_DSP2	sw_apsys_rst_n	dsp_subsys_rst_n	SW_IOPMP_DSP0_ARST_N	N.A	rstgen_iopmp_dsp0_arst_n
DSPSYS	IOPMP_DSP1	sw_apsys_rst_n	dsp_subsys_rst_n	SW_IOPMP_DSP1_ARST_N	N.A	rstgen_iopmp_dsp1_arst_n
DSPSYS	IOPMP_DSP2	sw_apsys_rst_n	dsp_subsys_rst_n	SW_IOPMP_DSP0_PRESETN	N.A	rstgen_iopmp_dsp0_presetn
DSPSYS	IOPMP_DSP1	sw_apsys_rst_n	dsp_subsys_rst_n	SW_IOPMP_DSP1_PRESETN	N.A	rstgen_iopmp_dsp1_presetn
DSPSYS	IOPMP_DSP1	sw_apsys_rst_n	dsp_subsys_rst_n	SW_AXI4_DSP_RS_ARST_N	N.A	rstgen_axi4_dsp_rs_arst_n
DSPSYS	DSP	sw_apsys_rst_n	dsp_subsys_rst_n	SW_X2X_DSP0_ARST_N	N.A	rstgen_x2x_dsp0_arst_n
DSPSYS	DSP	sw_apsys_rst_n	dsp_subsys_rst_n	SW_X2X_DSP1_ARST_N	N.A	rstgen_x2x_dsp1_arst_n
DSPSYS	DSP	sw_apsys_rst_n	dsp_subsys_rst_n	SW_X2X_X4_DSPSLV_DSP0_ARST_N	N.A	rstgen_x2x_x4_dspslv_dsp0_arst_n
DSPSYS	DSP	sw_apsys_rst_n	dsp_subsys_rst_n	SW_X2X_X4_DSPSLV_DSP1_ARST_N	N.A	rstgen_x2x_x4_dspslv_dsp1_arst_n
VPSYS	AXI4_VPSYS_DW_axi	sw_apsys_rst_n	vp_subsys_rst_n	SW_AXI4_VPSYS_PRST_N	N.A	rstgen_axi4_vpsys_presetn
VPSYS	AXI4_VPSYS_DW_axi	sw_apsys_rst_n	vp_subsys_rst_n	SW_AXI4_VPSYS_ARST_N	N.A	rstgen_axi4_vpsys_aresetn
VPSYS	fce_top	sw_apsys_rst_n	vp_subsys_rst_n	SW_FCE_PRST_N	N.A	rstgen_fce_prst_n
VPSYS	fce_top	sw_apsys_rst_n	vp_subsys_rst_n	SW_FCE_ARST_N	N.A	rstgen_fce_arst_n
VPSYS	vsi_gc620_top	sw_apsys_rst_n	vp_subsys_rst_n	SW_G2D_PRST_N	N.A	rstgen_g2d_prst_n
VPSYS	vsi_gc620_top	sw_apsys_rst_n	vp_subsys_rst_n	SW_G2D_ARST_N	N.A	rstgen_g2d_arst_n
VPSYS	vsi_gc620_top	sw_apsys_rst_n	vp_subsys_rst_n	SW_G2D_CRST_N	N.A	rstgen_g2d_crst_n
VPSYS	IOPMP_VPSYS	sw_apsys_rst_n	vp_subsys_rst_n	SW_IOPMP_VENC_ARST_N	N.A	rstgen_iopmp_venc_arst_n
VPSYS	IOPMP_VPSYS	sw_apsys_rst_n	vp_subsys_rst_n	SW_IOPMP_VDEC_ARST_N	N.A	rstgen_iopmp_vdec_arst_n
VPSYS	IOPMP_VPSYS	sw_apsys_rst_n	vp_subsys_rst_n	SW_IOPMP_G2D_ARST_N	N.A	rstgen_iopmp_g2d_arst_n
VPSYS	IOPMP_VPSYS	sw_apsys_rst_n	vp_subsys_rst_n	SW_IOPMP_FCE_ARST_N	N.A	rstgen_iopmp_fce_arst_n
VPSYS	IOPMP_VPSYS	sw_apsys_rst_n	vp_subsys_rst_n	SW_IOPMP_VENC_PRST_N	N.A	rstgen_iopmp_venc_prst_n
VPSYS	IOPMP_VPSYS	sw_apsys_rst_n	vp_subsys_rst_n	SW_IOPMP_VDEC_PRST_N	N.A	rstgen_iopmp_vdec_prst_n
VPSYS	IOPMP_VPSYS	sw_apsys_rst_n	vp_subsys_rst_n	SW_IOPMP_G2D_PRST_N	N.A	rstgen_iopmp_g2d_prst_n

SUBSYS	Module	SUBSYS Soft Reset 1	SUBSYS Soft Reset 2	Module Soft Reset 1	Module Soft Reset 2	Reset Name
VPSYS	IOPMP_VPSYS	sw_apsys_rst_n	vp_subsys_rst_n	SW_IOPMP_FCE_PRST_N	N.A	rstgen_iopmp_fce_prst_n
VPSYS	vc8000d_subsys_top	sw_apsys_rst_n	vp_subsys_rst_n	SW_VDEC_PRST_N	sw_vdec_rst_n	rstgen_vdec_prst_n
VPSYS	vc8000d_subsys_top	sw_apsys_rst_n	vp_subsys_rst_n	SW_VDEC_ARST_N	sw_vdec_rst_n	rstgen_vdec_arst_n
VPSYS	vc8000d_subsys_top	sw_apsys_rst_n	vp_subsys_rst_n	SW_VDEC_CRST_N	sw_vdec_rst_n	rstgen_vdec_crst_n
VPSYS	vc8000d_subsys_top	sw_apsys_rst_n	vp_subsys_rst_n	N.A	sw_vdec_rst_n	vc8000d_clkgen_top_rstn
VPSYS	VC_vc8000e_top	sw_apsys_rst_n	vp_subsys_rst_n	SW_VENC_PRST_N	sw_venc_rst_n	rstgen_venc_prst_n
VPSYS	VC_vc8000e_top	sw_apsys_rst_n	vp_subsys_rst_n	SW_VENC_ARST_N	sw_venc_rst_n	rstgen_venc_arst_n
VPSYS	X2X_X4_FCE_DW_axi_x2x	sw_apsys_rst_n	vp_subsys_rst_n	SW_X2XM_ARST_N	N.A	rstgen_x2xm_arst_n
VPSYS	X2X_X4_FCE_DW_axi_x2x	sw_apsys_rst_n	vp_subsys_rst_n	SW_X2XS_ARST_N	N.A	rstgen_x2xs_arst_n
VPSYS	vpsys_reg,APB_DECODER	sw_apsys_rst_n	vp_subsys_rst_n	N.A	N.A	rstgen_vpsys_prst_n
VISYS	ISP	sw_apsys_rst_n	vi_subsys_rst_n	SW_ISP_SRST_N	N.A	rstgen_isp_srst_n
VISYS	ISP	sw_apsys_rst_n	vi_subsys_rst_n	SW_ISP_RY_SRST_N	N.A	rstgen_isp_ry_srst_n
VISYS	DW200	sw_apsys_rst_n	vi_subsys_rst_n	SW_DW200_SRST_N	N.A	rstgen_dw200_srst_n
VISYS	MIPI_CSI	sw_apsys_rst_n	vi_subsys_rst_n	SW_MIPI_CSI2_PRESETN	N.A	rstgen_mipi_csi2_presetn
VISYS	MIPI_CSI	sw_apsys_rst_n	vi_subsys_rst_n	SW_MIPI_MIPI_CSI2X2_PRESETN_0	N.A	rstgen_mipi_csi2x2_presetn_0
VISYS	MIPI_CSI	sw_apsys_rst_n	vi_subsys_rst_n	SW_MIPI_MIPI_CSI2X2_PRESETN_1	N.A	rstgen_mipi_csi2x2_presetn_1
VISYS	VIPRE	sw_apsys_rst_n	vi_subsys_rst_n	SW_VIPRE_PRESETN	N.A	rstgen_vipre_presetn
VISYS	VIPRE	sw_apsys_rst_n	vi_subsys_rst_n	SW_VIPRE_ARSTN	N.A	rstgen_vipre_arstn
VISYS	VISYS	sw_apsys_rst_n	vi_subsys_rst_n	SW_AXI4_VISYS_ARST_N	N.A	rstgen_axi4_visys_arst_n
VISYS	VISYS1	sw_apsys_rst_n	vi_subsys_rst_n	SW_AXI4_VISYS1_ARST_N	N.A	rstgen_axi4_visys1_arst_n
VISYS	VISYS2	sw_apsys_rst_n	vi_subsys_rst_n	SW_AXI4_VISYS2_ARST_N	N.A	rstgen_axi4_visys2_arst_n
VISYS	VISYS3	sw_apsys_rst_n	vi_subsys_rst_n	SW_AXI4_VISYS3_ARST_N	N.A	rstgen_axi4_visys3_arst_n
VISYS	VISYS	sw_apsys_rst_n	vi_subsys_rst_n	SW_VISYS_PRESETN	N.A	rstgen_visys_presetn
VISYS	VISYS	sw_apsys_rst_n	vi_subsys_rst_n	SW_MIPI_CSI2X2_FIFO_RSTZ	N.A	rstgen_mipi_csi2x2_fifo_rstz
VISYS	ISP_VENC_SHAKE	sw_apsys_rst_n	vi_subsys_rst_n	SW_ISP_VENC_SHAKE_PRESETN	N.A	rstgen_isp_venc_shake_presetn
VISYS	ISP_VENC_SHAKE	sw_apsys_rst_n	vi_subsys_rst_n	SW_ISP_VENC_SHAKE_ARSTN	N.A	rstgen_isp_venc_shake_aresetn
VISYS	IOPMP_VSI1	sw_apsys_rst_n	vi_subsys_rst_n	SW_AXI4_IOPMP_VSI1_ARST_N	N.A	rstgen_axi4_iopmp_vsi1_arst_n

SUBSYS	Module	SUBSYS Soft Reset 1	SUBSYS Soft Reset 2	Module Soft Reset 1	Module Soft Reset 2	Reset Name
VISYS	IOPMP_VSI2	sw_apsys_rst_n	vi_subsys_rst_n	SW_AXI4_IOPMP_VSI2_ARST_N	N.A	rstgen_axi4_iopmp_vsi2_arst_n
VISYS	IOPMP_VSI3	sw_apsys_rst_n	vi_subsys_rst_n	SW_AXI4_IOPMP_VSI3_ARST_N	N.A	rstgen_axi4_iopmp_vsi3_arst_n
VISYS	IOPMP_VIPRE	sw_apsys_rst_n	vi_subsys_rst_n	SW_AXI4_IOPMP_VIPRE_ARST_N	N.A	rstgen_axi4_iopmp_vipre_arst_n
VISYS	IOPMP_VSI1	sw_apsys_rst_n	vi_subsys_rst_n	SW_IOPMP_VSI1_PRESETN	N.A	rstgen_iopmp_vsi1_presetn
VISYS	IOPMP_VSI2	sw_apsys_rst_n	vi_subsys_rst_n	SW_IOPMP_VSI2_PRESETN	N.A	rstgen_iopmp_vsi2_presetn
VISYS	IOPMP_VSI3	sw_apsys_rst_n	vi_subsys_rst_n	SW_IOPMP_VSI3_PRESETN	N.A	rstgen_iopmp_vsi3_presetn
VISYS	IOPMP_VIPRE	sw_apsys_rst_n	vi_subsys_rst_n	SW_IOPMP_VIPRE_PRESETN	N.A	rstgen_iopmp_vipre_presetn
MISCSYS	AXI4_MISCSYS	sw_apsys_rst_n	N.A	SW_MISCSYS_AXI_ARST_N	N.A	rstgen_miscsys_axi_arst_n
MISCSYS	AXI4_MISCSYS	sw_apsys_rst_n	N.A	SW_MISCSYS_AXI_PRST_N	N.A	rstgen_miscsys_axi_prst_n
MISCSYS	EMMC	sw_apsys_rst_n	N.A	SW_EMMC_SDIO_CLKGEN_RST_N	N.A	rstgen_emmc_sdio_clkgen_rst_n
MISCSYS	EMMC	sw_apsys_rst_n	N.A	SW_EMMC_RST_N	N.A	rstgen_emmc_rst_n
MISCSYS	SDIO0	sw_apsys_rst_n	N.A	SW_SDIO0_RST_N	N.A	rstgen_sdio0_rst_n
MISCSYS	SDIO1	sw_apsys_rst_n	N.A	SW_SDIO1_RST_N	N.A	rstgen_sdio1_rst_n
MISCSYS	USB3_DRD	sw_apsys_rst_n	N.A	SW_USB3_DRD_VCCRST_N	N.A	rstgen_usb3_drd_vccrst_n
MISCSYS	USB3_DRD	sw_apsys_rst_n	N.A	SW_USB3_DRD_PHYRST_N	N.A	rstgen_usb3_drd_phyrst_n
MISCSYS	USB3_DRD	sw_apsys_rst_n	N.A	SW_USB3_DRD_PRST_N	N.A	rstgen_usb3_drd_prst_n
MISCSYS	AHB2_TEESYS	sw_apsys_rst_n	N.A	SW_AHB2_TEESYS_HRST_N	N.A	rstgen_ahb2_teesys_hrst_n
MISCSYS	APB3_TEESYS	sw_apsys_rst_n	N.A	SW_APB3_TEESYS_HRST_N	N.A	rstgen_apb3_teesys_hrst_n
MISCSYS	AXI4_TEESYS	sw_apsys_rst_n	N.A	SW_AXI4_TEESYS_ARST_N	N.A	rstgen_axi4_teesys_arst_n
MISCSYS	X2X_TEESYS	sw_apsys_rst_n	N.A	SW_X2X_X4_TEESYS_128DW64_ARST_N	N.A	rstgen_x2x_x4_teesys_128dw64_arst_n
MISCSYS	TEE_SYSREG	sw_apsys_rst_n	N.A	SW_TEE_SYSREG_PRST_N	N.A	rstgen_tee_sysreg_prst_n
MISCSYS	TEE_DMAC	sw_apsys_rst_n	N.A	SW_TEE_DMAC_ARST_N	N.A	rstgen_tee_dmac_arst_n
MISCSYS	TEE_DMAC	sw_apsys_rst_n	N.A	SW_TEE_DMAC_HRST_N	N.A	rstgen_tee_dmac_hrst_n
MISCSYS	EFUSE	sw_apsys_rst_n	N.A	SW_EFUSE_PRST_N	N.A	rstgen_efuse_prst_n
MISCSYS	EIP120SI	sw_apsys_rst_n	N.A	SW_EIP120SI_ARST_N	N.A	rstgen_eip120si_arst_n
MISCSYS	EIP120SI	sw_apsys_rst_n	N.A	SW_EIP120SI_HRST_N	N.A	rstgen_eip120si_hrst_n
MISCSYS	EIP120SII	sw_apsys_rst_n	N.A	SW_EIP120SII_ARST_N	N.A	rstgen_eip120sii_arst_n

SUBSYS	Module	SUBSYS Soft Reset 1	SUBSYS Soft Reset 2	Module Soft Reset 1	Module Soft Reset 2	Reset Name
MISCSYS	EIP120SII	sw_apsys_rst_n	N.A	SW_EIP120SII_HRST_N	N.A	rstgen_eip120sii_hrst_n
MISCSYS	EIP120SIII	sw_apsys_rst_n	N.A	SW_EIP120SIII_ARST_N	N.A	rstgen_eip120siii_arst_n
MISCSYS	EIP120SIII	sw_apsys_rst_n	N.A	SW_EIP120SIII_HRST_N	N.A	rstgen_eip120siii_hrst_n
MISCSYS	EIP150B	sw_apsys_rst_n	N.A	SW_EIP150B_HRST_N	N.A	rstgen_eip150b_hrst_n
MISCSYS	SERAM	sw_apsys_rst_n	N.A	SW_OCRAM_HRST_N	N.A	rstgen_ocram_hrst_n
MISCSYS	IOPMP_EIP120	sw_apsys_rst_n	N.A	SW_IOPMP_EIP120SI_ARST_N	N.A	rstgen_iopmp_eip120si_arst_n
MISCSYS	IOPMP_EIP120	sw_apsys_rst_n	N.A	SW_IOPMP_EIP120SI_PRST_N	N.A	rstgen_iopmp_eip120si_prst_n
MISCSYS	IOPMP_EIP120	sw_apsys_rst_n	N.A	SW_IOPMP_EIP120SII_ARST_N	N.A	rstgen_iopmp_eip120sii_arst_n
MISCSYS	IOPMP_EIP120	sw_apsys_rst_n	N.A	SW_IOPMP_EIP120SII_PRST_N	N.A	rstgen_iopmp_eip120sii_prst_n
MISCSYS	IOPMP_EIP120	sw_apsys_rst_n	N.A	SW_IOPMP_EIP120SIII_ARST_N	N.A	rstgen_iopmp_eip120siii_arst_n
MISCSYS	IOPMP_EIP120	sw_apsys_rst_n	N.A	SW_IOPMP_EIP120SIII_PRST_N	N.A	rstgen_iopmp_eip120siii_prst_n
MISCSYS	IOPMP_EMMC	sw_apsys_rst_n	N.A	SW_IOPMP_EMMC_ARST_N	N.A	rstgen_iopmp_emmc_arst_n
MISCSYS	IOPMP_EMMC	sw_apsys_rst_n	N.A	SW_IOPMP_EMMC_PRST_N	N.A	rstgen_iopmp_emmc_prst_n
MISCSYS	IOPMP_SDIO0	sw_apsys_rst_n	N.A	SW_IOPMP_SDIO0_ARST_N	N.A	rstgen_iopmp_sdio0_arst_n
MISCSYS	IOPMP_SDIO0	sw_apsys_rst_n	N.A	SW_IOPMP_SDIO0_PRST_N	N.A	rstgen_iopmp_sdio0_prst_n
MISCSYS	IOPMP_SDIO1	sw_apsys_rst_n	N.A	SW_IOPMP_SDIO1_ARST_N	N.A	rstgen_iopmp_sdio1_arst_n
MISCSYS	IOPMP_SDIO1	sw_apsys_rst_n	N.A	SW_IOPMP_SDIO1_PRST_N	N.A	rstgen_iopmp_sdio1_prst_n
MISCSYS	IOPMP_DMAC	sw_apsys_rst_n	N.A	SW_IOPMP_TEEDMAC_ARST_N	N.A	rstgen_iopmp_teedmac_arst_n
MISCSYS	IOPMP_DMAC	sw_apsys_rst_n	N.A	SW_IOPMP_TEEDMAC_PRST_N	N.A	rstgen_iopmp_teedmac_prst_n
MISCSYS	IOPMP_USB3	sw_apsys_rst_n	N.A	SW_IOPMP_USB3_ARST_N	N.A	rstgen_iopmp_usb3_arst_n
MISCSYS	IOPMP_USB3	sw_apsys_rst_n	N.A	SW_IOPMP_USB3_PRST_N	N.A	rstgen_iopmp_usb3_prst_n
MISCSYS	DIGITAL_SENSOR	sw_apsys_rst_n	N.A	SW_DS_PRST_N	N.A	rstgen_ds_prst_n
MISCSYS	KEYRAM	sw_apsys_rst_n	N.A	SW_KEYRAM_PRST_N	N.A	rstgen_keyram_prst_n
VOSYS	rgx_hood_top	sw_apsys_rst_n	vo_subsys_rst_n	SW_GPU_RST_N	N.A	rstgen_gpu_resetn
VOSYS	DW_mipi_dsi_top	sw_apsys_rst_n	vo_subsys_rst_n	SW_MIPI_DSI0_PRST_N	N.A	rstgen_mipi_dsi0_prst_n

SUBSYS	Module	SUBSYS Soft Reset 1	SUBSYS Soft Reset 2	Module Soft Reset 1	Module Soft Reset 2	Reset Name
VOSYS	DW_mipi_dsi_top	sw_apsys_rst_n	vo_subsys_rst_n	SW_MIPI_DSI1_PRST_N	N.A	rstgen_mipi_dsi1_prst_n
VOSYS	iopmp_vosys_top	sw_apsys_rst_n	vo_subsys_rst_n	SW_IOPMP_VOSYS_GPU_PRST_N	N.A	rstgen_iopmp_vosys_gpu_prst_n
VOSYS	iopmp_vosys_top	sw_apsys_rst_n	vo_subsys_rst_n	SW_IOPMP_VOSYS_DPU_PRST_N	N.A	rstgen_iopmp_vosys_dpu_prst_n
VOSYS	iopmp_vosys_top	sw_apsys_rst_n	vo_subsys_rst_n	SW_IOPMP_VOSYS_DPU1_PRST_N	N.A	rstgen_iopmp_vosys_dpu1_prst_n
VOSYS	iopmp_vosys_top	sw_apsys_rst_n	vo_subsys_rst_n	SW_IOPMP_VOSYS_GPU_ARST_N	N.A	rstgen_iopmp_vosys_gpu_arst_n
VOSYS	iopmp_vosys_top	sw_apsys_rst_n	vo_subsys_rst_n	SW_IOPMP_VOSYS_DPU_ARST_N	N.A	rstgen_iopmp_vosys_dpu_arst_n
VOSYS	iopmp_vosys_top	sw_apsys_rst_n	vo_subsys_rst_n	SW_IOPMP_VOSYS_DPU1_ARST_N	N.A	rstgen_iopmp_vosys_dpu1_arst_n
VOSYS	hdmi_top	sw_apsys_rst_n	vo_subsys_rst_n	SW_HDMI_MAIN_RST_N	N.A	rstgen_hdmi_main_rst_n
VOSYS	hdmi_top	sw_apsys_rst_n	vo_subsys_rst_n	SW_HDMI_PRST_N	N.A	rstgen_hdmi_prst_n
VOSYS	dpu_top	sw_apsys_rst_n	vo_subsys_rst_n	SW_DPU_CRST_N	N.A	rstgen_dpu_crst_n
VOSYS	dpu_top	sw_apsys_rst_n	vo_subsys_rst_n	SW_DPU_ARST_N	N.A	rstgen_dpu_arst_n
VOSYS	dpu_top	sw_apsys_rst_n	vo_subsys_rst_n	SW_DPU_HRST_N	N.A	rstgen_dpu_hrst_n
VOSYS	axi4_vo_dw_axi	sw_apsys_rst_n	vo_subsys_rst_n	SW_AXI4_VO_ARST_N	N.A	rstgen_axi4_vo_arst_n
VOSYS	axi4_vo_dw_axi	sw_apsys_rst_n	vo_subsys_rst_n	SW_AXI4_VO_PRST_N	N.A	rstgen_axi4_vo_prst_n
VOSYS	axi4_vo_cfg_dw_axi	sw_apsys_rst_n	vo_subsys_rst_n	N.A	N.A	rstgen_axi4_vo_cfg_arst_n
VOSYS	x2h_x4_vosys_dw_axi_x2h	sw_apsys_rst_n	vo_subsys_rst_n	SW_X2H_DPU_ARST_N	N.A	rstgen_x2h_dpu_arst_n
VOSYS	x2h_x4_vosys_dw_axi_x2h	sw_apsys_rst_n	vo_subsys_rst_n	SW_X2H_DPU_HRST_N	N.A	rstgen_x2h_dpu_mhrst_n
VOSYS	x2h_x4_vosys_dw_axi_x2h	sw_apsys_rst_n	vo_subsys_rst_n	SW_X2H_DPU1_ARST_N	N.A	rstgen_x2h_dpu1_arst_n
VOSYS	x2h_x4_vosys_dw_axi_x2h	sw_apsys_rst_n	vo_subsys_rst_n	SW_X2H_DPU1_HRST_N	N.A	rstgen_x2h_dpu1_mhrst_n
VOSYS	x2p_x4_vosys_dw_axi_x2p	sw_apsys_rst_n	vo_subsys_rst_n	N.A	N.A	rstgen_x2p_x4_vosys_rst_n

5.4 Register Description

5.4.1 Register Memory Map

SUBSYS	REE BASE ADDRESS (C910)	TEE BASE ADDRESS (C910)	REE BASE ADDRESS (E902)	TEE BASE ADDRESS (E902)
AON_SUBSYS	NA	0xFF_FFF4_4000	NA	0xFFF4_4000
AP_SUBSYS	0xFF_EF01_4000	0xFF_FF01_5000	0xBF01_4000	0xFF01_5000
DDR_SUBSYS	NA	0xFF_FF00_5000	NA	0xFF00_5000
MISC_SUBSYS	0xFF_EC02_C000	0xFF_FC02_C000	0xBC02_C000	0xFC02_C000
VI_SUBSYS	0xFF_E404_0000	0xFF_F404_0000	0xB404_0000	0xF404_0000
VO_SUBSYS	0xFF_EF52_8000	0xFF_FF52_8000	0xBF52_8000	0xFF52_8000
VP_SUBSYS	0xFF_ECC3_0000	0xFF_FCC3_0000	0xBCC3_0000	0xFCC3_0000
DSP_SUBSYS	0xFF_EF04_0000	0xFF_FF04_0000	0xBF04_0000	0xFF04_0000
AUDIO_SUBSYS	NA	0xFF_CB00_0000	NA	0xCB00_0000

5.4.1.1 AON_SUBSYS

Register	Offset	Description	Section/Page
RST_CNT	0x00	Global soft reset delay counter register	5.4.2.1.1/462
SYS_RST_CFG	0x10	System soft reset configuration register	5.4.2.1.2/463
RTC_RST_CFG	0x14	RTC soft reset configuration register	5.4.2.1.3/463
AOGPIO_RST_CFG	0x18	AOGPIO soft reset configuration register	5.4.2.1.4/464
AOI2C_RST_CFG	0x1c	AOI2C soft reset configuration register	5.4.2.1.5/464
PVTC_RST_CFG	0x20	PVTC soft reset configuration register	5.4.2.1.6/464
E902_RST_CFG	0x24	E902 soft reset configuration register	5.4.2.1.7/465
AOTIMER_RST_CFG	0x28	AOTIMER soft reset configuration register	5.4.2.1.8/465
AOWDT_RST_CFG	0x2c	AOWDT soft reset configuration register	5.4.2.1.9/466
APSYS_RST_CFG	0x30	APSYS soft reset configuration register	5.4.2.1.10/466
NPUSYS_RST_CFG	0x34	NPUSYS soft reset configuration register	5.4.2.1.11/466
DDRSYS_RST_CFG	0x38	DDRSYS soft reset configuration register	5.4.2.1.12/467

Register	Offset	Description	Section/Page
AUDIO_RST_CFG	0x3c	AUDIOSYS soft reset configuration register	5.4.2.1.13/467
BISR_RST_CFG	0x50	Reserved	5.4.2.1.14/468
DSP0_RST_CFG	0x54	DSP0 soft reset configuration register	5.4.2.1.15/468
DSP1_RST_CFG	0x58	DSP1 soft reset configuration register	5.4.2.1.16/469
GPU_RST_CFG	0x5c	GPU soft reset configuration register	5.4.2.1.17/469
VDEC_RST_CFG	0x60	VDEC soft reset configuration register	5.4.2.1.18/469
VENC_RST_CFG	0x64	VENC soft reset configuration register	5.4.2.1.19/470
ADC_RST_CFG	0x70	ADC soft reset configuration register	5.4.2.1.20/470
AUDGPIO_RST_CFG	0x74	AUDGPIO soft reset configuration register	5.4.2.1.21/470
AOUART_RST_CFG	0x78	AOUART soft reset configuration register	5.4.2.1.22/471
RST_CLR_0	0x100	RST status clear configuration register 0	5.4.2.1.23/471
RST_CLR_1	0x104	RST status clear configuration register 1	5.4.2.1.24/471
RST_CLR_2	0x108	RST status clear configuration register 2	5.4.2.1.25/472
RST_CLR_3	0x10c	RST status clear configuration register 3	5.4.2.1.26/472
RST_CLR_4	0x110	RST status clear configuration register 4	5.4.2.1.27/472
RST_STS_0	0x120	RST status register 0	5.4.2.1.28/473
RST_STS_1	0x124	RST status register 1	5.4.2.1.29/473
RST_STS_2	0x128	RST status register 2	5.4.2.1.30/473
RST_STS_3	0x12c	RST status register 3	5.4.2.1.31/473
RST_STS_4	0x130	RST status register 4	5.4.2.1.32/474
RST_REQ_EN_0	0x140	RST request enable configuration register 0	5.4.2.1.33/474
RST_REQ_EN_1	0x144	RST request enable configuration register 1	5.4.2.1.34/474
RST_REQ_EN_2	0x148	RST request enable configuration register 2	5.4.2.1.35/474
RST_REQ_EN_3	0x14c	RST request enable configuration register 3	5.4.2.1.36/475
SRAM_AXI_RST_CFG	0x11f4	SRAM_AXI soft reset configuration register	5.4.2.1.37/475
SE_RST_CFG	0x160	SE soft reset configuration register	5.4.2.1.38/476

5.4.1.2 AP_SUBSYS

Register	Offset	Description	Section/Page
C910_BROM_SWRST	0x000	C910_BROM soft reset configuration register	5.4.2.2.1/476
C910_SWRST	0x004	C910 soft reset configuration register	5.4.2.2.2/476
CHIP_DBG_SWRST	0x00c	CHIP_DBG soft reset configuration register	5.4.2.2.3/477
AXI4_CPUSYS2_SWRST	0x010	AXI4_CPUSYS2 soft reset configuration register	5.4.2.2.4/477
X2X_CPUSYS_SWRST	0x014	X2X_CPUSYS soft reset configuration register	5.4.2.2.5/477
X2H_CPUSYS_SWRST	0x018	X2H_CPUSYS soft reset configuration register	5.4.2.2.6/478
AHB2_CPUSYS_SWRST	0x01c	AHB2_CPUSYS soft reset configuration register	5.4.2.2.7/478
APB3_CPUSYS_SWRST	0x020	APB3_CPUSYS soft reset configuration register	5.4.2.2.8/478
MBOX0_SWRST	0x024	MBOX0 soft reset configuration register	5.4.2.2.9/479
MBOX1_SWRST	0x028	MBOX1 soft reset configuration register	5.4.2.2.10/479
MBOX2_SWRST	0x02c	MBOX2 soft reset configuration register	5.4.2.2.11/479
MBOX3_SWRST	0x030	MBOX3 soft reset configuration register	5.4.2.2.12/479
WDT0_SWRST	0x034	WDT0 soft reset configuration register	5.4.2.2.13/480
WDT1_SWRST	0x038	WDT1 soft reset configuration register	5.4.2.2.14/480
TIMER0_SWRST	0x03c	TIMER0 soft reset configuration register	5.4.2.2.15/480
TIMER1_SWRST	0x040	TIMER1 soft reset configuration register	5.4.2.2.16/480
PERISYS_AHB_SWRST	0x044	PERISYS_AHB soft reset configuration register	5.4.2.2.17/481
PERISYS_APB1_SWRST	0x048	PERISYS_APB1 soft reset configuration register	5.4.2.2.18/481
PERISYS_APB2_SWRST	0x04c	PERISYS_APB2 soft reset configuration register	5.4.2.2.19/481
GMAC0_SWRST	0x068	GAMC soft reset configuration register	5.4.2.2.20/482
UART0_SWRST	0x070	UART0 soft reset configuration register	5.4.2.2.21/482
UART1_SWRST	0x074	UART1 soft reset configuration register	5.4.2.2.22/482

Register	Offset	Description	Section/Page
UART2_SWRST	0x078	UART2 soft reset configuration register	5.4.2.2.23/483
UART3_SWRST	0x07c	UART3 soft reset configuration register	5.4.2.2.24/483
UART4_SWRST	0x080	UART4 soft reset configuration register	5.4.2.2.25/483
UART5_SWRST	0x084	UART5 soft reset configuration register	5.4.2.2.26/484
QSPI0_SWRST	0x08c	QSPI0 soft reset configuration register	5.4.2.2.27/484
QSPI1_SWRST	0x090	QSPI1 soft reset configuration register	5.4.2.2.28/484
SPI_SWRST	0x094	SPI soft reset configuration register	5.4.2.2.29/485
I2C0_SWRST	0x098	I2C0 soft reset configuration register	5.4.2.2.30/485
I2C1_SWRST	0x09c	I2C1 soft reset configuration register	5.4.2.2.31/485
I2C2_SWRST	0x0a0	I2C2 soft reset configuration register	5.4.2.2.32/486
I2C3_SWRST	0x0a4	I2C3 soft reset configuration register	5.4.2.2.33/486
I2C4_SWRST	0x0a8	I2C4 soft reset configuration register	5.4.2.2.34/486
I2C5_SWRST	0x0ac	I2C5 soft reset configuration register	5.4.2.2.35/487
GPIO0_SWRST	0x0b0	GPIO0 soft reset configuration register	5.4.2.2.36/487
GPIO1_SWRST	0x0b4	GPIO1 soft reset configuration register	5.4.2.2.37/487
GPIO2_SWRST	0x0b8	GPIO2 soft reset configuration register	5.4.2.2.38/488
PWM_SWRST	0x0c0	PWM soft reset configuration register	5.4.2.2.39/488
PADCTRL0_APSYS_SWRST	0x0c4	PADCTRL_APSYS soft reset configuration register	5.4.2.2.40/488
CPU2PERI_X2H_SWRST	0x0cc	CPU2PERI_X2H soft reset configuration register	5.4.2.2.41/489
AXI4_CFG_BUS_SWRST	0x0d4	AXI4_CFG_BUS soft reset configuration register	5.4.2.2.42/489
CPU2CFG_X2H_SWRST	0x0d8	CPU2CFG_X2H soft reset configuration register	5.4.2.2.43/489
CPU2CFG_X2X_SWRST	0x0dc	CPU2CFG_X2X soft reset configuration register	5.4.2.2.44/490
CPU2AON_X2H_SWRST	0x0e4	CPU2AON_X2H soft reset configuration register	5.4.2.2.45/490
AXI4_CPUSYS1_SWRST	0x0f8	AXI4_CPUSYS1 soft reset configuration register	5.4.2.2.46/490

Register	Offset	Description	Section/Page
AON2CPU_A2X_SWRST	0x0fc	AON2CPU_A2X soft reset configuration register	5.4.2.2.47/490
RESERVED_REG_1	0x100	Reserved	5.4.2.2.48/491
RESERVED_REG_2	0x104	Reserved	5.4.2.2.49/491
RESERVED_REG_3	0x108	Reserved	5.4.2.2.50/491
RESERVED_REG_4	0x10c	Reserved	5.4.2.2.51/491
NPUSYS_AXI_SWRST	0x128	NPUSYS_AXI soft reset configuration register	5.4.2.2.52/492
CPU2VP_X2P_SWRST	0x12c	CPU2VP_X2P soft reset configuration register	5.4.2.2.53/492
CPU2VI_X2H_SWRST	0x138	CPU2VI_X2H soft reset configuration register	5.4.2.2.54/492
BMU_C910_SWRST	0x148	BMU_C910 soft reset configuration register	5.4.2.2.55/493
DMAC_CPUSYS_SWRST	0x14c	DMAC_CPUSYS soft reset configuration register	5.4.2.2.56/493
SPINLOCK_SWRST	0x178	SPINLOCK soft reset configuration register	5.4.2.2.57/493
CFG2TEE_X2H_SWRST	0x188	CFG2TEE_X2H soft reset configuration register	5.4.2.2.58/494
DSMART_SWRST	0x18c	DSMART soft reset configuration register	5.4.2.2.59/494
GPIO3_SWRST	0x1a8	GPIO3 soft reset configuration register	5.4.2.2.60/494
I2S_SWRST	0x1ac	I2S soft reset configuration register	5.4.2.2.61/494
IMG_NNA_SWRST	0x1b0	IMG_NNA soft reset configuration register	5.4.2.2.62/495
PERI_APB3_SWRST	0x1dc	PERI_APB3 soft reset configuration register	5.4.2.2.63/495
VP_SUBSYS_SWRST	0x1ec	VP_SUBSYS soft reset configuration register	5.4.2.2.64/495
PERISYS_APB4_SWRST	0x1f8	PERISYS_APB4 soft reset configuration register	5.4.2.2.65/496
GMAC1_SWRST	0x204	GMAC1 soft reset configuration register	5.4.2.2.66/496
GMAC_AXI_SWRST	0x208	GMAC_AXI soft reset configuration register	5.4.2.2.67/496
PADCTRL1_APSYS_SWRST	0x20c	PADCTRL1_APSYS soft reset configuration register	5.4.2.2.68/497
VOSYS_AXI_SWRST	0x210	VOSYS_AXI soft reset configuration register	5.4.2.2.69/497
VOSYS_X2X_SWRST	0x214	VOSYS_X2X soft reset configuration register	5.4.2.2.70/497

Register	Offset	Description	Section/Page
MISC2VP_X2X_SWRST	0x218	MISC2VP_X2X soft reset configuration register	5.4.2.2.71/497
SUBSYS_SWRST	0x220	SUBSYS soft reset configuration register	5.4.2.2.72/498
C910_BROM_TEESWRST	0x1000	C910_BROM soft reset configuration register	5.4.2.2.73/498
C910_TEESWRST	0x1004	C910 soft reset configuration register	5.4.2.2.74/498
C910_DS_TEESWRST	0x1008	C910 DS soft reset configuration register	5.4.2.2.75/499
CHIP_DBG_TEESWRST	0x100c	CHIP_DBG soft reset configuration register	5.4.2.2.76/499
AXI4_CPUSYS2_TEESWRST	0x1010	AXI4_CPUSYS2 soft reset configuration register	5.4.2.2.77/500
X2X_CPUSYS_TEESWRST	0x1014	X2X_CPUSYS soft reset configuration register	5.4.2.2.78/500
X2H_CPUSYS_TEESWRST	0x1018	X2H_CPUSYS's soft reset configuration register	5.4.2.2.79/500
AHB2_CPUSYS_TEESWRST	0x101c	AHB2_CPUSYS soft reset configuration register	5.4.2.2.80/501
APB3_CPUSYS_TEESWRST	0x1020	APB3_CPUSYS soft reset configuration register	5.4.2.2.81/501
MBOX0_TEESWRST	0x1024	MBOX0 soft reset configuration register	5.4.2.2.82/501
MBOX1_TEESWRST	0x1028	MBOX1 soft reset configuration register	5.4.2.2.83/502
MBOX2_TEESWRST	0x102c	MBOX2 soft reset configuration register	5.4.2.2.84/502
MBOX3_TEESWRST	0x1030	MBOX3 soft reset configuration register	5.4.2.2.85/502
WDT0_TEESWRST	0x1034	WDT0 soft reset configuration register	5.4.2.2.86/502
WDT1_TEESWRST	0x1038	WDT1 soft reset configuration register	5.4.2.2.87/503
TIMER0_TEESWRST	0x103c	TIMER0 soft reset configuration register	5.4.2.2.88/503
TIMER1_TEESWRST	0x1040	TIMER1 soft reset configuration register	5.4.2.2.89/503
PERISYS_AHB_TEESWRST	0x1044	PERISYS_AHB soft reset configuration register	5.4.2.2.90/504
PERISYS_APB1_TEESWRST	0x1048	PERISYS_APB1 soft reset configuration register	5.4.2.2.91/504
PERISYS_APB2_TEESWRST	0x104c	PERISYS_APB2 soft reset configuration register	5.4.2.2.92/504

Register	Offset	Description	Section/Page
GMAC0_TEESWRST	0x1068	GAMC soft reset configuration register	5.4.2.2.93/504
UART0_TEESWRST	0x1070	UART0 soft reset configuration register	5.4.2.2.94/505
UART1_TEESWRST	0x1074	UART1 soft reset configuration register	5.4.2.2.95/505
UART2_TEESWRST	0x1078	UART2 soft reset configuration register	5.4.2.2.96/505
UART3_TEESWRST	0x107c	UART3 soft reset configuration register	5.4.2.2.97/506
UART4_TEESWRST	0x1080	UART4 soft reset configuration register	5.4.2.2.98/506
UART5_TEESWRST	0x1084	UART5 soft reset configuration register	5.4.2.2.99/506
QSPI0_TEESWRST	0x108c	QSPI0 soft reset configuration register	5.4.2.2.100/507
QSPI1_TEESWRST	0x1090	QSPI1 soft reset configuration register	5.4.2.2.101/507
SPI_TEESWRST	0x1094	SPI soft reset configuration register	5.4.2.2.102/507
I2C0_TEESWRST	0x1098	I2C0 soft reset configuration register	5.4.2.2.103/508
I2C1_TEESWRST	0x109c	I2C1 soft reset configuration register	5.4.2.2.104/508
I2C2_TEESWRST	0x10a0	I2C2 soft reset configuration register	5.4.2.2.105/508
I2C3_TEESWRST	0x10a4	I2C3 soft reset configuration register	5.4.2.2.106/509
I2C4_TEESWRST	0x10a8	I2C4 soft reset configuration register	5.4.2.2.107/509
I2C5_TEESWRST	0x10ac	I2C5 soft reset configuration register	5.4.2.2.108/509
GPIO0_TEESWRST	0x10b0	GPIO0 soft reset configuration register	5.4.2.2.109/510
GPIO1_TEESWRST	0x10b4	GPIO1 soft reset configuration register	5.4.2.2.110/510
GPIO2_TEESWRST	0x10b8	GPIO2 soft reset configuration register	5.4.2.2.111/510
PWM_TEESWRST	0x10c0	PWM soft reset configuration register	5.4.2.2.112/511
PADCTRL0_APSYS_TEESWRST	0x10c4	PADCTRL_APSYS soft reset configuration register	5.4.2.2.113/511
CPU2PERI_X2H_TEESWRST	0x10cc	CPU2PERI_X2H soft reset configuration register	5.4.2.2.114/511
AXI4_CFG_BUS_TEESWRST	0x10d4	AXI4_CFG_BUS soft reset configuration register	5.4.2.2.115/512
CPU2CFG_X2H_TEESWRST	0x10d8	CPU2CFG_X2H soft reset configuration register	5.4.2.2.116/512
CPU2CFG_X2X_TEESWRST	0x10dc	CPU2CFG_X2X soft reset configuration register	5.4.2.2.117/512

Register	Offset	Description	Section/Page
CPU2AON_X2H_TEESWRST	0x10e4	CPU2AON_X2H soft reset configuration register	5.4.2.2.118/513
AXI4_CPUSYS1_TEESWRST	0x10f8	AXI4_CPUSYS1 soft reset configuration register	5.4.2.2.119/513
AON2CPU_A2X_TEESWRST	0x10fc	AON2CPU_A2X soft reset configuration register	5.4.2.2.120/513
RESERVED_REG_1_TEE	0x1100	Reserved	5.4.2.2.121/513
RESERVED_REG_2_TEE	0x1104	Reserved	5.4.2.2.122/514
RESERVED_REG_3_TEE	0x1108	Reserved	5.4.2.2.123/514
RESERVED_REG_4_TEE	0x110c	Reserved	5.4.2.2.124/514
NPUSYS_AXI_TEESWRST	0x1128	NPUSYS_AXI soft reset configuration register	5.4.2.2.125/514
CPU2VP_X2P_TEESWRST	0x112c	CPU2VP_X2P soft reset configuration register	5.4.2.2.126/515
CPU2VI_X2H_TEESWRST	0x1138	CPU2VI_X2H soft reset configuration register	5.4.2.2.127/515
BMU_C910_TEESWRST	0x1148	BMU_C910 soft reset configuration register	5.4.2.2.128/515
DMAC_CPUSYS_TEESWRST	0x114c	DMAC_CPUSYS soft reset configuration register	5.4.2.2.129/516
SPINLOCK_TEESWRST	0x1178	SPINLOCK soft reset configuration register	5.4.2.2.130/516
CFG2TEE_X2H_TEESWRST	0x1188	CFG2TEE_X2H soft reset configuration register	5.4.2.2.131/516
DSMART_TEESWRST	0x118c	DSMART soft reset configuration register	5.4.2.2.132/517
GPIO3_TEESWRST	0x11a8	GPIO3 soft reset configuration register	5.4.2.2.133/517
I2S_TEESWRST	0x11ac	I2S soft reset configuration register	5.4.2.2.134/517
IMG_NNA_TEESWRST	0x11b0	IMG_NNA soft reset configuration register	5.4.2.2.135/517
PERI_APB3_TEESWRST	0x11dc	PERI_APB3 soft reset configuration register	5.4.2.2.136/518
VP_SUBSYS_TEESWRST	0x11ec	VP_SUBSYS soft reset configuration register	5.4.2.2.137/518
PERISYS_APB4_TEESWRST	0x11f8	PERISYS_APB4 soft reset configuration register	5.4.2.2.138/518
GMAC1_TEESWRST	0x1204	GMAC1 soft reset configuration register	5.4.2.2.139/519
GMAC_AXI_TEESWRST	0x1208	GMAC_AXI soft reset configuration register	5.4.2.2.140/519

Register	Offset	Description	Section/Page
PADCTRL1_APSYS_TEESWRST	0x120c	GMAC_APB soft reset configuration register	5.4.2.2.141/519
VOSYS_AXI_TEESWRST	0x1210	VOSYS_AXI soft reset configuration register	5.4.2.2.142/520
VOSYS_X2X_TEESWRST	0x1214	VOSYS_X2X soft reset configuration register	5.4.2.2.143/520
MISC2VP_X2X_TEESWRST	0x1218	MISC2VP_X2X soft reset configuration register	5.4.2.2.144/520
SUBSYS_TEESWRST	0x1220	SUBSYS soft reset configuration register	5.4.2.2.145/520
IOPMP_TEESWRST	0x1500	IOPMP soft reset configuration register	5.4.2.2.146/521
RST_LOCK_0	0x1800	RST LOCK configuration register0	5.4.2.2.147/522
RST_LOCK_1	0x1804	RST LOCK configuration register1	5.4.2.2.148/524
RST_LOCK_2	0x1808	RST LOCK configuration register2	5.4.2.2.149/526
RST_LOCK_3	0x180c	RST LOCK configuration register3	5.4.2.2.150/528

5.4.1.3 DDR_SUBSYS

Register	Offset	Description	Section/Page
DDR_CFG0	0x0	Misc configuration of DDR subsystem	5.4.2.3.1/529

5.4.1.4 MISC_SUBSYS

Register	Offset	Description	Section/Page
EMMC_SWRST	0x0000	eMMC soft reset configuration register	5.4.2.4.1/530
MISCSYS_AXI_SWRST	0x0008	MISCSYS AXI bus soft reset configuration register	5.4.2.4.2/530
SDIO0_SWRST	0x000C	SDIO0 soft reset configuration register	5.4.2.4.3/531
SDIO1_SWRST	0x0010	SDIO1 soft reset configuration register	5.4.2.4.4/531
USB3_DRD_SWRST	0x0014	USB3_DRD soft reset configuration register	5.4.2.4.5/531
EMMC_SWRST_TEE	0x1000	eMMC soft reset configuration register	5.4.2.4.6/532
MISCSYS_AXI_SWRST_TEE	0x1008	MISCSYS AXI bus soft reset configuration register	5.4.2.4.7/532
SDIO0_SWRST_TEE	0x100C	SDIO0 soft reset configuration register	5.4.2.4.8/532
SDIO1_SWRST_TEE	0x1010	SDIO1 soft reset configuration register	5.4.2.4.9/533
USB3_DRD_SWRST_TEE	0x1014	USB3_DRD soft reset configuration register	5.4.2.4.10/533

Register	Offset	Description	Section/Page
TEESTS_AHB_TEESWRST_TEE	0x1020	TEE subsystem AHB bus reset configuration register	5.4.2.4.11/533
TEESTS_APB_TEESWRST_TEE	0x1024	TEE subsystem APB bus reset configuration register	5.4.2.4.12/534
TEESTS_AXI_TEESWRST_TEE	0x1028	TEE subsystem AXI bus reset configuration register	5.4.2.4.13/534
TEESYS_X2X_TEESWRST_TEE	0x102c	TEE subsystem X2X bus reset configuration register	5.4.2.4.14/534
TEESYS_REG_TEESWRST_TEE	0x1030	TEE subsystem sysreg bus reset configuration register	5.4.2.4.15/534
TEEDMAC_TEESWRST_TEE	0x1034	TEE subsystem DMA module reset configuration register	5.4.2.4.16/535
EFUSE_TEESWRST_TEE	0x1038	TEE subsystem eFuse module reset configuration register	5.4.2.4.17/535
EIP120SI_TEESWRST_TEE	0x103C	TEE subsystem EIP120SI module reset configuration register	5.4.2.4.18/535
EIP120SII_TEESWRST_TEE	0x1040	TEE subsystem EIP120SII module reset configuration register	5.4.2.4.19/536
EIP120SIII_TEESWRST_TEE	0x1044	TEE subsystem EIP120SIII module reset configuration register	5.4.2.4.20/536
EIP150B_TEESWRST_TEE	0x1048	TEE subsystem EIP150B module reset configuration register	5.4.2.4.21/536
OCRAM_TEESWRST_TEE	0x104C	TEE subsystem OCRAM module reset configuration register	5.4.2.4.22/537
IOPMP_TEESWRST_TEE	0x1050	TEE subsystem IOPMP module reset configuration register	5.4.2.4.23/537
DS_TEESWRST_TEE	0x1054	TEE subsystem DS module reset configuration register	5.4.2.4.24/538
KEYRAM_TEESWRST_TEE	0x1058	TEE subsystem KEYRAM module reset configuration register	5.4.2.4.25/538

5.4.1.5 VI_SUBSYS

Register	Offset	Description	Section/Page
VISYS_SW_RST	0x100	VISYS_SW_RST1	5.4.2.5.1/539

Register	Offset	Description	Section/Page
VISYS_SW_RST2	0x104	VISYS_SW_RST2	5.4.2.5.2/540
VISYS_SW_RST_TEE	0x1100	VISYS_SW_RST1	5.4.2.5.3/541
VISYS_SW_RST2_TEE	0x1104	VISYS_SW_RST2	5.4.2.5.4/542
CFG_RST_LOCK_TEE	0x1210	VI reset register TEE lock	5.4.2.5.5/544

5.4.1.6 VO_SUBSYS

Register	Offset	Description	Section/Page
GPU_RST_CFG	0x00	GPU reset register	5.4.2.6.1/546
DPU_RST_CFG	0x04	DPU reset register	5.4.2.6.2/546
MIPI_DSI0_RST_CFG	0x8	DSI0 reset register	5.4.2.6.3/546
MIPI_DSI1_RST_CFG	0xc		5.4.2.6.4/547
HDMI_RST_CFG	0x14		5.4.2.6.5/547
AXI4_VO_DW_AXI	0x18	AXI4 bus reset register	5.4.2.6.6/547
X2H_X4_VOSYS_DW_AXI_X2H	0x20	X2H bus reset register	5.4.2.6.7/547
GPU_RST_CFG_TEE	0x1000	GPU reset TEE register	5.4.2.6.8/548
DPU_RST_CFG_TEE	0x1004	DPU reset TEE register	5.4.2.6.9/548
MIPI_DSI0_RST_CFG_TEE	0x1008	DSI0 APB reset TEE register	5.4.2.6.10/549
MIPI_DSI1_RST_CFG_TEE	0x100c	DSI1 APB reset TEE register	5.4.2.6.11/549
IOPMP_VOSYS_RST_CFG_TEE	0x1010	IOPMP reset TEE register	5.4.2.6.12/549
HDMI_RST_CFG_TEE	0x1014	HDMI reset TEE register	5.4.2.6.13/550
AXI4_VO_DW_AXI_TEE	0x1018	AXI4_VO bus reset TEE register	5.4.2.6.14/551
X2H_X4_VOSYS_DW_AXI_X2H_TEE	0x1020	X2H reset TEE register	5.4.2.6.15/551
CFG_LOCK_TEE	0x1a00	Configuration lock TEE register	5.4.2.6.16/552

5.4.1.7 VP_SUBSYS

Register	Offset	Description	Section/Page
AXIBUS_RST_CFG	0x00	AXIBUS_RST_CFG	5.4.2.7.1/552
FCE_RST_CFG	0x04	FCE_RST_CFG	5.4.2.7.2/553

Register	Offset	Description	Section/Page
G2D_RST_CFG	0x08	G2D_RST_CFG	5.4.2.7.3/553
VDEC_RST_CFG	0x0c	VDEC_RST_CFG	5.4.2.7.4/554
VENC_RST_CFG	0x10	VENC_RST_CFG	5.4.2.7.5/555
AXIBUS_RST_TEECFG	0x1000	AXIBUS_RST_TEECFG	5.4.2.7.6/555
FCE_RST_TEECFG	0x1004	FCE_RST_TEECFG	5.4.2.7.7/555
G2D_RST_TEECFG	0x1008	G2D_RST_TEECFG	5.4.2.7.8/556
VDEC_RST_TEECFG	0x100c	VDEC_RST_TEECFG	5.4.2.7.9/557
VENC_RST_TEECFG	0x1010	VENC_RST_TEECFG	5.4.2.7.10/558

5.4.1.8 DSP_SUBSYS

Register	Offset	Description	Section/Page
DSPSYS_SW_RST	0x28	DSP subsystem reset register	5.4.2.8.1/559
DSPSYS_SW_RST_TEE	0x1028	DSP subsystem reset TEE register	5.4.2.8.2/560
CFG_CLK_LOCK_TEE	0x1140	Clock lock TEE register	5.4.2.8.3/562
CFG_RST_LOCK_TEE	0x1144	Reset lock TEE register	5.4.2.8.4/563
CFG_DSPSYS_LOCK_TEE	0x1148	DSP subsystem lock TEE register	5.4.2.8.5/563

5.4.1.9 AUDIO_SUBSYS

Register	Offset	Description	Section/Page
IP_RST_REG	0x14	Module reset control register	5.4.2.9.1/564

5.4.2 Register and Field Description

5.4.2.1 AON_SUBSYS

5.4.2.1.1 RST_CNT

- Description: Global soft reset delay counter register
- Offset: 0x00
- Default Value: 0xf0f

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	

Bits	Field Name	Access	Description
[17]	R_DLY_CNT_EN	RW	Delay count enable Value After Reset: 0x0
[16]	R_RST_CNT_EN	RW	Reset count enable Value After Reset: 0x0
[15:8]	R_DLY_CNT	RW	Global soft reset delay count, such as wdt reset, soft reset, with 24MHz crystal clock as the reference period, for example, the delay value of 1us is 24. Value After Reset: 0xF
[7:0]	R_RST_CNT	RW	Global soft reset delay count, such as wdt reset, soft reset, with 24MHz crystal clock as the reference period, for example, the delay value of 1us is 24. Value After Reset: 0xF

5.4.2.1.2 SYS_RST_CFG

- Description: System soft reset configuration register
- Offset: 0x10
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_SYS_RST_REQ	RW	System global soft reset Value After Reset: 0x0

5.4.2.1.3 RTC_RST_CFG

- Description: RTC soft reset configuration register
- Offset: 0x14
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_RTC_CRST_N	RW	RTC reference reset soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1
[0]	SW_RTC_PRST_N	RW	RTC APB reset soft reset 0: Assert reset.

Bits	Field Name	Access	Description
			1: Deassert reset. Value After Reset: 0x1

5.4.2.1.4 AOGPIO_RST_CFG

- Description: AOGPIO soft reset configuration register
- Offset: 0x18
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_AOGPIO_PRST_N	RW	AOGPIO APB soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1
[0]	SW_AOGPIO_DBCLK_RST_N	RW	AOGPIO debounce soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1

5.4.2.1.5 AOI2C_RST_CFG

- Description: AOI2C soft reset configuration register
- Offset: 0x1c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_AOI2C_PRST_N	RW	AOI2C APB reset soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1

5.4.2.1.6 PVTC_RST_CFG

- Description: PVTC soft reset configuration register
- Offset: 0x20
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_PVTC_PRST_N	RW	PVTC APB reset soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1

5.4.2.1.7 E902_RST_CFG

- Description: E902 soft reset configuration register
- Offset: 0x24
- Default Value: 0x2

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_E902_HAD_RST_N	RW	E902 HAD reset soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1
[0]	SW_E902_CRST_N	RW	E902 core reset soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x0

5.4.2.1.8 AOTIMER_RST_CFG

- Description: AOTIMER soft reset configuration register
- Offset: 0x28
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_AOTIMER_CRST_N	RW	AOTIMER core reset soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1
[0]	SW_AOTIMER_PRST_N	RW	AOTIMER APB reset soft reset 0: Assert reset.

Bits	Field Name	Access	Description
			1: Deassert reset. Value After Reset: 0x1

5.4.2.1.9 AOWDT_RST_CFG

- Description: AOWDT soft reset configuration register
- Offset: 0x2c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_AOWDT_PRST_N	RW	AOWDT APB reset soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1

5.4.2.1.10 APSYS_RST_CFG

- Description: APSYS soft reset configuration register
- Offset: 0x30
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_APSYS_RST_N	RW	APSYS soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1

5.4.2.1.11 NPUSYS_RST_CFG

- Description: NPUSYS soft reset configuration register
- Offset: 0x34
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_NPUSYS_RST_N	RW	NPUSYS soft reset 0: Assert reset.

Bits	Field Name	Access	Description
			1: Deassert reset. Value After Reset: 0x1

5.4.2.1.12 DDRSYS_RST_CFG

- Description: DDRSYS soft reset configuration register
- Offset: 0x38
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_DDRSYS_RST_N	RW	DDRSYS soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1

5.4.2.1.13 AUDIO_RST_CFG

- Description: AUDIOSYS soft reset configuration register
- Offset: 0x3c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	SW_AUDIO_RST_N	RW	AUDIOSYS's soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x0
[4]	SW_AUDIO_SUBSYS_IOPMP_CP_RST_N	RW	AUDIOSYS IOPMP soft reset 0: Assert reset. 1: Deassert reset. The IOPMP interrupt should be masked before reset. Value After Reset: 0x0
[3]	SW_AUDIO_SUBSYS_CRST_N	RW	AUDIOSYS core soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x0

Bits	Field Name	Access	Description
[2]	SW_AUDIO_SUBSYS_ARST_N_CP2SRAM	RW	CP2SRAM AXI soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x0
[1]	SW_AUDIO_SUBSYS_ARST_N_CP2AP	RW	CP2AP AXI soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x0
[0]	SW_AUDIO_SUBSYS_ARST_N_AP2CP	RW	AP2CP AXI soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x0

5.4.2.1.14 BISR_RST_CFG

- Description: Reserved
- Offset: 0x50
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_BISR_L2_RST_N	RW	Reserved. Value After Reset: 0x1
[0]	SW_BISR_SRAM_RST_N	RW	Reserved Value After Reset: 0x1

5.4.2.1.15 DSP0_RST_CFG

- Description: DSP0 soft reset configuration register
- Offset: 0x54
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_DSP0_RST_N	RW	DSP0 soft reset 0: Assert reset. 1: Deassert reset.

Bits	Field Name	Access	Description
			Value After Reset: 0x1

5.4.2.1.16 DSP1_RST_CFG

- Description: DSP1 soft reset configuration register
- Offset: 0x58
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_DSP1_RST_N	RW	DSP1 soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1

5.4.2.1.17 GPU_RST_CFG

- Description: GPU soft reset configuration register
- Offset: 0x5c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_GPU_RST_N	RW	GPU soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1

5.4.2.1.18 VDEC_RST_CFG

- Description: VDEC soft reset configuration register
- Offset: 0x60
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_VDEC_RST_N	RW	VDEC soft reset 0: Assert reset. 1: Deassert reset.

Bits	Field Name	Access	Description
			Value After Reset: 0x1

5.4.2.1.19 VENC_RST_CFG

- Description: VENC soft reset configuration register
- Offset: 0x64
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_VENC_RST_N	RW	VENC soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1

5.4.2.1.20 ADC_RST_CFG

- Description: ADC soft reset configuration register
- Offset: 0x70
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_ADC_PRST_N	RW	ADC APB reset soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1

5.4.2.1.21 AUDGPIO_RST_CFG

- Description: AUDGPIO soft reset configuration register
- Offset: 0x74
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_AUDGPIO_PRST_N	RW	AUDGPIO APB reset soft reset 0: Assert reset. 1: Deassert reset.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[0]	SW_AUDGPIO_DBCLK_RST_N	RW	AUDGPIO debounce reset soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1

5.4.2.1.22 AOUART_RST_CFG

- Description: AOUART soft reset configuration register
- Offset: 0x78
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_AOUART_PRST_N	RW	AOUART APB reset soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1
[0]	SW_AOUART_S_RST_N	RW	AOUART interface reset soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1

5.4.2.1.23 RST_CLR_0

- Description: Reset status clear configuration register 0
- Offset: 0x100
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1:0]	R_RST_CLR_0	RW	Reset status clear [0]: r_por_rst_sts [1]: r_ext_rst_sts Value After Reset: 0x0

5.4.2.1.24 RST_CLR_1

- Description: Reset status clear configuration register 1

- Offset: 0x104
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	R_RST_CLR_1	RW	Reset status clear Table 3-2 bit[31:0] Value After Reset: 0x0

5.4.2.1.25 RST_CLR_2

- Description: Reset status clear configuration register 2
- Offset: 0x108
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	R_RST_CLR_2	RW	Reset status clear Table 3-2 bit[63:32] Value After Reset: 0x0

5.4.2.1.26 RST_CLR_3

- Description: Reset status clear configuration register 3
- Offset: 0x10c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	R_RST_CLR_3	RW	Reset status clear Table 3-2 bit[95:64] Value After Reset: 0x0

5.4.2.1.27 RST_CLR_4

- Description: Reset status clear configuration register 4
- Offset: 0x110
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	R_RST_CLR_4	RW	Reset status clear Table 3-2 bit[127:96] Value After Reset: 0x0

5.4.2.1.28 RST_STS_0

- Description: Reset status register 0
- Offset: 0x120
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1:0]	R_RST_STS_0	RO	Reset status [0]: r_por_rst_sts [1]: r_ext_rst_sts Value After Reset: 0x0

5.4.2.1.29 RST_STS_1

- Description: Reset status register 1
- Offset: 0x124
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	R_RST_STS_1	RO	Reset status Table 3-2 bit[31:0] Value After Reset: 0x0

5.4.2.1.30 RST_STS_2

- Description: Reset status register 2
- Offset: 0x128
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	R_RST_STS_2	RO	Reset status Table 3-2 bit[63:32] Value After Reset: 0x0

5.4.2.1.31 RST_STS_3

- Description: Reset status register 3
- Offset: 0x12c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	R_RST_STS_3	RO	Reset status Table 3-2 bit[95:64] Value After Reset: 0x0

5.4.2.1.32 RST_STS_4

- Description: Reset status register 4
- Offset: 0x130
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	R_RST_STS_4	RO	Reset status Table 3-2 bit[127:96] Value After Reset: 0x0

5.4.2.1.33 RST_REQ_EN_0

- Description: Reset request enable configuration register 0
- Offset: 0x140
- Default Value: 0x11100

Bits	Field Name	Access	Description
[31:0]	R_RST_REQ_EN_0	RW	Reset request enable Table 3-2 bit[31:0] Value After Reset: 0x11100

5.4.2.1.34 RST_REQ_EN_1

- Description: Reset request enable configuration register 1
- Offset: 0x144

1. Default Value: 0xbb000000

Bits	Field Name	Access	Description
[31:0]	R_RST_REQ_EN_1	RW	Reset request enable Table 3-2 bit[63:32] Value After Reset: 0xBB000000

5.4.2.1.35 RST_REQ_EN_2

- Description: Reset request enable configuration register 2
- Offset: 0x148

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	R_RST_REQ_EN_2	RW	Reset request enable Table 3-2 bit[95:64] Value After Reset: 0x0

5.4.2.1.36 RST_REQ_EN_3

- Description: Reset request enable configuration register 3
- Offset: 0x14c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	R_RST_REQ_EN_3	RW	Reset request enable Table 3-2 bit[127:96] Value After Reset: 0x0

5.4.2.1.37 SRAM_AXI_RST_CFG

- Description: SRAM_AXI soft reset configuration register
- Offset: 0x11f4
- Default Value: 0x5f

Bits	Field Name	Access	Description
[31:7]	RESERVED_2	-	
[6]	SW_SRAM_AXI_CORE_RST_N	RW	SRAM_AXI core soft reset, active low Value After Reset: 0x1
[5]	RESERVED_1	-	
[4]	SW_SRAM_AXI_ARST_N_4	RW	SRAM_AXI slave port4 soft reset, active low Value After Reset: 0x1
[3]	SW_SRAM_AXI_ARST_N_3	RW	SRAM_AXI slave port3 soft reset, active low Value After Reset: 0x1
[2]	SW_SRAM_AXI_ARST_N_2	RW	SRAM_AXI slave port2 soft reset, active low Value After Reset: 0x1
[1]	SW_SRAM_AXI_ARST_N_1	RW	SRAM_AXI slave port1 soft reset, active low Value After Reset: 0x1
[0]	SW_SRAM_AXI_ARST_N_0	RW	SRAM_AXI slave port0 soft reset, active low Value After Reset: 0x1

5.4.2.1.38 SE_RST_CFG

- Description: SE soft reset configuration register
- Offset: 0x160
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	PAD_SE_RST_N	RW	SE soft reset 0: Assert reset. 1: Deassert reset. Value After Reset: 0x1

5.4.2.2 AP_SUBSYS

5.4.2.2.1 C910_BROM_SWRST

- Description: C910_BROM soft reset configuration register
- Offset: 0x000
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_C910_BROM_HRST_N	RW	C910_BROM soft reset, active low Value After Reset: 0x1

5.4.2.2.2 C910_SWRST

- Description: C910 soft reset configuration register
- Offset: 0x004
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	SW_C910_CORE3_RST_N	RW	C910 core3 soft reset, active low Value After Reset: 0x0
[3]	SW_C910_CORE2_RST_N	RW	C910 core2 soft reset, active low Value After Reset: 0x0
[2]	SW_C910_CORE1_RST_N	RW	C910 core1 soft reset, active low Value After Reset: 0x0

Bits	Field Name	Access	Description
[1]	SW_C910_CORE0_RST_N	RW	C910 core0 soft reset, active low Value After Reset: 0x1
[0]	SW_C910_RST_N	RW	C910 top soft reset, active low Value After Reset: 0x1

5.4.2.2.3 CHIP_DBG_SWRST

- Description: CHIP_DBG's soft reset configuration register
- Offset: 0x00c
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_CHIP_DBG_ARST_N	RW	CHIP_DBG AXI soft reset, active low. sw_chip_dbg_arst_n should be asserted before sw_chip_dbg_crst_n, and be deasserted after sw_chip_dbg_crst_n. Value After Reset: 0x1
[0]	SW_CHIP_DBG_CRST_N	RW	CHIP_DBG core soft reset, active low. sw_chip_dbg_arst_n should be asserted before sw_chip_dbg_crst_n, and be deasserted after sw_chip_dbg_crst_n. Value After Reset: 0x1

5.4.2.2.4 AXI4_CPUSYS2_SWRST

- Description: AXI4_CPUSYS2 soft reset configuration register
- Offset: 0x010
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_AXI4_CPUSYS2_PRST_N	RW	AXI4_CPUSYS2 APB soft reset, active low Value After Reset: 0x1
[0]	SW_AXI4_CPUSYS2_ARST_N	RW	AXI4_CPUSYS2 AXI soft reset, active low Value After Reset: 0x1

5.4.2.2.5 X2X_CPUSYS_SWRST

- Description: X2X_CPUSYS soft reset configuration register

- Offset: 0x014
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_X2X_CPUSYS_RST_N	RW	Reserved, software can't write it. Value After Reset: 0x1

5.4.2.2.6 X2H_CPUSYS_SWRST

- Description: X2H_CPUSYS soft reset configuration register
- Offset: 0x018
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_X2H_CPUSYS_RST_N	RW	X2H_CPUSYS soft reset, active low Value After Reset: 0x1

5.4.2.2.7 AHB2_CPUSYS_SWRST

- Description: AHB2_CPUSYS soft reset configuration register
- Offset: 0x01c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_AHB2_CPUSYS_HRST_N	RW	AHB2_CPUSYS AHB soft reset, active low Value After Reset: 0x1

5.4.2.2.8 APB3_CPUSYS_SWRST

- Description: APB3_CPUSYS soft reset configuration register
- Offset: 0x020
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_APB3_CPUSYS_HRST_N	RW	APB3_CPUSYS APB soft reset, active low Value After Reset: 0x1

5.4.2.2.9 MBOX0_SWRST

- Description: MBOX0 soft reset configuration register
- Offset: 0x024
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_MBOX0_PRST_N	RW	MBOX0 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.10 MBOX1_SWRST

- Description: MBOX1 soft reset configuration register
- Offset: 0x028
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_MBOX1_PRST_N	RW	MBOX1 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.11 MBOX2_SWRST

- Description: MBOX2 soft reset configuration register
- Offset: 0x02c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_MBOX2_PRST_N	RW	MBOX2 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.12 MBOX3_SWRST

- Description: MBOX3 soft reset configuration register
- Offset: 0x030
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_MBOX3_PRST_N	RW	MBOX3 APB soft reset, active low

Bits	Field Name	Access	Description
			Value After Reset: 0x1

5.4.2.2.13 WDT0_SWRST

- Description: WDT0 soft reset configuration register
- Offset: 0x034
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_WDT0_PRST_N	RW	WDT0 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.14 WDT1_SWRST

- Description: WDT1 soft reset configuration register
- Offset: 0x038
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_WDT1_PRST_N	RW	WDT1 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.15 TIMER0_SWRST

- Description: TIMER0 soft reset configuration register
- Offset: 0x03c
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_TIMER0_CRST_N	RW	Timer0 core soft reset, active low Value After Reset: 0x1
[0]	SW_TIMER0_PRST_N	RW	Timer0 APB bus soft reset, active low Value After Reset: 0x1

5.4.2.2.16 TIMER1_SWRST

- Description: TIMER1 soft reset configuration register
- Offset: 0x040

- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_TIMER1_CRST_N	RW	Timer1 core soft reset, active low Value After Reset: 0x1
[0]	SW_TIMER1_PRST_N	RW	Timer1 APB bus soft reset, active low Value After Reset: 0x1

5.4.2.2.17 PERISYS_AHB_SWRST

- Description: PERISYS_AHB soft reset configuration register
- Offset: 0x044
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_PERISYS_AHB_HRST_N	RW	PERISYS_AHB soft reset, active low Value After Reset: 0x1

5.4.2.2.18 PERISYS_APB1_SWRST

- Description: PERISYS_APB1 soft reset configuration register
- Offset: 0x048
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_PERISYS_APB1_HRST_N	RW	PERISYS_APB1 soft reset, active low Value After Reset: 0x1

5.4.2.2.19 PERISYS_APB2_SWRST

- Description: PERISYS_APB2 soft reset configuration register
- Offset: 0x04c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_PERISYS_APB2_HRST_N	RW	PERISYS_APB2 soft reset, active low Value After Reset: 0x1

5.4.2.2.20 GMAC0_SWRST

- Description: GAMC soft reset configuration register
- Offset: 0x068
- Default Value: 0xf

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	SW_GMAC0_ARST_N	RW	GMAC AXI soft reset, active low Value After Reset: 0x1
[2]	SW_GMAC0_GRST_N	RW	GMAC ephy_ref_clk_div soft reset, active low Value After Reset: 0x1
[1]	SW_GMAC0_HRST_N	RW	GMAC AHB soft reset, active low Value After Reset: 0x1
[0]	SW_GMAC0_PRST_N	RW	GMAC APB soft reset, active low Value After Reset: 0x1

5.4.2.2.21 UART0_SWRST

- Description: UART0 soft reset configuration register
- Offset: 0x070
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_UART0_S_RST_N	RW	UART0 interface soft reset, active low Value After Reset: 0x1
[0]	SW_UART0_PRST_N	RW	UART0 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.22 UART1_SWRST

- Description: UART1 soft reset configuration register
- Offset: 0x074
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_UART1_S_RST_N	RW	UART1 interface soft reset, active low

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[0]	SW_UART1_PRST_N	RW	UART1 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.23 UART2_SWRST

- Description: UART2 soft reset configuration register
- Offset: 0x078
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_UART2_S_RST_N	RW	UART2 interface soft reset, active low Value After Reset: 0x1
[0]	SW_UART2_PRST_N	RW	UART2 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.24 UART3_SWRST

- Description: UART3 soft reset configuration register
- Offset: 0x07c
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_UART3_S_RST_N	RW	UART3 interface soft reset, active low Value After Reset: 0x1
[0]	SW_UART3_PRST_N	RW	UART3 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.25 UART4_SWRST

- Description: UART4 soft reset configuration register
- Offset: 0x080
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_UART4_S_RST_N	RW	UART4 interface soft reset, active low

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[0]	SW_UART4_PRST_N	RW	UART4 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.26 UART5_SWRST

- Description: UART5 soft reset configuration register
- Offset: 0x084
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_UART5_S_RST_N	RW	UART5 interface soft reset, active low Value After Reset: 0x1
[0]	SW_UART5_PRST_N	RW	UART5 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.27 QSPI0_SWRST

- Description: QSPI0 soft reset configuration register
- Offset: 0x08c
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_QSPI0_PRST_N	RW	QSPI0 APB soft reset, active low Value After Reset: 0x1
[0]	SW_QSPI0_SSI_RST_N	RW	QSPI0 interface soft reset, active low Value After Reset: 0x1

5.4.2.2.28 QSPI1_SWRST

- Description: QSPI1 soft reset configuration register
- Offset: 0x090
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_QSPI1_PRST_N	RW	QSPI1 APB soft reset, active low

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[0]	SW_QSPI1_SSI_RST_N	RW	QSPI1 interface soft reset, active low Value After Reset: 0x1

5.4.2.2.29 SPI_SWRST

- Description: SPI soft reset configuration register
- Offset: 0x094
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_SPI_PRST_N	RW	SPI APB soft reset, active low Value After Reset: 0x1
[0]	SW_SPI_SSI_RST_N	RW	SPI1 interface soft reset, active low Value After Reset: 0x1

5.4.2.2.30 I2C0_SWRST

- Description: I2C0 soft reset configuration register
- Offset: 0x098
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_I2C0_IC_RST_N	RW	I2C0 core soft reset, active low Value After Reset: 0x1
[0]	SW_I2C0_PRST_N	RW	I2C0 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.31 I2C1_SWRST

- Description: I2C1 soft reset configuration register
- Offset: 0x09c
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_I2C1_IC_RST_N	RW	I2C1 core soft reset, active low

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[0]	SW_I2C1_PRST_N	RW	I2C1 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.32 I2C2_SWRST

- Description: I2C2 soft reset configuration register
- Offset: 0x0a0
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_I2C2_IC_RST_N	RW	I2C2 core soft reset, active low Value After Reset: 0x1
[0]	SW_I2C2_PRST_N	RW	I2C2 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.33 I2C3_SWRST

- Description: I2C3 soft reset configuration register
- Offset: 0x0a4
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_I2C3_IC_RST_N	RW	I2C3 core soft reset, active low Value After Reset: 0x1
[0]	SW_I2C3_PRST_N	RW	I2C3 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.34 I2C4_SWRST

- Description: I2C4 soft reset configuration register
- Offset: 0x0a8
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_I2C4_IC_RST_N	RW	I2C4 core soft reset, active low

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[0]	SW_I2C4_PRST_N	RW	I2C4 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.35 I2C5_SWRST

- Description: I2C5 soft reset configuration register
- Offset: 0x0ac
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_I2C5_IC_RST_N	RW	I2C5 core soft reset, active low Value After Reset: 0x1
[0]	SW_I2C5_PRST_N	RW	I2C5 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.36 GPIO0_SWRST

- Description: GPIO0 soft reset configuration register
- Offset: 0x0b0
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_GPIO0_PRST_N	RW	GPIO0 APB soft reset, active low Value After Reset: 0x1
[0]	SW_GPIO0_DBRST_N	RW	GPIO0 debounce soft reset, active low Value After Reset: 0x1

5.4.2.2.37 GPIO1_SWRST

- Description: GPIO1 soft reset configuration register
- Offset: 0x0b4
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_GPIO1_PRST_N	RW	GPIO1 APB soft reset, active low

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[0]	SW_GPIO1_DBRST_N	RW	GPIO1 debounce soft reset, active low Value After Reset: 0x1

5.4.2.2.38 GPIO2_SWRST

- Description: GPIO2 soft reset configuration register
- Offset: 0x0b8
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_GPIO2_PRST_N	RW	GPIO2 APB soft reset, active low Value After Reset: 0x1
[0]	SW_GPIO2_DBRST_N	RW	GPIO2 debounce soft reset, active low Value After Reset: 0x1

5.4.2.2.39 PWM_SWRST

- Description: PWM soft reset configuration register
- Offset: 0x0c0
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_PWM_PRST_N	RW	PWM APB soft reset, active low Value After Reset: 0x1
[0]	SW_PWM_CRST_N	RW	PWM counter soft reset, active low Value After Reset: 0x1

5.4.2.2.40 PADCTRL0_APSYS_SWRST

- Description: PADCTRL_APSYS soft reset configuration register
- Offset: 0x0c4
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_PADCTRL0_APSYS_PRST_N	RW	PADCTRL_APSYS APB soft reset, active low

Bits	Field Name	Access	Description
			Value After Reset: 0x1

5.4.2.2.41 CPU2PERI_X2H_SWRST

- Description: CPU2PERI_X2H soft reset configuration register
- Offset: 0x0cc
- Default Value: 0x2

Bits	Field Name	Access	Description
[31:2]	RESERVED_2	-	
[1]	SW_CPU2PERI_X2H_RST_N	RW	CPU2PERI_X2H soft reset, active low Value After Reset: 0x1
[0]	RESERVED_1	-	

5.4.2.2.42 AXI4_CFG_BUS_SWRST

- Description: AXI4_CFG_BUS soft reset configuration register
- Offset: 0x0d4
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_AXI4_CFG_BUS_ARST_N	RW	Reserved, software can't write it. Value After Reset: 0x1

5.4.2.2.43 CPU2CFG_X2H_SWRST

- Description: CPU2CFG_X2H soft reset configuration register
- Offset: 0x0d8
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_CPU2CFG_X2H_RST_N	RW	Reserved, software can't write it. Value After Reset: 0x1
[0]	SW_CPU2CFG_APB_RST_N	RW	Reserved, software can't write it. Value After Reset: 0x1

5.4.2.2.44 CPU2CFG_X2X_SWRST

- Description: CPU2CFG_X2X soft reset configuration register
- Offset: 0x0dc
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_CPU2CFG_X2X_ARST_N	RW	Reserved, software can't write it. Value After Reset: 0x1

5.4.2.2.45 CPU2AON_X2H_SWRST

- Description: CPU2AON_X2H soft reset configuration register
- Offset: 0x0e4
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_CPU2AON_X2H_RST_N	RW	CPU2AON_X2H soft reset, active low Value After Reset: 0x1

5.4.2.2.46 AXI4_CPUSYS1_SWRST

- Description: AXI4_CPUSYS1 soft reset configuration register
- Offset: 0x0f8
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_AXI4_CPUSYS1_PRST_N	RW	Reserved, software can't write it. Value After Reset: 0x1
[0]	SW_AXI4_CPUSYS1_ARST_N	RW	Reserved, software can't write it. Value After Reset: 0x1

5.4.2.2.47 AON2CPU_A2X_SWRST

- Description: AON2CPU_A2X soft reset configuration register
- Offset: 0x0fc
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_AON2CPU_A2X_HRST_N	RW	AON2CPU_A2X soft reset, active low Value After Reset: 0x1

5.4.2.2.48 RESERVED_REG_1

- Description: Reserved
- Offset: 0x100
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_1	RW	Reserved Value After Reset: 0x0

5.4.2.2.49 RESERVED_REG_2

- Description: Reserved
- Offset: 0x104
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_2	RW	Reserved Value After Reset: 0x0

5.4.2.2.50 RESERVED_REG_3

- Description: Reserved
- Offset: 0x108
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_3	RW	Reserved Value After Reset: 0x0

5.4.2.2.51 RESERVED_REG_4

- Description: Reserved
- Offset: 0x10c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_4	RW	Reserved Value After Reset: 0x0

5.4.2.2.52 NPUSYS_AXI_SWRST

- Description: NPUSYS_AXI soft reset configuration register
- Offset: 0x128
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_NPUSYS_AXI_PRST_N	RW	NPUSYS_AXI APB soft reset, active low Value After Reset: 0x1
[0]	SW_NPUSYS_AXI_ARST_N	RW	NPUSYS_AXI AXI soft reset, active low Value After Reset: 0x1

5.4.2.2.53 CPU2VP_X2P_SWRST

- Description: CPU2VP_X2P soft reset configuration register
- Offset: 0x12c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_CPU2VP_X2P_RST_N	RW	CPU2VP_X2P soft reset, active low Value After Reset: 0x1

5.4.2.2.54 CPU2VI_X2H_SWRST

- Description: CPU2VI_X2H soft reset configuration register
- Offset: 0x138
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_CPU2VI_X2H_RST_N	RW	CPU2VI_X2H soft reset, active low Value After Reset: 0x1

5.4.2.2.55 BMU_C910_SWRST

- Description: BMU_C910 soft reset configuration register
- Offset: 0x148
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_BMU_C910_PRST_N	RW	BMU_C910 AHB soft reset, active low. sw_bmu_c910_arst_n should be asserted before sw_bmu_c910_prst_n, and be deasserted after sw_chip_dbg_crst_n. Value After Reset: 0x1
[0]	SW_BMU_C910_ARST_N	RW	BMU_C910 AXI soft reset, active low. sw_bmu_c910_arst_n should be asserted before sw_bmu_c910_prst_n, and be deasserted after sw_chip_dbg_crst_n. Value After Reset: 0x1

5.4.2.2.56 DMAC_CPUSYS_SWRST

- Description: DMAC_CPUSYS soft reset configuration register
- Offset: 0x14c
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_DMAC_CPUSYS_HRST_N	RW	DMAC_CPUSYS AHB soft reset, active low Value After Reset: 0x1
[0]	SW_DMAC_CPUSYS_ARST_N	RW	DMAC_CPUSYS AXI soft reset, active low Value After Reset: 0x1

5.4.2.2.57 SPINLOCK_SWRST

- Description: SPINLOCK soft reset configuration register
- Offset: 0x178
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_SPINLOCK_HRST_N	RW	SPINLOCK soft reset, active low

Bits	Field Name	Access	Description
			Value After Reset: 0x1

5.4.2.2.58 CFG2TEE_X2H_SWRST

- Description: CFG2TEE_X2H soft reset configuration register
- Offset: 0x188
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_CFG2TEE_X2H_RST_N	RW	CFG2TEE_X2H soft reset, active low Value After Reset: 0x1

5.4.2.2.59 DSMART_SWRST

- Description: DSMART soft reset configuration register
- Offset: 0x18c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_DSMART_PRST_N	RW	DSMART soft reset, active low Value After Reset: 0x1

5.4.2.2.60 GPIO3_SWRST

- Description: GPIO3 soft reset configuration register
- Offset: 0x1a8
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_GPIO3_PRST_N	RW	GPIO3 APB soft reset, active low Value After Reset: 0x1
[0]	SW_GPIO3_DBRST_N	RW	GPIO3 debounce soft reset, active low Value After Reset: 0x1

5.4.2.2.61 I2S_SWRST

- Description: I2S soft reset configuration register
- Offset: 0x1ac

- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_I2S_PRST_N	RW	PERI I2S soft reset, active low Value After Reset: 0x1

5.4.2.2.62 IMG_NNA_SWRST

- Description: IMG_NNA soft reset configuration register
- Offset: 0x1b0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_IMG_NNA_RST_N	RW	IMG_NNA soft reset, active low Value After Reset: 0x0

5.4.2.2.63 PERI_APB3_SWRST

- Description: PERI_APB3 soft reset configuration register
- Offset: 0x1dc
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_PERI2PERI1_APB_PRST_N	RW	PERI2PERI1_APB soft reset, active low Value After Reset: 0x1
[0]	SW_PERI_APB3_HRST_N	RW	PERI_APB3 soft reset, active low Value After Reset: 0x1

5.4.2.2.64 VP_SUBSYS_SWRST

- Description: VP_SUBSYS soft reset configuration register
- Offset: 0x1ec
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_VP_SUBSYS_PRST_N	RW	VP_SUBSYS APB soft reset, active low Value After Reset: 0x1

5.4.2.2.65 PERISYS_APB4_SWRST

- Description: PERISYS_APB4 soft reset configuration register
- Offset: 0x1f8
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_PERISYS_APB4_HRST_N	RW	PERISYS_APB4 soft reset, active low Value After Reset: 0x1

5.4.2.2.66 GMAC1_SWRST

- Description: GMAC1 soft reset configuration register
- Offset: 0x204
- Default Value: 0xf

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	SW_GMAC1_ARST_N	RW	GMAC1 AXI soft reset, active low Value After Reset: 0x1
[2]	SW_GMAC1_GRST_N	RW	GMAC1 CLKGEN soft reset, active low Value After Reset: 0x1
[1]	SW_GMAC1_HRST_N	RW	GMAC1 AHB soft reset, active low Value After Reset: 0x1
[0]	SW_GMAC1_PRST_N	RW	GMAC1 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.67 GMAC_AXI_SWRST

- Description: GMAC_AXI soft reset configuration register
- Offset: 0x208
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_GMAC_AXI_PRST_N	RW	GMAC_AXI APB soft reset, active low Value After Reset: 0x1
[0]	SW_GMAC_AXI_ARST_N	RW	GMAC_AXI AXI soft reset, active low

Bits	Field Name	Access	Description
			Value After Reset: 0x1

5.4.2.2.68 PADCTRL1_APSYS_SWRST

- Description: PADCTRL1_APSYS soft reset configuration register
- Offset: 0x20c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_PADCTRL1_APSYS_PRST_N	RW	PADCTRL1_APSYS APB soft reset, active low Value After Reset: 0x1

5.4.2.2.69 VOSYS_AXI_SWRST

- Description: VOSYS_AXI soft reset configuration register
- Offset: 0x210
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_VOSYS_AXI_PRST_N	RW	VOSYS_AXI APB soft reset, active low Value After Reset: 0x1
[0]	SW_VOSYS_AXI_ARST_N	RW	VOSYS_AXI AXI soft reset, active low Value After Reset: 0x1

5.4.2.2.70 VOSYS_X2X_SWRST

- Description: VOSYS_X2X soft reset configuration register
- Offset: 0x214
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_VOBUS2NPUBUS_X2X_ARST_N	RW	VOSYS_X2X AXI soft reset, active low Value After Reset: 0x1

5.4.2.2.71 MISC2VP_X2X_SWRST

- Description: MISC2VP_X2X soft reset configuration register
- Offset: 0x218

- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_MISC2VP_X2X_ARST_N	RW	MISC2VP_X2X AXI soft reset, active low Value After Reset: 0x1

5.4.2.2.72 SUBSYS_SWRST

- Description: SUBSYS soft reset configuration register
- Offset: 0x220
- Default Value: 0x8

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	VP_SUBSYS_RST_N	RW	VP_SUBSYS soft reset, active low Value After Reset: 0x1
[2]	VO_SUBSYS_RST_N	RW	VO_SUBSYS soft reset, active low Value After Reset: 0x0
[1]	VI_SUBSYS_RST_N	RW	VI_SUBSYS soft reset, active low Value After Reset: 0x0
[0]	DSP_SUBSYS_RST_N	RW	DSP_SUBSYS soft reset, active low Value After Reset: 0x0

5.4.2.2.73 C910_BROM_TEESWRST

- Description: C910_BROM soft reset configuration register
- Offset: 0x1000
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_C910_BROM_HRST_N	RW	C910_BROM soft reset, active low Value After Reset: 0x1

5.4.2.2.74 C910_TEESWRST

- Description: C910 soft reset configuration register
- Offset: 0x1004
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	SW_C910_CORE3_RST_N	RW	C910 core3 soft reset, active low. Value After Reset: 0x0
[3]	SW_C910_CORE2_RST_N	RW	C910 core2 soft reset, active low Value After Reset: 0x0
[2]	SW_C910_CORE1_RST_N	RW	C910 core1 soft reset, active low Value After Reset: 0x0
[1]	SW_C910_CORE0_RST_N	RW	C910 core0 soft reset, active low Value After Reset: 0x1
[0]	SW_C910_RST_N	RW	C910 top soft reset, active low Value After Reset: 0x1

5.4.2.2.75 C910_DS_TEESWRST

- Description: C910 DS soft reset configuration register
- Offset: 0x1008
- Default Value: 0x1f

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	SW_C910_TOP_DS_PRST_N	RW	C910 top DS soft reset, active low Value After Reset: 0x1
[3]	SW_C910_TOP_CORE3_DS_RST_N	RW	C910 core3 DS soft reset, active low Value After Reset: 0x1
[2]	SW_C910_TOP_CORE2_DS_RST_N	RW	C910 core2 DS soft reset, active low Value After Reset: 0x1
[1]	SW_C910_TOP_CORE1_DS_RST_N	RW	C910 core1 DS soft reset, active low Value After Reset: 0x1
[0]	SW_C910_TOP_CORE0_DS_RST_N	RW	C910 core0 DS soft reset, active low Value After Reset: 0x1

5.4.2.2.76 CHIP_DBG_TEESWRST

- Description: CHIP_DBG soft reset configuration register
- Offset: 0x100c
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_CHIP_DBG_ARST_N	RW	CHIP_DBG AXI soft reset, active low. sw_chip_dbg_arst_n should be asserted before sw_chip_dbg_crst_n, and be deasserted after sw_chip_dbg_crst_n. Value After Reset: 0x1
[0]	SW_CHIP_DBG_CRST_N	RW	CHIP_DBG core soft reset, active low. sw_chip_dbg_arst_n should be asserted before sw_chip_dbg_crst_n, and be deasserted after sw_chip_dbg_crst_n. Value After Reset: 0x1

5.4.2.2.77 AXI4_CPUSYS2_TEESWRST

- Description: AXI4_CPUSYS2 soft reset configuration register
- Offset: 0x1010
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_AXI4_CPUSYS2_PRST_N	RW	AXI4_CPUSYS2 APB soft reset, active low Value After Reset: 0x1
[0]	SW_AXI4_CPUSYS2_ARST_N	RW	AXI4_CPUSYS2 AXI soft reset, active low Value After Reset: 0x1

5.4.2.2.78 X2X_CPUSYS_TEESWRST

- Description: X2X_CPUSYS soft reset configuration register
- Offset: 0x1014
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_X2X_CPUSYS_RST_N	RW	Reserved, software can't write it. Value After Reset: 0x1

5.4.2.2.79 X2H_CPUSYS_TEESWRST

- Description: X2H_CPUSYS soft reset configuration register
- Offset: 0x1018

- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_X2H_CPUSYS_RST_N	RW	X2H_CPUSYS soft reset, active low Value After Reset: 0x1

5.4.2.2.80 AHB2_CPUSYS_TEESWRST

- Description: AHB2_CPUSYS soft reset configuration register
- Offset: 0x101c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_AHB2_CPUSYS_HRST_N	RW	AHB2_CPUSYS AHB soft reset, active low Value After Reset: 0x1

5.4.2.2.81 APB3_CPUSYS_TEESWRST

- Description: APB3_CPUSYS soft reset configuration register
- Offset: 0x1020
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_APB3_CPUSYS_HRST_N	RW	APB3_CPUSYS APB soft reset, active low Value After Reset: 0x1

5.4.2.2.82 MBOX0_TEESWRST

- Description: MBOX0 soft reset configuration register
- Offset: 0x1024
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_MBOX0_PRST_N	RW	MBOX0 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.83 MBOX1_TEESWRST

- Description: MBOX1 soft reset configuration register
- Offset: 0x1028
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_MBOX1_PRST_N	RW	MBOX1 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.84 MBOX2_TEESWRST

- Description: MBOX2 soft reset configuration register
- Offset: 0x102c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_MBOX2_PRST_N	RW	MBOX2 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.85 MBOX3_TEESWRST

- Description: MBOX3 soft reset configuration register
- Offset: 0x1030
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_MBOX3_PRST_N	RW	MBOX3 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.86 WDT0_TEESWRST

- Description: WDT0 soft reset configuration register
- Offset: 0x1034
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_WDT0_PRST_N	RW	WDT0 APB soft reset, active low

Bits	Field Name	Access	Description
			Value After Reset: 0x1

5.4.2.2.87 WDT1_TEESWRST

- Description: WDT1 soft reset configuration register
- Offset: 0x1038
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_WDT1_PRST_N	RW	WDT1 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.88 TIMER0_TEESWRST

- Description: TIMER0 soft reset configuration register
- Offset: 0x103c
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_TIMER0_CRST_N	RW	Timer0 core soft reset, active low Value After Reset: 0x1
[0]	SW_TIMER0_PRST_N	RW	Timer0 APB bus soft reset, active low Value After Reset: 0x1

5.4.2.2.89 TIMER1_TEESWRST

- Description: TIMER1 soft reset configuration register
- Offset: 0x1040
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_TIMER1_CRST_N	RW	Timer1 core soft reset, active low Value After Reset: 0x1
[0]	SW_TIMER1_PRST_N	RW	Timer1 APB bus soft reset, active low Value After Reset: 0x1

5.4.2.2.90 PERISYS_AHB_TEESWRST

- Description: PERISYS_AHB soft reset configuration register
- Offset: 0x1044
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_PERISYS_AHB_HRST_N	RW	PERISYS_AHB soft reset, active low Value After Reset: 0x1

5.4.2.2.91 PERISYS_APB1_TEESWRST

- Description: PERISYS_APB1 soft reset configuration register
- Offset: 0x1048
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_PERISYS_APB1_HRST_N	RW	PERISYS_APB1 soft reset, active low Value After Reset: 0x1

5.4.2.2.92 PERISYS_APB2_TEESWRST

- Description: PERISYS_APB2 soft reset configuration register
- Offset: 0x104c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_PERISYS_APB2_HRST_N	RW	PERISYS_APB2 soft reset, active low Value After Reset: 0x1

5.4.2.2.93 GMAC0_TEESWRST

- Description: GAMC soft reset configuration register
- Offset: 0x1068
- Default Value: 0xf

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	SW_GMAC0_ARST_N	RW	GMAC AXI soft reset, active low

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[2]	SW_GMAC0_GRST_N	RW	GMAC CLKGEN soft reset, active low Value After Reset: 0x1
[1]	SW_GMAC0_HRST_N	RW	GMAC AHB soft reset, active low Value After Reset: 0x1
[0]	SW_GMAC0_PRST_N	RW	GMAC APB's soft reset, active low Value After Reset: 0x1

5.4.2.2.94 UART0_TEESWRST

- Description: UART0 soft reset configuration register
- Offset: 0x1070
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_UART0_S_RST_N	RW	UART0 interface soft reset, active low Value After Reset: 0x1
[0]	SW_UART0_PRST_N	RW	UART0 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.95 UART1_TEESWRST

- Description: UART1 soft reset configuration register
- Offset: 0x1074
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_UART1_S_RST_N	RW	UART1 interface soft reset, active low Value After Reset: 0x1
[0]	SW_UART1_PRST_N	RW	UART1 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.96 UART2_TEESWRST

- Description: UART2 soft reset configuration register
- Offset: 0x1078

- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_UART2_S_RST_N	RW	UART2 interface soft reset, active low Value After Reset: 0x1
[0]	SW_UART2_PRST_N	RW	UART2 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.97 UART3_TEESWRST

- Description: UART3 soft reset configuration register
- Offset: 0x107c
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_UART3_S_RST_N	RW	UART3 interface soft reset, active low Value After Reset: 0x1
[0]	SW_UART3_PRST_N	RW	UART3 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.98 UART4_TEESWRST

- Description: UART4 soft reset configuration register
- Offset: 0x1080
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_UART4_S_RST_N	RW	UART4 interface soft reset, active low Value After Reset: 0x1
[0]	SW_UART4_PRST_N	RW	UART4 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.99 UART5_TEESWRST

- Description: UART5 soft reset configuration register
- Offset: 0x1084
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_UART5_S_RST_N	RW	UART5 interface soft reset, active low Value After Reset: 0x1
[0]	SW_UART5_PRST_N	RW	UART5 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.100 QSPI0_TEESWRST

- Description: QSPI0 soft reset configuration register
- Offset: 0x108c
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_QSPI0_PRST_N	RW	QSPI0 APB soft reset, active low Value After Reset: 0x1
[0]	SW_QSPI0_SSI_RST_N	RW	QSPI0 interface soft reset, active low Value After Reset: 0x1

5.4.2.2.101 QSPI1_TEESWRST

- Description: QSPI1 soft reset configuration register
- Offset: 0x1090
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_QSPI1_PRST_N	RW	QSPI1 APB soft reset, active low Value After Reset: 0x1
[0]	SW_QSPI1_SSI_RST_N	RW	QSPI1 interface soft reset, active low Value After Reset: 0x1

5.4.2.2.102 SPI_TEESWRST

- Description: SPI soft reset configuration register
- Offset: 0x1094
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_SPI_PRST_N	RW	SPI APB soft reset, active low Value After Reset: 0x1
[0]	SW_SPI_SSI_RST_N	RW	SPI1 interface soft reset, active low Value After Reset: 0x1

5.4.2.2.103 I2C0_TEESWRST

- Description: I2C0 soft reset configuration register
- Offset: 0x1098
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_I2C0_IC_RST_N	RW	I2C0 core soft reset, active low Value After Reset: 0x1
[0]	SW_I2C0_PRST_N	RW	I2C0 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.104 I2C1_TEESWRST

- Description: I2C1 soft reset configuration register
- Offset: 0x109c
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_I2C1_IC_RST_N	RW	I2C1 core soft reset, active low Value After Reset: 0x1
[0]	SW_I2C1_PRST_N	RW	I2C1 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.105 I2C2_TEESWRST

- Description: I2C2 soft reset configuration register
- Offset: 0x10a0
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_I2C2_IC_RST_N	RW	I2C2 core soft reset, active low Value After Reset: 0x1
[0]	SW_I2C2_PRST_N	RW	I2C2 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.106 I2C3_TEESWRST

- Description: I2C3 soft reset configuration register
- Offset: 0x10a4
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_I2C3_IC_RST_N	RW	I2C3 core soft reset, active low Value After Reset: 0x1
[0]	SW_I2C3_PRST_N	RW	I2C3 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.107 I2C4_TEESWRST

- Description: I2C4 soft reset configuration register
- Offset: 0x10a8
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_I2C4_IC_RST_N	RW	I2C4 core soft reset, active low Value After Reset: 0x1
[0]	SW_I2C4_PRST_N	RW	I2C4 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.108 I2C5_TEESWRST

- Description: I2C5 soft reset configuration register
- Offset: 0x10ac
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_I2C5_IC_RST_N	RW	I2C5 core soft reset, active low Value After Reset: 0x1
[0]	SW_I2C5_PRST_N	RW	I2C5 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.109 GPIO0_TEESWRST

- Description: GPIO0 soft reset configuration register
- Offset: 0x10b0
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_GPIO0_PRST_N	RW	GPIO0 APB soft reset, active low Value After Reset: 0x1
[0]	SW_GPIO0_DBRST_N	RW	GPIO0 debounce soft reset, active low Value After Reset: 0x1

5.4.2.2.110 GPIO1_TEESWRST

- Description: GPIO1 soft reset configuration register
- Offset: 0x10b4
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_GPIO1_PRST_N	RW	GPIO1 APB soft reset, active low Value After Reset: 0x1
[0]	SW_GPIO1_DBRST_N	RW	GPIO1 debounce soft reset, active low Value After Reset: 0x1

5.4.2.2.111 GPIO2_TEESWRST

- Description: GPIO2 soft reset configuration register
- Offset: 0x10b8
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_GPIO2_PRST_N	RW	GPIO2 APB soft reset, active low Value After Reset: 0x1
[0]	SW_GPIO2_DBRST_N	RW	GPIO2 debounce soft reset, active low Value After Reset: 0x1

5.4.2.2.112 PWM_TEESWRST

- Description: PWM soft reset configuration register
- Offset: 0x10c0
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_PWM_PRST_N	RW	PWM APB soft reset, active low Value After Reset: 0x1
[0]	SW_PWM_CRST_N	RW	PWM counter soft reset, active low Value After Reset: 0x1

5.4.2.2.113 PADCTRL0_APSYS_TEESWRST

- Description: PADCTRL_APSYS soft reset configuration register
- Offset: 0x10c4
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_PADCTRL0_APSYS_PRST_N	RW	PADCTRL_APSYS APB soft reset, active low Value After Reset: 0x1

5.4.2.2.114 CPU2PERI_X2H_TEESWRST

- Description: CPU2PERI_X2H soft reset configuration register
- Offset: 0x10cc
- Default Value: 0x2

Bits	Field Name	Access	Description
[31:2]	RESERVED_2	-	
[1]	SW_CPU2PERI_X2H_RST_N	RW	CPU2PERI_X2H soft reset, active low Value After Reset: 0x1
[0]	RESERVED_1	-	

5.4.2.2.115 AXI4_CFG_BUS_TEESWRST

- Description: AXI4_CFG_BUS soft reset configuration register
- Offset: 0x10d4
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_AXI4_CFG_BUS_ARST_N	RW	Reserved, software can't write it. Value After Reset: 0x1

5.4.2.2.116 CPU2CFG_X2H_TEESWRST

- Description: CPU2CFG_X2H soft reset configuration register
- Offset: 0x10d8
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_CPU2CFG_X2H_RST_N	RW	Reserved, software can't write it. Value After Reset: 0x1
[0]	SW_CPU2CFG_APB_RST_N	RW	Reserved, software can't write it. Value After Reset: 0x1

5.4.2.2.117 CPU2CFG_X2X_TEESWRST

- Description: CPU2CFG_X2X soft reset configuration register
- Offset: 0x10dc
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_CPU2CFG_X2X_ARST_N	RW	Reserved, software can't write it. Value After Reset: 0x1

5.4.2.2.118 CPU2AON_X2H_TEESWRST

- Description: CPU2AON_X2H soft reset configuration register
- Offset: 0x10e4
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_CPU2AON_X2H_RST_N	RW	CPU2AON_X2H soft reset, active low Value After Reset: 0x1

5.4.2.2.119 AXI4_CPUSYS1_TEESWRST

- Description: AXI4_CPUSYS1 soft reset configuration register
- Offset: 0x10f8
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_AXI4_CPUSYS1_PRST_N	RW	Reserved, software can't write it. Value After Reset: 0x1
[0]	SW_AXI4_CPUSYS1_ARST_N	RW	Reserved, software can't write it. Value After Reset: 0x1

5.4.2.2.120 AON2CPU_A2X_TEESWRST

- Description: AON2CPU_A2X soft reset configuration register
- Offset: 0x10fc
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_AON2CPU_A2X_HRST_N	RW	AON2CPU_A2X soft reset, active low Value After Reset: 0x1

5.4.2.2.121 RESERVED_REG_1_TEE

- Description: Reserved
- Offset: 0x1100
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_1	RW	Reserved Value After Reset: 0x0

5.4.2.2.122 RESERVED_REG_2_TEE

- Description: Reserved
- Offset: 0x1104
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_2	RW	Reserved Value After Reset: 0x0

5.4.2.2.123 RESERVED_REG_3_TEE

- Description: Reserved
- Offset: 0x1108
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_3	RW	Reserved Value After Reset: 0x0

5.4.2.2.124 RESERVED_REG_4_TEE

- Description: Reserved
- Offset: 0x110c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_4	RW	Reserved Value After Reset: 0x0

5.4.2.2.125 NPUSYS_AXI_TEESWRST

- Description: NPUSYS_AXI soft reset configuration register
- Offset: 0x1128
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	

Bits	Field Name	Access	Description
[1]	SW_NPUSYS_AXI_PRST_N	RW	NPUSYS_AXI soft reset, active low Value After Reset: 0x1
[0]	SW_NPUSYS_AXI_ARST_N	RW	NPUSYS_AXI soft reset, active low Value After Reset: 0x1

5.4.2.2.126 CPU2VP_X2P_TEESWRST

- Description: CPU2VP_X2P soft reset configuration register
- Offset: 0x112c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_CPU2VP_X2P_RST_N	RW	CPU2VP_X2P soft reset, active low Value After Reset: 0x1

5.4.2.2.127 CPU2VI_X2H_TEESWRST

- Description: CPU2VI_X2H soft reset configuration register
- Offset: 0x1138
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_CPU2VI_X2H_RST_N	RW	CPU2VI_X2H soft reset, active low Value After Reset: 0x1

5.4.2.2.128 BMU_C910_TEESWRST

- Description: BMU_C910 soft reset configuration register
- Offset: 0x1148
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_BMU_C910_PRST_N	RW	BMU_C910 AHB soft reset, active low. sw_bmu_c910_arst_n should be asserted before sw_bmu_c910_prst_n, and be deasserted after sw_chip_dbg_crst_n. Value After Reset: 0x1

Bits	Field Name	Access	Description
[0]	SW_BMU_C910_ARST_N	RW	BMU_C910 AXI's soft reset, active low. sw_bmu_c910_arst_n should be asserted before sw_bmu_c910_prst_n, and be deasserted after sw_chip_dbg_crst_n. Value After Reset: 0x1

5.4.2.2.129 DMAC_CPUSYS_TEESWRST

- Description: DMAC_CPUSYS soft reset configuration register
- Offset: 0x114c
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_DMAC_CPUSYS_HRST_N	RW	DMAC_CPUSYS AHB soft reset, active low Value After Reset: 0x1
[0]	SW_DMAC_CPUSYS_ARST_N	RW	DMAC_CPUSYS AXI soft reset, active low Value After Reset: 0x1

5.4.2.2.130 SPINLOCK_TEESWRST

- Description: SPINLOCK soft reset configuration register
- Offset: 0x1178
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_SPINLOCK_HRST_N	RW	SPINLOCK soft reset, active low Value After Reset: 0x1

5.4.2.2.131 CFG2TEE_X2H_TEESWRST

- Description: CFG2TEE_X2H soft reset configuration register
- Offset: 0x1188
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_CFG2TEE_X2H_RST_N	RW	CFG2TEE_X2H soft reset, active low Value After Reset: 0x1

5.4.2.2.132 DSMART_TEESWRST

- Description: DSMART soft reset configuration register
- Offset: 0x118c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_DSMART_PRST_N	RW	DSMART soft reset, active low Value After Reset: 0x1

5.4.2.2.133 GPIO3_TEESWRST

- Description: GPIO3 soft reset configuration register
- Offset: 0x11a8
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_GPIO3_PRST_N	RW	GPIO3 APB soft reset, active low Value After Reset: 0x1
[0]	SW_GPIO3_DBRST_N	RW	GPIO3 debounce soft reset, active low Value After Reset: 0x1

5.4.2.2.134 I2S_TEESWRST

- Description: I2S soft reset configuration register
- Offset: 0x11ac
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_I2S_PRST_N	RW	PERI I2S soft reset, active low Value After Reset: 0x1

5.4.2.2.135 IMG_NNA_TEESWRST

- Description: IMG_NNA soft reset configuration register
- Offset: 0x11b0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_IMG_NNA_RST_N	RW	IMG_NNA soft reset, active low Value After Reset: 0x0

5.4.2.2.136 PERI_APB3_TEESWRST

- Description: PERI_APB3 soft reset configuration register
- Offset: 0x11dc
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_PERI2PERI1_APB_PRST_N	RW	PERI2PERI1_APB soft reset, active low Value After Reset: 0x1
[0]	SW_PERI_APB3_HRST_N	RW	PERI_APB3 soft reset, active low Value After Reset: 0x1

5.4.2.2.137 VP_SUBSYS_TEESWRST

- Description: VP_SUBSYS soft reset configuration register
- Offset: 0x11ec
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_VP_SUBSYS_PRST_N	RW	VP_SUBSYS APB soft reset, active low Value After Reset: 0x1

5.4.2.2.138 PERISYS_APB4_TEESWRST

- Description: PERISYS_APB4 soft reset configuration register
- Offset: 0x11f8
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_PERISYS_APB4_HRST_N	RW	PERISYS_APB4 soft reset, active low Value After Reset: 0x1

5.4.2.2.139 GMAC1_TEESWRST

- Description: GMAC1 soft reset configuration register
- Offset: 0x1204
- Default Value: 0xf

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	SW_GMAC1_ARST_N	RW	GMAC1 AXI soft reset, active low Value After Reset: 0x1
[2]	SW_GMAC1_GRST_N	RW	GMAC1 CLKGEN soft reset, active low Value After Reset: 0x1
[1]	SW_GMAC1_HRST_N	RW	GMAC1 AHB soft reset, active low Value After Reset: 0x1
[0]	SW_GMAC1_PRST_N	RW	GMAC1 APB soft reset, active low Value After Reset: 0x1

5.4.2.2.140 GMAC_AXI_TEESWRST

- Description: GMAC_AXI soft reset configuration register
- Offset: 0x1208
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_GMAC_AXI_ARST_N	RW	GMAC_AXI AXI soft reset, active low Value After Reset: 0x1

5.4.2.2.141 PADCTRL1_APSYS_TEESWRST

- Description: GMAC_APB soft reset configuration register
- Offset: 0x120c
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_GMAC_AXI_PRST_N	RW	PADCTRL1_APSYS APB soft reset, active low Value After Reset: 0x1
[0]	SW_PADCTRL1_APSYS_PRST_N	RW	GMAC_AXI APB soft reset, active low

Bits	Field Name	Access	Description
			Value After Reset: 0x1

5.4.2.2.142 VOSYS_AXI_TEESWRST

- Description: VOSYS_AXI soft reset configuration register
- Offset: 0x1210
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_VOSYS_AXI_PRST_N	RW	VOSYS_AXI APB soft reset, active low Value After Reset: 0x1
[0]	SW_VOSYS_AXI_ARST_N	RW	VOSYS_AXI AXI soft reset, active low Value After Reset: 0x1

5.4.2.2.143 VOSYS_X2X_TEESWRST

- Description: VOSYS_X2X soft reset configuration register
- Offset: 0x1214
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_VOBUS2NPUBUS_X2X_ARST_N	RW	VOSYS_X2X AXI soft reset, active low Value After Reset: 0x1

5.4.2.2.144 MISC2VP_X2X_TEESWRST

- Description: MISC2VP_X2X soft reset configuration register
- Offset: 0x1218
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_MISC2VP_X2X_ARST_N	RW	MISC2VP_X2X AXI soft reset, active low Value After Reset: 0x1

5.4.2.2.145 SUBSYS_TEESWRST

- Description: Subsystem soft reset configuration register
- Offset: 0x1220

- Default Value: 0x8

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	VP_SUBSYS_RST_N	RW	VP_SUBSYS soft reset, active low Value After Reset: 0x1
[2]	VO_SUBSYS_RST_N	RW	VO_SUBSYS soft reset, active low Value After Reset: 0x0
[1]	VI_SUBSYS_RST_N	RW	VI_SUBSYS soft reset, active low Value After Reset: 0x0
[0]	DSP_SUBSYS_RST_N	RW	DSP_SUBSYS soft reset, active low Value After Reset: 0x0

5.4.2.2.146 IOPMP_TEESWRST

- Description: IOPMP soft reset configuration register
- Offset: 0x1500
- Default Value: 0x100f00ff

Bits	Field Name	Access	Description
[31:29]	RESERVED_3	-	
[28]	SW_IOPMP_NPU_PRST_N	RW	IOPMP_NPU APB soft reset, active low. The IOPMP interrupt should be masked before reset. Value After Reset: 0x1
[27:20]	RESERVED_2	-	
[19]	SW_IOPMP_GMAC1_PRST_N	RW	IOPMP_GMAC1 APB soft reset, active low. The iOPMP interrupt should be masked before reset. Value After Reset: 0x1
[18]	SW_IOPMP_GMAC1_ARST_N	RW	IOPMP_GMAC1 AXI soft reset, active low. The IOPMP interrupt should be masked before reset. Value After Reset: 0x1
[17]	SW_IOPMP_GMAC0_PRST_N	RW	IOPMP_GMAC0 APB soft reset, active low. The IOPMP interrupt should be masked before reset. Value After Reset: 0x1
[16]	SW_IOPMP_GMAC0_ARST_N	RW	IOPMP_GMAC0 AXI soft reset, active low. The IOPMP interrupt should be masked before reset. Value After Reset: 0x1

Bits	Field Name	Access	Description
[15:8]	RESERVED_1	-	
[7]	SW_IOPMP_DMAC_CPUSYS_PRST_N	RW	IOPMP_DMAC_CPUSYS APB soft reset, active low. The IOPMP interrupt should be masked before reset. Value After Reset: 0x1
[6]	SW_IOPMP_DMAC_CPUSYS_ARST_N	RW	IOPMP_DMAC_CPUSYS AXI soft reset, active low. The IOPMP interrupt should be masked before reset. Value After Reset: 0x1
[5]	SW_IOPMP_CHIP_DBG_PRST_N	RW	IOPMP_CHIP_DBG APB soft reset, active low. The IOPMP interrupt should be masked before reset. Value After Reset: 0x1
[4]	SW_IOPMP_CHIP_DBG_ARST_N	RW	IOPMP_CHIP_DBG AXI soft reset, active low. The IOPMP interrupt should be masked before reset. Value After Reset: 0x1
[3]	SW_IOPMP_AUD_PRST_N	RW	iopmp_aud APB soft reset, active low. Value After Reset: 0x1
[2]	SW_IOPMP_AUD_ARST_N	RW	IOPMP_AUD AXI soft reset, active low. The IOPMP interrupt should be masked before reset. Value After Reset: 0x1
[1]	SW_IOPMP_AON_PRST_N	RW	IOPMP_AON APB soft reset, active low. Value After Reset: 0x1
[0]	SW_IOPMP_AON_ARST_N	RW	IOPMP_AON AXI soft reset, active low. The IOPMP interrupt should be masked before reset. Value After Reset: 0x1

5.4.2.2.147 RST_LOCK_0

- Description: Reset lock configuration register 0
- Offset: 0x1800
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	UART5_RST_LOCK	RW	UART5 REE soft reset write lock register Value After Reset: 0x0
[30]	UART4_RST_LOCK	RW	UART4 REE soft reset write lock register Value After Reset: 0x0
[29]	UART3_RST_LOCK	RW	UART3 REE soft reset write lock register

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[28]	UART2_RST_LOCK	RW	UART2 REE soft reset write lock register Value After Reset: 0x0
[27]	UART1_RST_LOCK	RW	UART1 REE soft reset write lock register Value After Reset: 0x0
[26]	UART0_RST_LOCK	RW	UART0 REE soft reset write lock register Value After Reset: 0x0
[25]	USB3_DRD_LOCK	RW	USB3_DRD REE soft reset write lock register Value After Reset: 0x0
[24]	GMAC0_RST_LOCK	RW	GMAC0 REE soft reset write lock register Value After Reset: 0x0
[23]	PERISYS_AXI_RST_LOCK	RW	PERISYS_AXI REE soft reset write lock register Value After Reset: 0x0
[22]	PERISYS_APB2_RST_LOCK	RW	PERISYS_APB2 REE soft reset write lock register Value After Reset: 0x0
[21]	PERISYS_APB1_RST_LOCK	RW	PERISYS_APB1 REE soft reset write lock register Value After Reset: 0x0
[20]	PERISYS_AHB_RST_LOCK	RW	PERISYS_AHB REE soft reset write lock register Value After Reset: 0x0
[19]	TIMER1_RST_LOCK	RW	Timer1 REE soft reset write lock register Value After Reset: 0x0
[18]	TIMER0_RST_LOCK	RW	Timer0 REE soft reset write lock register Value After Reset: 0x0
[17]	WDT1_RST_LOCK	RW	WDT1 REE soft reset write lock register Value After Reset: 0x0
[16]	WDT0_RST_LOCK	RW	WDT0 REE soft reset write lock register Value After Reset: 0x0
[15]	MBOX3_RST_LOCK	RW	MBOX3 REE soft reset write lock register Value After Reset: 0x0
[14]	MBOX2_RST_LOCK	RW	MBOX2 REE soft reset write lock register Value After Reset: 0x0
[13]	MBOX1_RST_LOCK	RW	MBOX1 REE soft reset write lock register

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[12]	MBOX0_RST_LOCK	RW	MBOX0 REE soft reset write lock register Value After Reset: 0x0
[11]	APB3_CPUSYS_RST_LOCK	RW	APB3_CPUSYS REE soft reset write lock register Value After Reset: 0x0
[10]	AHB2_CPUSYS_RST_LOCK	RW	AHB2_CPUSYS REE soft reset write lock register Value After Reset: 0x0
[9]	X2H_CPUSYS_RST_LOCK	RW	X2H_CPUSYS REE soft reset write lock register Value After Reset: 0x0
[8]	X2X_CPUSYS_RST_LOCK	RW	X2X_CPUSYS REE soft reset write lock register Value After Reset: 0x0
[7]	AXI4_CPUSYS2_RST_LOCK	RW	AXI4_CPUSYS2 REE soft reset write lock register Value After Reset: 0x0
[6]	CHIP_DBG_RST_LOCK	RW	CHIP_DBG REE soft reset write lock register Value After Reset: 0x0
[5]	C910_RST_LOCK	RW	C910 REE soft reset write lock register Value After Reset: 0x0
[4]	C910_CORE0_RST_LCOK	RW	C910_CORE0 REE soft reset write lock register Value After Reset: 0x0
[3]	C910_CORE1_RST_LCOK	RW	C910_CORE1 REE soft reset write lock register Value After Reset: 0x0
[2]	C910_CORE2_RST_LCOK	RW	C910_CORE2 REE soft reset write lock register Value After Reset: 0x0
[1]	C910_CORE3_RST_LCOK	RW	C910_CORE3 REE soft reset write lock register Value After Reset: 0x0
[0]	C910_BROM_RST_LOCK	RW	C910_BROM REE soft reset write lock register Value After Reset: 0x0

5.4.2.2.148 RST_LOCK_1

- Description: Reset lock configuration register 1
- Offset: 0x1804
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	VISYS_AXI_RST_LOCK	RW	VISYS_AXI REE soft reset write lock register Value After Reset: 0x0
[30]	RESERVED_4	-	
[29]	PERI2DDR_X2X_RST_LOCK	RW	PERI2DDR_X2X REE soft reset write lock register Value After Reset: 0x0
[28]	RESERVED_3	-	
[27]	RESERVED_REG_4_LOCK	RW	RESERVED_REG_4_LOCK Value After Reset: 0x0
[26]	RESERVED_REG_3_LOCK	RW	RESERVED_REG_3_LOCK Value After Reset: 0x0
[25]	RESERVED_REG_2_LOCK	RW	RESERVED_REG_2_LOCK Value After Reset: 0x0
[24]	RESERVED_REG_1_LOCK	RW	RESERVED_REG_1_LOCK Value After Reset: 0x0
[23]	AON2CPU_A2X_RST_LOCK	RW	AON2CPU_A2X REE soft reset write lock register Value After Reset: 0x0
[22]	AXI4_CPUSYS1_RST_LOCK	RW	AXI4_CPUSYS1 REE soft reset write lock register Value After Reset: 0x0
[21]	CPU2AON_X2H_RST_LOCK	RW	CPU2AON_X2H REE soft reset write lock register Value After Reset: 0x0
[20]	CPU2CFG_X2X_RST_LOCK	RW	CPU2CFG_X2X REE soft reset write lock register Value After Reset: 0x0
[19]	CPU2CFG_APB_RST_LOCK	RW	CPU2CFG_APB REE soft reset write lock register Value After Reset: 0x0
[18]	CPU2CFG_X2H_RST_LOCK	RW	CPU2CFG_X2H REE soft reset write lock register Value After Reset: 0x0
[17]	AXI4_CFG_BUS_RST_LOCK	RW	AXI4_CFG_BUS REE soft reset write lock register Value After Reset: 0x0
[16]	CPU2PERI_X2H_RST_LOCK	RW	CPU2PERI_X2H REE soft reset write lock register Value After Reset: 0x0
[15]	RESERVED_2	-	

Bits	Field Name	Access	Description
[14]	PADCTRL0_APSYS_RST_LOCK	RW	PADCTRL0_APSYS REE soft reset write lock register Value After Reset: 0x0
[13]	PWM_RST_LOCK	RW	PWM REE soft reset write lock register Value After Reset: 0x0
[12]	RESERVED_1	-	
[11]	GPIO2_RST_LOCK	RW	GPIO2 REE soft reset write lock register Value After Reset: 0x0
[10]	GPIO1_RST_LOCK	RW	GPIO1 REE soft reset write lock register Value After Reset: 0x0
[9]	GPIO0_RST_LOCK	RW	GPIO0 REE soft reset write lock register Value After Reset: 0x0
[8]	I2C5_RST_LOCK	RW	I2C5 REE soft reset write lock register Value After Reset: 0x0
[7]	I2C4_RST_LOCK	RW	I2C4 REE soft reset write lock register Value After Reset: 0x0
[6]	I2C3_RST_LOCK	RW	I2C3 REE soft reset write lock register Value After Reset: 0x0
[5]	I2C2_RST_LOCK	RW	I2C2 REE soft reset write lock register Value After Reset: 0x0
[4]	I2C1_RST_LOCK	RW	I2C1 REE soft reset write lock register Value After Reset: 0x0
[3]	I2C0_RST_LOCK	RW	I2C0 REE soft reset write lock register Value After Reset: 0x0
[2]	SPI_RST_LOCK	RW	SPI REE soft reset write lock register Value After Reset: 0x0
[1]	QSPI1_RST_LOCK	RW	QSPI1 REE soft reset write lock register Value After Reset: 0x0
[0]	QSPI0_RST_LOCK	RW	QSPI0 REE soft reset write lock register Value After Reset: 0x0

5.4.2.2.149 RST_LOCK_2

- Description: Reset lock configuration register 2

- Offset: 0x1808
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	IMG_NNA_RST_LOCK	RW	IMG_NNA REE soft reset write lock register Value After Reset: 0x0
[30]	I2S_RST_LOCK	RW	I2S REE soft reset write lock register Value After Reset: 0x0
[29]	GPIO3_RST_LOCK	RW	GPIO3 REE soft reset write lock register Value After Reset: 0x0
[28]	EMMC_X2X_RST_LOCK	RW	EMMC_X2X REE soft reset write lock register Value After Reset: 0x0
[27]	EMMC_RST_LOCK	RW	EMMC REE soft reset write lock register Value After Reset: 0x0
[26:23]	RESERVED_6	-	
[22]	DSMART_RST_LOCK	RW	DSMART REE soft reset write lock register Value After Reset: 0x0
[21]	CFG2TEE_X2H_RST_LOCK	RW	CFG2TEE_X2H REE soft reset write lock register Value After Reset: 0x0
[20:19]	RESERVED_5	-	
[18]	SPINLOCK_RST_LOCK	RW	SPINLOCK REE soft reset write lock register Value After Reset: 0x0
[17]	RESERVED_4	-	
[16]	SDIO1_RST_LOCK	RW	SDIO1 REE soft reset write lock register Value After Reset: 0x0
[15]	RESERVED_3	-	
[14]	SDIO0_RST_LOCK	RW	SDIO0 REE soft reset write lock register Value After Reset: 0x0
[13:8]	RESERVED_2	-	
[7]	DMAC_CPUSYS_RST_LOCK	RW	DMAC_CPUSYS REE soft reset write lock register Value After Reset: 0x0
[6]	BMU_C910_RST_LOCK	RW	BMU_C910 REE soft reset write lock register Value After Reset: 0x0

Bits	Field Name	Access	Description
[5]	NPU2SRAM_X2X_RST_LOCK	RW	NPU2SRAM_X2X REE soft reset write lock register Value After Reset: 0x0
[4]	TEE2DDR_X2X_RST_LOCK	RW	TEE2DDR_X2X REE soft reset write lock register Value After Reset: 0x0
[3]	CPU2VI_X2H_RST_LOCK	RW	CPU2VI_X2H REE soft reset write lock register Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	CPU2VP_X2P_RST_LOCK	RW	CPU2VP_X2P REE soft reset write lock register Value After Reset: 0x0
[0]	NPUSYS_AXI_RST_LOCK	RW	NPUSYS_AXI REE soft reset write lock register Value After Reset: 0x0

5.4.2.2.150 RST_LOCK_3

- Description: Reset lock configuration register 3
- Offset: 0x180c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:29]	RESERVED_6	-	
[28]	VOSYS_RST_LOCK	RW	VOSYS REE soft reset write lock register Value After Reset: 0x0
[27]	VISYS_RST_LOCK	RW	VISYS REE soft reset write lock register Value After Reset: 0x0
[26]	DSPSYS_RST_LOCK	RW	DSPSYS REE soft reset write lock register Value After Reset: 0x0
[25]	MISC2VP_X2X_ARST_LOCK	RW	MISC2VP_X2X reset write lock register Value After Reset: 0x0
[24]	VOSYS_AXI_ARST_LOCK	RW	VOSYS_AXI reset write lock register Value After Reset: 0x0
[23]	VOBUS2NPUBUS_X2X_ARST_LOCK	RW	VOBUS2NPUBUS_X2X reset write lock register Value After Reset: 0x0
[22]	GMAC_AXI_RST_LOCK	RW	GMAC_AXI REE soft reset write lock register Value After Reset: 0x0

Bits	Field Name	Access	Description
[21]	PADCTRL1_APSYS_RST_LOCK	RW	PADCTRL1_APSYS REE soft reset write lock register Value After Reset: 0x0
[20:19]	RESERVED_5	-	
[18]	GMAC1_RST_LOCK	RW	GMAC1 REE soft reset write lock register Value After Reset: 0x0
[17]	RESERVED_4	-	
[16]	PERISYS_APB4_LOCK	RW	PERISYS_APB4 write lock register Value After Reset: 0x0
[15]	RESERVED_3	-	
[14]	GPIO4_RST_LOCK	RW	GPIO4 REE soft reset write lock register Value After Reset: 0x0
[13]	VP_SUBSYS_RST_LOCK	RW	VP_SUBSYS REE soft reset write lock register Value After Reset: 0x0
[12:11]	RESERVED_2	-	
[10]	PERI2PERI1_APB_RST_LOCK	RW	PERI2PERI1_APB REE soft reset write lock register Value After Reset: 0x0
[9]	PERI_APB3_RST_LOCK	RW	PERI_APB3 REE soft reset write lock register Value After Reset: 0x0
[8:0]	RESERVED_1	-	

5.4.2.3 DDR_SUBSYS

5.4.2.3.1 DDR_CFG0

- Description: Misc configuration of DDR subsystem
- Offset: 0x0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RG_CTL_DDR_USW_RST_REG	RW	1: Exit/release reset 0: Enter reset [0]: APB sw reset [1]: CTRL sw reset [2]: PHY PwrOk sw reset [3]: PHY core sw reset

Bits	Field Name	Access	Description
			[4]: AXI port0 sw reset [5]: AXI port1 sw reset [6]: AXI port2 sw reset [7]: AXI port3 sw reset [8]: AXI port4 sw reset Others: Reserved Value After Reset: 0x0
[3:2]	RESERVED_1	-	
[1]	RG_DDRC_32EN	RW	0: 64bit mode ,PHY1/PHY0 clock should be free on. 1: 32bit mode, PHY1 clock will be gated. Value After Reset: 0x0
[0]	RG_BROADCAST_MODE	RW	0: Disable broadcast mode. 1: PHY1/PHY0 in broadcast mode, program to PHY0 will also apply to PHY1. Value After Reset: 0x0

5.4.2.4 MISC_SUBSYS

5.4.2.4.1 EMMC_SWRST

- Description: eMMC soft reset configuration register
- Offset: 0x0000
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_EMMC_RST_N	RW	eMMC soft reset, active low Value After Reset: 0x1
[0]	SW_EMMC_SDIO_CLKGEN_RST_N	RW	eMMC clock generator soft reset, active low Value After Reset: 0x1

5.4.2.4.2 MISCSYS_AXI_SWRST

- Description: MISCSYS AXI bus soft reset configuration register
- Offset: 0x0008
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_MISCSYS_AXI_PRST_N	RW	MISC SUBSYS AXI bus configuration port soft reset, active low Value After Reset: 0x1
[0]	SW_MISCSYS_AXI_ARST_N	RW	MISC SUBSYS AXI bus soft reset, active low Value After Reset: 0x1

5.4.2.4.3 SDIO0_SWRST

- Description: SDIO0 soft reset configuration register
- Offset: 0x000C
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_SDIO0_RST_N	RW	SDIO0 clock generator soft reset, active low Value After Reset: 0x1

5.4.2.4.4 SDIO1_SWRST

- Description: SDIO1 soft reset configuration register
- Offset: 0x0010
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_SDIO1_RST_N	RW	SDIO1 clock generator soft reset, active low Value After Reset: 0x1

5.4.2.4.5 USB3_DRD_SWRST

- Description: USB3_DRD soft reset configuration register
- Offset: 0x0014
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	SW_USB3_DRD_VCCRST_N	RW	USB3 VCC soft reset, active low Value After Reset: 0x0

Bits	Field Name	Access	Description
[1]	SW_USB3_DRD_PHYRST_N	RW	USB3 APB port reset, active low Value After Reset: 0x0
[0]	SW_USB3_DRD_PRST_N	RW	USB3 PHY soft reset, active low Value After Reset: 0x1

5.4.2.4.6 EMMC_SWRST_TEE

- Description: eMMC soft reset configuration register
- Offset: 0x1000
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_EMMC_RST_N	RW	eMMC soft reset, active low Value After Reset: 0x1
[0]	SW_EMMC_SDIO_CLKGEN_RST_N	RW	eMMC clock generator soft reset, active low Value After Reset: 0x1

5.4.2.4.7 MISCSYS_AXI_SWRST_TEE

- Description: MISCSYS AXI bus soft reset configuration register
- Offset: 0x1008
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_MISCSYS_AXI_PRST_N	RW	MISC SUBSYS AXI bus configuration port soft reset, active low Value After Reset: 0x1
[0]	SW_MISCSYS_AXI_ARST_N	RW	MISC SUBSYS AXI bus soft reset, active low Value After Reset: 0x1

5.4.2.4.8 SDIO0_SWRST_TEE

- Description: SDIO0 soft reset configuration register
- Offset: 0x100C
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_SDIO0_RST_N	RW	SDIO0 clock generator soft reset, active low Value After Reset: 0x1

5.4.2.4.9 SDIO1_SWRST_TEE

- Description: SDIO1 soft reset configuration register
- Offset: 0x1010
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_SDIO1_RST_N	RW	SDIO1 clock generator soft reset, active low Value After Reset: 0x1

5.4.2.4.10 USB3_DRD_SWRST_TEE

- Description: USB3_DRD soft reset configuration register
- Offset: 0x1014
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	SW_USB3_DRD_VCCRST_N	RW	USB3 VCC soft reset, active low Value After Reset: 0x0
[1]	SW_USB3_DRD_PHYRST_N	RW	USB3 APB port reset, active low Value After Reset: 0x0
[0]	SW_USB3_DRD_PRST_N	RW	USB3 PHY soft reset, active low Value After Reset: 0x1

5.4.2.4.11 TEESTS_AHB_TEESWRST_TEE

- Description: TEE subsystem AHB bus reset configuration register
- Offset: 0x1020
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_AHB2_TEESYS_HRST_N	RW	TEESYS AHB bus soft reset, active low

Bits	Field Name	Access	Description
			Value After Reset: 0x1

5.4.2.4.12 TEESTS_APB_TEESWRST_TEE

- Description: TEE subsystem APB bus reset configuration register
- Offset: 0x1024
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_APB3_TEESYS_HRST_N	RW	TEESYS APB bus soft reset, active low Value After Reset: 0x1

5.4.2.4.13 TEESTS_AXI_TEESWRST_TEE

- Description: TEE subsystem AXI bus reset configuration register
- Offset: 0x1028
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_AXI4_TEESYS_ARST_N	RW	TEESYS AXI bus soft reset, active low Value After Reset: 0x1

5.4.2.4.14 TEESYS_X2X_TEESWRST_TEE

- Description: TEE subsystem X2X bus reset configuration register
- Offset: 0x102c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_X2X_X4_TEESYS_128DW64_ARST_N	RW	TEESYS X2X bridge soft reset, active low Value After Reset: 0x1

5.4.2.4.15 TEESYS_REG_TEESWRST_TEE

- Description: TEE subsystem sysreg bus reset configuration register
- Offset: 0x1030
- Default Value: 0x4

Bits	Field Name	Access	Description
[31:3]	RESERVED_2	-	
[2]	SW_TEE_SYSREG_PRST_N	RW	TEEDMAC AXI soft reset, active low Value After Reset: 0x1
[1:0]	RESERVED_1	-	

5.4.2.4.16 TEEDMAC_TEESWRST_TEE

- Description: TEE subsystem DMA module reset configuration register
- Offset: 0x1034
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_TEE_DMAC_HRST_N	RW	TEEDMAC AHB soft reset, active low Value After Reset: 0x1
[0]	SW_TEE_DMAC_ARST_N	RW	TEEDMAC AXI soft reset, active low Value After Reset: 0x1

5.4.2.4.17 EFUSE_TEESWRST_TEE

- Description: TEE subsystem eFuse module reset configuration register
- Offset: 0x1038
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_EFUSE_PRST_N	RW	eFuse soft reset, active low Value After Reset: 0x1

5.4.2.4.18 EIP120SI_TEESWRST_TEE

- Description: TEE subsystem EIP120SI module reset configuration register
- Offset: 0x103C
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_EIP120SI_HRST_N	RW	EIP120SI_HRST soft reset, active low Value After Reset: 0x1

Bits	Field Name	Access	Description
[0]	SW_EIP120SI_ARST_N	RW	EIP120SI_ARST soft reset, active low Value After Reset: 0x1

5.4.2.4.19 EIP120SII_TEESWRST_TEE

- Description: TEE subsystem EIP120SII module reset configuration register
- Offset: 0x1040
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_EIP120SII_HRST_N	RW	EIP120SII_HRST soft reset, active low Value After Reset: 0x1
[0]	SW_EIP120SII_ARST_N	RW	EIP120SII_ARST soft reset, active low Value After Reset: 0x1

5.4.2.4.20 EIP120SIII_TEESWRST_TEE

- Description: TEE subsystem EIP120SIII module reset configuration register
- Offset: 0x1044
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_EIP120SIII_HRST_N	RW	EIP120SIII_HRST soft reset, active low Value After Reset: 0x1
[0]	SW_EIP120SIII_ARST_N	RW	EIP120SIII_ARST soft reset, active low Value After Reset: 0x1

5.4.2.4.21 EIP150B_TEESWRST_TEE

- Description: TEE subsystem EIP150B module reset configuration register
- Offset: 0x1048
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_EIP150B_HRST_N	RW	EIP150B_HRST soft reset, active low Value After Reset: 0x1

5.4.2.4.22 OCRAM_TEESWRST_TEE

- Description: TEE subsystem OCRAM module reset configuration register
- Offset: 0x104C
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_OCRAM_HRST_N	RW	OCRAM_HRST soft reset, active low Value After Reset: 0x1

5.4.2.4.23 IOPMP_TEESWRST_TEE

- Description: TEE subsystem IOPMP module reset configuration register
- Offset: 0x1050
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15]	SW_IOPMP_USB3_PRST_N	RW	IOPMP_USB3_PRST soft reset, active low Value After Reset: 0x1
[14]	SW_IOPMP_USB3_ARST_N	RW	IOPMP_USB3_ARST soft reset, active low Value After Reset: 0x1
[13]	SW_IOPMP_TEEDMAC_PRST_N	RW	IOPMP_TEEDMAC_PRST soft reset, active low Value After Reset: 0x1
[12]	SW_IOPMP_TEEDMAC_ARST_N	RW	IOPMP_TEEDMAC_ARST soft reset, active low Value After Reset: 0x1
[11]	SW_IOPMP_SDIO1_PRST_N	RW	IOPMP_SDIO1_PRST soft reset, active low Value After Reset: 0x1
[10]	SW_IOPMP_SDIO1_ARST_N	RW	IOPMP_SDIO1_ARST soft reset, active low Value After Reset: 0x1
[9]	SW_IOPMP_SDIO0_PRST_N	RW	IOPMP_SDIO0_PRST soft reset, active low Value After Reset: 0x1
[8]	SW_IOPMP_SDIO0_ARST_N	RW	IOPMP_SDIO0_ARST soft reset, active low Value After Reset: 0x1
[7]	SW_IOPMP_EMMC_PRST_N	RW	IOPMP_EMMC_PRST soft reset, active low Value After Reset: 0x1

Bits	Field Name	Access	Description
[6]	SW_IOPMP_EMMC_ARST_N	RW	IOPMP_EMMC_ARST soft reset, active low Value After Reset: 0x1
[5]	SW_IOPMP_EIP120SIII_PRST_N	RW	IOPMP_EIP120SIII_PRST soft reset, active low Value After Reset: 0x1
[4]	SW_IOPMP_EIP120SIII_ARST_N	RW	IOPMP_EIP120SIII_ARST soft reset, active low Value After Reset: 0x1
[3]	SW_IOPMP_EIP120SII_PRST_N	RW	IOPMP_EIP120SII_PRST soft reset, active low Value After Reset: 0x1
[2]	SW_IOPMP_EIP120SII_ARST_N	RW	IOPMP_EIP120SII_ARST soft reset, active low Value After Reset: 0x1
[1]	SW_IOPMP_EIP120SI_PRST_N	RW	IOPMP_EIP120SI_PRST soft reset, active low Value After Reset: 0x1
[0]	SW_IOPMP_EIP120SI_ARST_N	RW	IOPMP_EIP120SI_ARST soft reset, active low Value After Reset: 0x1

5.4.2.4.24 DS_TEESWRST_TEE

- Description: TEE subsystem DS module reset configuration register
- Offset: 0x1054
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_DS_PRST_N	RW	DS soft reset, active low Value After Reset: 0x1

5.4.2.4.25 KEYRAM_TEESWRST_TEE

- Description: TEE subsystem KEYRAM module reset configuration register
- Offset: 0x1058
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_KEYRAM_PRST_N	RW	KEYRAM APB soft reset, active low Value After Reset: 0x1

5.4.2.5 VI_SUBSYS

5.4.2.5.1 VISYS_SW_RST

- Description: VISYS_SW_RST1
- Offset: 0x100
- Default Value: 0xb1170011

Bits	Field Name	Access	Description
[31]	SW_DW200_SRST_N	RW	DW200 sw APB reset 0: resetn active Value After Reset: 0x1
[30]	RESERVED_6	-	
[29]	SW_VIPRE_ARSTN	RW	VIPRE sw AXI reset 0: resetn active Value After Reset: 0x1
[28]	SW_VIPRE_PRESETN	RW	VIPRE sw APB reset 0: resetn active Value After Reset: 0x1
[27:25]	RESERVED_5	-	
[24]	SW_ISP_VENC_SHAKE_PRESETN	RW	ISP_VENC_HANDSHAKE sw APB reset 0: resetn active Note: Reset flow please follow the description of sw_isp_venc_shake_arstn. Value After Reset: 0x1
[23:21]	RESERVED_4	-	
[20]	SW_MIPI_CSI2X2_FIFO_RSTZ	RW	MIPI FIFO CTRL reset Value After Reset: 0x1
[19]	RESERVED_3	-	
[18]	SW_MIPI_MIPI_CSI2X2_PRESETN_1	RW	MIPI_CSI2 sw APB reset 0: resetn active Value After Reset: 0x1
[17]	SW_MIPI_MIPI_CSI2X2_PRESETN_0	RW	MIPI_CSI1 sw APB reset 0: resetn active Value After Reset: 0x1
[16]	SW_MIPI_CSI2_PRESETN	RW	MIPI_CSI0 sw APB reset

Bits	Field Name	Access	Description
			0: resetn active Value After Reset: 0x1
[15:5]	RESERVED_2	-	
[4]	SW_ISP_RY_SRST_N	RW	ISP1 sw reset 0: resetn active Value After Reset: 0x1
[3:1]	RESERVED_1	-	
[0]	SW_ISP_SRST_N	RW	ISP0 sw reset 0: resetn active Value After Reset: 0x1

5.4.2.5.2 VISYS_SW_RST2

- Description: VISYS_SW_RST2
- Offset: 0x104
- Default Value: 0x111700

Bits	Field Name	Access	Description
[31:21]	RESERVED_5	-	
[20]	SW_ISP_VENC_SHAKE_ARSTN	RW	ISP_VENC_HANDSHAKE sw AXI reset 0: resetn active Note: Reset flow should follow the steps: 1. Reset sw_isp_venc_shake_arstn. 2. Reset sw_iopmp_vipre_presetn. 3. Release sw_isp_venc_shake_presetn. 4. Release sw_isp_venc_shake_arstn. Value After Reset: 0x1
[19:17]	RESERVED_4	-	
[16]	SW_VISYS_PRESETN	RW	VI subsystem sw APB reset 0: resetn active Value After Reset: 0x1
[15:13]	RESERVED_3	-	
[12]	SW_AXI4_VISYS_ARST_N	RW	VI subsystem sw AXI reset 0: resetn active Value After Reset: 0x1

Bits	Field Name	Access	Description
[11]	RESERVED_2	-	
[10]	SW_AXI4_VISYS1_ARST_N	RW	ISP0 bus sw AXI reset 0: resetn active Value After Reset: 0x1
[9]	SW_AXI4_VISYS2_ARST_N	RW	ISP1 bus AXI reset 0: resetn active Value After Reset: 0x1
[8]	SW_AXI4_VISYS3_ARST_N	RW	ISP_RY and DW200 sw AXI reset 0: resetn active Value After Reset: 0x1
[7:0]	RESERVED_1	-	

5.4.2.5.3 VISYS_SW_RST_TEE

- Description: VISYS_SW_RST1
- Offset: 0x1100
- Default Value: 0xb1170011

Bits	Field Name	Access	Description
[31]	SW_DW200_SRST_N	RW	DW200 sw APB reset 0: resetn active Value After Reset: 0x1
[30]	RESERVED_6	-	
[29]	SW_VIPRE_ARSTN	RW	VIPRE sw AXI reset 0: resetn active Value After Reset: 0x1
[28]	SW_VIPRE_PRESETN	RW	VIPRE sw APB reset 0: resetn active Value After Reset: 0x1
[27:25]	RESERVED_5	-	
[24]	SW_ISP_VENC_SHAKE_PRESETN	RW	ISP_VENC_HANDSHAKE sw APB reset 0: resetn active Note: Reset flow please follow the description of sw_isp_venc_shake_arstn. Value After Reset: 0x1

Bits	Field Name	Access	Description
[23:21]	RESERVED_4	-	
[20]	SW_MIPI_CSI2X2_FIFO_RSTZ	RW	MIPI FIFO CTRL reset Value After Reset: 0x1
[19]	RESERVED_3	-	
[18]	SW_MIPI_MIPI_CSI2X2_PRESETN_1	RW	MIPI_CSI2 sw APB reset 0: resetn active Value After Reset: 0x1
[17]	SW_MIPI_MIPI_CSI2X2_PRESETN_0	RW	MIPI_CSI1 sw APB reset 0: resetn active Value After Reset: 0x1
[16]	SW_MIPI_CSI2_PRESETN	RW	MIPI_CSI0 sw APB reset 0: resetn active Value After Reset: 0x1
[15:5]	RESERVED_2	-	
[4]	SW_ISP_RY_SRST_N	RW	ISP1 sw reset 0: resetn active Value After Reset: 0x1
[3:1]	RESERVED_1	-	
[0]	SW_ISP_SRST_N	RW	ISP0 sw reset 0: resetn active Value After Reset: 0x1

5.4.2.5.4 VISYS_SW_RST2_TEE

- Description: VISYS_SW_RST2
- Offset: 0x1104
- Default Value: 0xff111700

Bits	Field Name	Access	Description
[31]	SW_AXI4_IOPMP_VSI1_ARST_N	RW	ISP0 IOPMP sw AXI reset 0: resetn active Note: Need to mask IOPMP interrupt before active resetn. Value After Reset: 0x1
[30]	SW_AXI4_IOPMP_VSI2_ARST_N	RW	ISP1 IOPMP AXI reset

Bits	Field Name	Access	Description
			0: resetn active Note: Need to mask IOPMP interrupt before active resetn. Value After Reset: 0x1
[29]	SW_AXI4_IOPMP_VSI3_ARST_N	RW	ISP_RY and DW200 IOPMP sw AXI reset 0: resetn active Note: Need to mask IOPMP interrupt before active resetn. Value After Reset: 0x1
[28]	SW_AXI4_IOPMP_VIPRE_ARST_N	RW	VIPRE IOPMP AXI reset 0: resetn active Note: Need to mask IOPMP interrupt before active resetn. Value After Reset: 0x1
[27]	SW_IOPMP_VSI1_PRESETN	RW	ISP0 IOPMP sw APB reset 0: resetn active Note: Need to mask IOPMP interrupt before active resetn. Value After Reset: 0x1
[26]	SW_IOPMP_VSI2_PRESETN	RW	ISP1 IOPMP APB reset 0: resetn active Note: Need to mask IOPMP interrupt before active resetn. Value After Reset: 0x1
[25]	SW_IOPMP_VSI3_PRESETN	RW	ISP_RY and DW200 IOPMP sw APB reset Note: Need to mask IOPMP interrupt before active resetnpb reset. 0: resetn active Value After Reset: 0x1
[24]	SW_IOPMP_VIPRE_PRESETN	RW	VIPRE IOPMP APB reset 0: resetn active Note: Need to mask IOPMP interrupt before active resetn. Value After Reset: 0x1
[23:21]	RESERVED_5	-	

Bits	Field Name	Access	Description
[20]	SW_ISP_VENC_SHAKE_ARSTN	RW	ISP_VENC_HANDSHAKE sw AXI reset 0: resetn active Note: Reset flow should follow the steps: 1. Reset sw_isp_venc_shake_arstn. 2. Reset sw_iopmp_vipre_presetn. 3. Release sw_isp_venc_shake_presetn. 4. Release sw_isp_venc_shake_arstn. Value After Reset: 0x1
[19:17]	RESERVED_4	-	
[16]	SW_VISYS_PRESETN	RW	VI subsystem sw APB reset 0: resetn active Value After Reset: 0x1
[15:13]	RESERVED_3	-	
[12]	SW_AXI4_VISYS_ARST_N	RW	VI subsystem sw AXI reset 0: resetn active Value After Reset: 0x1
[11]	RESERVED_2	-	
[10]	SW_AXI4_VISYS1_ARST_N	RW	ISP0 bus sw AXI reset 0: resetn active Value After Reset: 0x1
[9]	SW_AXI4_VISYS2_ARST_N	RW	ISP1 bus AXI reset 0: resetn active Value After Reset: 0x1
[8]	SW_AXI4_VISYS3_ARST_N	RW	ISP_RY and DW200 bus sw AXI reset 0: resetn active Value After Reset: 0x1
[7:0]	RESERVED_1	-	

5.4.2.5.5 CFG_RST_LOCK_TEE

- Description: VI reset register TEE lock
- Offset: 0x1210
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_5	-	
[30]	VI_SUBSYS_RSTCFG_LOCK	RW	VI_SUBSYS_RSTCFG_LOCK Value After Reset: 0x0
[29]	VI_SUBSYS1_RSTCFG_LOCK	RW	VI_SUBSYS1_RSTCFG_LOCK Value After Reset: 0x0
[28]	VI_SUBSYS2_RSTCFG_LOCK	RW	VI_SUBSYS2_RSTCFG_LOCK Value After Reset: 0x0
[27]	VI_SUBSYS3_RSTCFG_LOCK	RW	VI_SUBSYS3_RSTCFG_LOCK Value After Reset: 0x0
[26:25]	RESERVED_4	-	
[24]	DW200_RSTCFG_LOCK	RW	DW200_RSTCFG_LOCK Value After Reset: 0x0
[23:18]	RESERVED_3	-	
[17]	ISP_RSTCFG_LOCK	RW	ISP_RSTCFG_LOCK Value After Reset: 0x0
[16]	ISP_RY_RSTCFG_LOCK	RW	ISP_RY_RSTCFG_LOCK Value After Reset: 0x0
[15]	MIPI_CSI2X2_FIFO_RSTCFG_LOCK	RW	MIPI_CSI2X2_FIFO_RSTCFG_LOCK Value After Reset: 0x0
[14]	MIPI_CSI0_RSTCFG_LOCK	RW	MIPI_CSI0_RSTCFG_LOCK Value After Reset: 0x0
[13]	MIPI_CSI1_RSTCFG_LOCK	RW	MIPI_CSI1_RSTCFG_LOCK Value After Reset: 0x0
[12]	MIPI_CSI2_RSTCFG_LOCK	RW	MIPI_CSI2_RSTCFG_LOCK Value After Reset: 0x0
[11:10]	RESERVED_2	-	
[9]	ISP_VENC_SHAKE_RSTCFG_LOCK	RW	ISP_VENC_SHAKE_RSTCFG_LOCK Value After Reset: 0x0
[8]	VIPRE_RSTCFG_LOCK	RW	VIPRE_RSTCFG_LOCK Value After Reset: 0x0
[7:0]	RESERVED_1	-	

5.4.2.6 VO_SUBSYS

5.4.2.6.1 GPU_RST_CFG

- Description: GPU reset register
- Offset: 0x00
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_GPU_CLKGEN_RST_N	RW	GPU clkgen reset, sw_gpu_clkgen_rst_n active low Value After Reset: 0x0
[0]	SW_GPU_RST_N	RW	GPU reset, sw_gpu_rst_n active low Value After Reset: 0x0

5.4.2.6.2 DPU_RST_CFG

- Description: DPU reset register
- Offset: 0x04
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	SW_DPU_CRST_N	RW	DPU Core reset, sw_dpu_crst_n active low Value After Reset: 0x0
[1]	SW_DPU_ARST_N	RW	DPU AXI reset, sw_dpu_arst_n active low Value After Reset: 0x0
[0]	SW_DPU_HRST_N	RW	DPU AHB reset, sw_dpu_hrst_n active low Value After Reset: 0x0

5.4.2.6.3 MIPI_DSI0_RST_CFG

- Description: DSI0 reset register
- Offset: 0x8
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_MIPI_DSI0_PRST_N	RW	MIPI_DSI0 APB reset, sw_mipi_dsi0_prst_n active low Value After Reset: 0x1

5.4.2.6.4 MIPI_DSI1_RST_CFG

- Description:
- Offset: 0xc
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_MIPI_DSI1_PRST_N	RW	MIPI_DSI1 APB reset, sw_mipi_dsi1_prst_n active low Value After Reset: 0x1

5.4.2.6.5 HDMI_RST_CFG

- Description:
- Offset: 0x14
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_HDMI_PRST_N	RW	HDMI APB reset, sw_hdmi_prst_n active low Value After Reset: 0x1
[0]	SW_HDMI_MAIN_RST_N	RW	HDMI Main reset, sw_hdmi_main_rst_n active low Value After Reset: 0x1

5.4.2.6.6 AXI4_VO_DW_AXI

- Description: AXI4 bus reset register
- Offset: 0x18
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_AXI4_VO_PRST_N	RW	AXI_VO bus APB reset, sw_axi4_vo_prst_n active low Value After Reset: 0x1
[0]	SW_AXI4_VO_ARST_N	RW	AXI_VO bus AXI reset, sw_axi4_vo_arst_n active low Value After Reset: 0x1

5.4.2.6.7 X2H_X4_VOSYS_DW_AXI_X2H

- Description: X2H bus reset register
- Offset: 0x20

- Default Value: 0xf

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	SW_X2H_DPU1_HRST_N	RW	X2H_DPU bus AHB reset, sw_x2h_dpu1_hrst_n active low Value After Reset: 0x1
[2]	SW_X2H_DPU1_ARST_N	RW	X2H_DPU bus AXI reset, sw_x2h_dpu1_arst_n active low Value After Reset: 0x1
[1]	SW_X2H_DPU_HRST_N	RW	X2H_DPU bus AHB reset, sw_x2h_dpu_hrst_n active low Value After Reset: 0x1
[0]	SW_X2H_DPU_ARST_N	RW	X2H_DPU bus AXI reset, sw_x2h_dpu_arst_n active low Value After Reset: 0x1

5.4.2.6.8 GPU_RST_CFG_TEE

- Description: GPU reset TEE register
- Offset: 0x1000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_GPU_CLKGEN_RST_N	RW	GPU clkgen reset, sw_gpu_clkgen_rst_n active low Value After Reset: 0x0
[0]	SW_GPU_RST_N	RW	GPU reset, sw_gpu_rst_n active low Value After Reset: 0x0

5.4.2.6.9 DPU_RST_CFG_TEE

- Description: DPU reset TEE register
- Offset: 0x1004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	SW_DPU_CRST_N	RW	DPU Core reset, sw_dpu_crst_n active low Value After Reset: 0x0
[1]	SW_DPU_ARST_N	RW	DPU AXI reset, sw_dpu_arst_n active low

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[0]	SW_DPU_HRST_N	RW	DPU AHB reset, sw_dpu_hrst_n active low Value After Reset: 0x0

5.4.2.6.10 MIPI_DSI0_RST_CFG_TEE

- Description: DSI0 APB reset TEE register
- Offset: 0x1008
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_MIPI_DSI0_PRST_N	RW	MIPI_DSI0 APB reset, sw_mipi_dsi0_prst_n active low Value After Reset: 0x1

5.4.2.6.11 MIPI_DSI1_RST_CFG_TEE

- Description: DSI1 APB reset TEE register
- Offset: 0x100c
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SW_MIPI_DSI1_PRST_N	RW	MIPI_DSI1 APB reset, sw_mipi_dsi1_prst_n active low Value After Reset: 0x1

5.4.2.6.12 IOPMP_VOSYS_RST_CFG_TEE

- Description: IOPMP reset TEE register
- Offset: 0x1010
- Default Value: 0x3f

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	SW_IOPMP_VOSYS_DPU1_ARST_N	RW	IOPMP_DPU1 AXI reset, sw_iopmp_vosys_dpu1_prst_n active low 1. User must follow the first reset, the last de-reset ruler. 2. User must mask IOPMP reset before reset. Value After Reset: 0x1

Bits	Field Name	Access	Description
[4]	SW_IOPMP_VOSYS_DPU_ARST_N	RW	IOPMP_DPU AXI reset, sw_iopmp_vosys_dpu_prst_n active low 1. User must follow the first reset, the last de-reset ruler. 2. User must mask IOPMP reset before reset. Value After Reset: 0x1
[3]	SW_IOPMP_VOSYS_GPU_ARST_N	RW	IOPMP_GPU AXI reset, sw_iopmp_vosys_gpu_prst_n active low 2. User must follow the first reset, the last de-reset ruler. 3. User must mask IOPMP reset before reset. Value After Reset: 0x1
[2]	SW_IOPMP_VOSYS_DPU1_PRST_N	RW	IOPMP_DPU1 APB reset, sw_iopmp_vosys_dpu1_prst_n active low 1. User must follow the first reset, the last de-reset ruler. 2. User must mask IOPMP reset before reset. Value After Reset: 0x1
[1]	SW_IOPMP_VOSYS_DPU_PRST_N	RW	IOPMP_DPU APB reset, sw_iopmp_vosys_dpu_prst_n active low 1. User must follow the first reset, the last de-reset ruler. 2. User must mask IOPMP reset before reset. Value After Reset: 0x1
[0]	SW_IOPMP_VOSYS_GPU_PRST_N	RW	IOPMP_GPU APB reset, sw_iopmp_vosys_gpu_prst_n active low 1. User must follow the first reset, the last de-reset ruler. 2. User must mask IOPMP reset before reset. Value After Reset: 0x1

5.4.2.6.13 HDMI_RST_CFG_TEE

- Description: HDMI reset TEE register
- Offset: 0x1014
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_HDMI_PRST_N	RW	HDMI APB reset, sw_hdmi_prst_n active low Value After Reset: 0x1
[0]	SW_HDMI_MAIN_RST_N	RW	HDMI Main reset, sw_hdmi_main_rst_n active low Value After Reset: 0x1

5.4.2.6.14 AXI4_VO_DW_AXI_TEE

- Description: AXI4_VO bus reset TEE register
- Offset: 0x1018
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_AXI4_VO_PRST_N	RW	AXI_VO bus APB reset, sw_axi4_vo_prst_n active low Value After Reset: 0x1
[0]	SW_AXI4_VO_ARST_N	RW	AXI_VO bus AXI reset, sw_axi4_vo_arst_n active low Value After Reset: 0x1

5.4.2.6.15 X2H_X4_VOSYS_DW_AXI_X2H_TEE

- Description: X2H reset TEE register
- Offset: 0x1020
- Default Value: 0xf

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	SW_X2H_DPU1_HRST_N	RW	X2H_DPU bus AHB reset, sw_x2h_dpu1_hrst_n active low Value After Reset: 0x1
[2]	SW_X2H_DPU1_ARST_N	RW	X2H_DPU bus AXI reset, sw_x2h_dpu1_arst_n active low Value After Reset: 0x1
[1]	SW_X2H_DPU_HRST_N	RW	X2H_DPU bus AHB reset, sw_x2h_dpu_hrst_n active low Value After Reset: 0x1
[0]	SW_X2H_DPU_ARST_N	RW	X2H_DPU bus AXI reset, sw_x2h_dpu_arst_n active low Value After Reset: 0x1

5.4.2.6.16 CFG_LOCK_TEE

- Description: Configuration lock TEE register
- Offset: 0x1a00
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7]	DPU_ADDR_REMAP_LOCK	RW	DPU address remap lock Value After Reset: 0x0
[6]	VO_SUBSYS_CFG_LOCK	RW	VO subsystem bus configuration lock Value After Reset: 0x0
[5]	TEST_CLK_CFG_LOCK	RW	TEST_CLK configuration lock for clk_calc module Value After Reset: 0x0
[4]	MIPI_DSI1_CFG_LOCK	RW	MIPI_DSI1 module configuration lock Value After Reset: 0x0
[3]	MIPI_DSI0_CFG_LOCK	RW	MIPI_DSI0 module configuration lock Value After Reset: 0x0
[2]	HDMI_CFG_LOCK	RW	HDMI module configuration lock Value After Reset: 0x0
[1]	GPU_CFG_LOCK	RW	GPU module configuration lock Value After Reset: 0x0
[0]	DPU_CFG_LOCK	RW	DPU module configuration lock Value After Reset: 0x0

5.4.2.7 VP_SUBSYS

5.4.2.7.1 AXIBUS_RST_CFG

- Description: AXIBUS_RST_CFG
- Offset: 0x00
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_AXI4_VPSYS_ARST_N	RW	VPSYS AXI4 bus core soft reset 1: Release reset. 0: Enter reset.

Bits	Field Name	Access	Description
			Value After Reset: 0x1
[0]	SW_AXI4_VPSYS_PRST_N	RW	VPSYS AXI4 bus APB soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1

5.4.2.7.2 FCE_RST_CFG

- Description: FCE_RST_CFG
- Offset: 0x04
- Default Value: 0x33

Bits	Field Name	Access	Description
[31:6]	RESERVED_2	-	
[5]	SW_X2XS_ARST_N	RW	FCE X2X slave reset, need assert master and slave reset in same time. 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[4]	SW_X2XM_ARST_N	RW	FCE X2X master reset, need assert master and slave reset in same time. 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[3:2]	RESERVED_1	-	
[1]	SW_FCE_ARST_N	RW	FCE core soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[0]	SW_FCE_PRST_N	RW	FCE APB soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1

5.4.2.7.3 G2D_RST_CFG

- Description: G2D_RST_CFG

- Offset: 0x08
- Default Value: 0x7

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	SW_G2D_CRST_N	RW	G2D core soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[1]	SW_G2D_ARST_N	RW	G2D aclk soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[0]	SW_G2D_PRST_N	RW	G2D APB soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1

5.4.2.7.4 VDEC_RST_CFG

- Description: VDEC_RST_CFG
- Offset: 0x0c
- Default Value: 0x7

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	SW_VDEC_CRST_N	RW	VDEC core soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[1]	SW_VDEC_ARST_N	RW	VDEC aclk soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[0]	SW_VDEC_PRST_N	RW	VDEC APB soft reset 1: Release reset. 0: Enter reset.

Bits	Field Name	Access	Description
			Value After Reset: 0x1

5.4.2.7.5 VENC_RST_CFG

- Description: VENC_RST_CFG
- Offset: 0x10
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_VENC_ARST_N	RW	VENC core soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[0]	SW_VENC_PRST_N	RW	VENC APB soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1

5.4.2.7.6 AXIBUS_RST_TEECFG

- Description: AXIBUS_RST_TEECFG
- Offset: 0x1000
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SW_AXI4_VPSYS_ARST_N	RW	VPSYS AXI4 bus core soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[0]	SW_AXI4_VPSYS_PRST_N	RW	VPSYS AXI4 bus APB soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1

5.4.2.7.7 FCE_RST_TEECFG

- Description: FCE_RST_TEECFG

- Offset: 0x1004
- Default Value: 0x3f

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	SW_X2XS_ARST_N	RW	FCE X2X slave reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[4]	SW_X2XM_ARST_N	RW	FCE X2X master reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[3]	SW_IOPMP_FCE_PRST_N	RW	FCE IOPMP APB soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[2]	SW_IOPMP_FCE_ARST_N	RW	FCE IOPMP core soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[1]	SW_FCE_ARST_N	RW	FCE core soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[0]	SW_FCE_PRST_N	RW	FCE APB soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1

5.4.2.7.8 G2D_RST_TEECFG

- Description: G2D_RST_TEECFG
- Offset: 0x1008
- Default Value: 0x1f

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	SW_IOPMP_G2D_PRST_N	RW	G2D IOPMP APB soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[3]	SW_IOPMP_G2D_ARST_N	RW	G2D IOPMP core soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[2]	SW_G2D_CRST_N	RW	G2D core soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[1]	SW_G2D_ARST_N	RW	G2D aclk soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[0]	SW_G2D_PRST_N	RW	G2D APB soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1

5.4.2.7.9 VDEC_RST_TEECFG

- Description: VDEC_RST_TEECFG
- Offset: 0x100c
- Default Value: 0x1f

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	SW_IOPMP_VDEC_PRST_N	RW	VDEC IOPMP APB soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[3]	SW_IOPMP_VDEC_ARST_N	RW	VDEC IOPMP core soft reset

Bits	Field Name	Access	Description
			1: Release reset. 0: Enter reset. Value After Reset: 0x1
[2]	SW_VDEC_CRST_N	RW	VDEC core soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[1]	SW_VDEC_ARST_N	RW	VDEC aclk soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[0]	SW_VDEC_PRST_N	RW	VDEC APB soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1

5.4.2.7.10 VENC_RST_TEECFG

- Description: VENC_RST_TEECFG
- Offset: 0x1010
- Default Value: 0xf

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	SW_IOPMP_VENC_PRST_N	RW	VENC IOPMP APB soft reset. 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[2]	SW_IOPMP_VENC_ARST_N	RW	VENC IOPMP core soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1
[1]	SW_VENC_ARST_N	RW	VENC core soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1

Bits	Field Name	Access	Description
[0]	SW_VENC_PRST_N	RW	VENC APB soft reset 1: Release reset. 0: Enter reset. Value After Reset: 0x1

5.4.2.8 DSP_SUBSYS

5.4.2.8.1 DSPSYS_SW_RST

- Description: DSP subsystem reset register
- Offset: 0x28
- Default Value: 0x511000f

Bits	Field Name	Access	Description
[31:27]	RESERVED_7	-	
[26]	SW_AXI4_DSP_RS_ARST_N	RW	AXI4_DSP_RS areset, active low Value After Reset: 0x1
[25]	RESERVED_6	-	
[24]	SW_AXI4_DSPSYS_ARST_N	RW	AXI4_DSPSYS areset, active low Value After Reset: 0x1
[23:21]	RESERVED_5	-	
[20]	SW_AXI4_DSPSYS_SLV_ARST_N	RW	AXI4_DSPSYS_SLV areset, active low Value After Reset: 0x1
[19:17]	RESERVED_4	-	
[16]	SW_DSPSYS_PRESETN	RW	DSPSYSP areset, active low Value After Reset: 0x1
[15]	RESERVED_3	-	
[14]	SW_DSP1_PRST_N	RW	DSP1 sw APB reset, active low Value After Reset: 0x0
[13]	SW_DSP1_DRST_N	RW	DSP1 sw debug reset, active low. Value After Reset: 0x0
[12]	SW_DSP1_CRST_N	RW	DSP1 sw core reset, active low Value After Reset: 0x0
[11]	RESERVED_2	-	

Bits	Field Name	Access	Description
[10]	SW_DSP0_PRST_N	RW	DSP0 sw APB reset, active low Value After Reset: 0x0
[9]	SW_DSP0_DRST_N	RW	DSP0 sw debug reset, active low Value After Reset: 0x0
[8]	SW_DSP0_CRST_N	RW	DSP0 sw core reset, active low Value After Reset: 0x0
[7:4]	RESERVED_1	-	
[3]	SW_X2X_X4_DSPSLV_DSP0_ARST_N	RW	DSP0 core reset, active low Value After Reset: 0x1
[2]	SW_X2X_X4_DSPSLV_DSP1_ARST_N	RW	X2X_X4_DSPSLV_DSP0 aresetn, active low Value After Reset: 0x1
[1]	SW_X2X_DSP0_ARST_N	RW	X2X_DSP0 areset, active low Value After Reset: 0x1
[0]	SW_X2X_DSP1_ARST_N	RW	X2X_DSP1 areset, active low Value After Reset: 0x1

5.4.2.8.2 DSPSYS_SW_RST_TEE

- Description: DSP subsystem reset TEE register
- Offset: 0x1028
- Default Value: 0x7d11000f

Bits	Field Name	Access	Description
[31]	RESERVED_7	-	
[30]	SW_IOPMP_DSP0_PRESETN	RW	IOPMP DSP0 bus preset: active low 1. User must follow the first reset, the last de-reset ruler. 2. User must mask IOPMP reset before reset. Value After Reset: 0x1
[29]	SW_IOPMP_DSP1_PRESETN	RW	IOPMP DSP0 bus preset, active low 1. User must follow the first reset, the last de-reset ruler. 2. User must mask IOPMP reset before reset. Value After Reset: 0x1
[28]	SW_IOPMP_DSP0_ARST_N	RW	IOPMP DSP0 bus preset, active low

Bits	Field Name	Access	Description
			1. User must follow the first reset, the last de-reset ruler. 2. User must mask IOPMP reset before reset. Value After Reset: 0x1
[27]	SW_IOPMP_DSP1_ARST_N	RW	IOPMP DSP0 bus areset, active low 1. User must follow the first reset, the last de-reset ruler. 2. User must mask IOPMP reset before reset. Value After Reset: 0x1
[26]	SW_AXI4_DSP_RS_ARST_N	RW	AXI4_DSP_RS areset, active low Value After Reset: 0x1
[25]	RESERVED_6	-	
[24]	SW_AXI4_DSPSYS_ARST_N	RW	AXI4_DSPSYS areset, active low Value After Reset: 0x1
[23:21]	RESERVED_5	-	
[20]	SW_AXI4_DSPSYS_SLV_ARST_N	RW	AXI4_DSPSYS_SLV areset, active low Value After Reset: 0x1
[19:17]	RESERVED_4	-	
[16]	SW_DSPSYS_PRESETN	RW	Dspsyspareset, active low Value After Reset: 0x1
[15]	RESERVED_3	-	
[14]	SW_DSP1_PRST_N	RW	DSP1 sw APB reset, resetn active Value After Reset: 0x0
[13]	SW_DSP1_DRST_N	RW	DSP1 sw debug reset, resetn active Value After Reset: 0x0
[12]	SW_DSP1_CRST_N	RW	DSP1 sw core reset, resetn active Value After Reset: 0x0
[11]	RESERVED_2	-	
[10]	SW_DSP0_PRST_N	RW	DSP0 sw APB reset, resetn active Value After Reset: 0x0
[9]	SW_DSP0_DRST_N	RW	DSP0 sw debug reset, resetn active Value After Reset: 0x0

Bits	Field Name	Access	Description
[8]	SW_DSP0_CRST_N	RW	DSP0 sw core reset, resetn active Value After Reset: 0x0
[7:4]	RESERVED_1	-	
[3]	SW_X2X_X4_DSPSLV_DSP0_ARST_N	RW	DSP0 core reset, resetn active Value After Reset: 0x1
[2]	SW_X2X_X4_DSPSLV_DSP1_ARST_N	RW	X2X_X4_DSPSLV_DSP0 aresetn, active low Value After Reset: 0x1
[1]	SW_X2X_DSP0_ARST_N	RW	X2X_DSP0 areset, active low Value After Reset: 0x1
[0]	SW_X2X_DSP1_ARST_N	RW	X2X_DSP1 areset, active low Value After Reset: 0x1

5.4.2.8.3 CFG_CLK_LOCK_TEE

- Description: Clock lock TEE register
- Offset: 0x1140
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_4	-	
[30]	DSP_SUBSYS_CLKCFG_LOCK	RW	DSP_SUBSYS_CLKCFG_LOCK Value After Reset: 0x0
[29:26]	RESERVED_3	-	
[25]	DSP_SUBSYS_SLV_CLKCFG_LOCK	RW	DSP_SUBSYS_SLV_CLKCFG_LOCK Value After Reset: 0x0
[24:7]	RESERVED_2	-	
[6]	DSPSYS_CLKCFG_LOCK	RW	DSPSYS_CLKCFG_LOCK Value After Reset: 0x0
[5]	DSP0_CLKCFG_LOCK	RW	DSP0_CLKCFG_LOCK Value After Reset: 0x0
[4]	DSP1_CLKCFG_LOCK	RW	DSP1_CLKCFG_LOCK Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	TEST_CLK_CFG_LOCK	RW	TEST_CLK_CFG_LOCK

Bits	Field Name	Access	Description
			Value After Reset: 0x0

5.4.2.8.4 CFG_RST_LOCK_TEE

- Description: Reset lock TEE register
- Offset: 0x1144
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_4	-	
[30]	DSP_SUBSYS_RSTCFG_LOCK	RW	DSP_SUBSYS_RSTCFG_LOCK Value After Reset: 0x0
[29:26]	RESERVED_3	-	
[25]	DSP_SUBSYS_SLV_RSTCFG_LOCK	RW	DSP_SUBSYS_SLV_RSTCFG_LOCK Value After Reset: 0x0
[24:6]	RESERVED_2	-	
[5]	DSP0_RSTCFG_LOCK	RW	DSP0_RSTCFG_LOCK Value After Reset: 0x0
[4]	DSP1_RSTCFG_LOCK	RW	DSP1_RSTCFG_LOCK Value After Reset: 0x0
[3:0]	RESERVED_1	-	

5.4.2.8.5 CFG_DSPSYS_LOCK_TEE

- Description: DSP subsystem lock TEE register
- Offset: 0x1148
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_1	-	
[8]	DSP1_DDR_CH_SEL_LOCK	RW	DSP1_DDR_CH_SEL_LOCK Value After Reset: 0x0
[7]	DSP0_DDR_CH_SEL_LOCK	RW	DSP0_DDR_CH_SEL_LOCK Value After Reset: 0x0
[6]	DSP1_REMAP_LOCK	RW	DSP1_REMAP_LOCK Value After Reset: 0x0

Bits	Field Name	Access	Description
[5]	DSP0_REMAP_LOCK	RW	DSP0_REMAP_LOCK Value After Reset: 0x0
[4]	DSPSYS_BUS_CFG_LOCK	RW	DSPSYS_BUS_CFG_LOCK Value After Reset: 0x0
[3]	RESERVED_REG0_LOCK	RW	RESERVED_REG0_LOCK Value After Reset: 0x0
[2]	RESERVED_REG1_LOCK	RW	RESERVED_REG1_LOCK Value After Reset: 0x0
[1]	DSP0_BUS_CFG_LOCK	RW	DSP0_BUS_CFG_LOCK Value After Reset: 0x0
[0]	DSP1_BUS_CFG_LOCK	RW	DSP1_BUS_CFG_LOCK Value After Reset: 0x0

5.4.2.9 AUDIO_SUBSYS

5.4.2.9.1 IP_RST_REG

- Description: Module reset control register
- Offset: 0x14
- Default Value: 0x7ffff10

Bits	Field Name	Access	Description
[31:27]	RESERVED_3	-	
[26]	IOMUX_SRST_N	RW	IOMUX soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[25]	VAD_SRST_N	RW	VAD soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[24]	SPDIF1_SRST_N	RW	SPDIF1 soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1

Bits	Field Name	Access	Description
[23]	SPDIF0_SRST_N	RW	SPDIF0 soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[22]	GPIO_SRST_N	RW	GPIO soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[21]	TDM_SRST_N	RW	TDM soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[20]	I2S8CH_SRST_N	RW	I2S-IN soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[19]	I2S2_SRST_N	RW	I2S2 soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[18]	I2S1_SRST_N	RW	I2S1 soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[17]	I2S0_SRST_N	RW	I2S0 soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[16]	UART_SRST_N	RW	UART soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[15]	I2C1_SRST_N	RW	I2C1 soft reset 0: Enter reset.

Bits	Field Name	Access	Description
			1: Release reset. Value After Reset: 0x1
[14]	I2C0_SRST_N	RW	I2C0 soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[13]	WDT_SRST_N	RW	WDT soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[12]	TIM_CNT4_SRST_N	RW	Timer CNT4 soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[11]	TIM_CNT3_SRST_N	RW	Timer CNT3 soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[10]	TIM_CNT2_SRST_N	RW	Timer CNT2 soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[9]	TIM_CNT1_SRST_N	RW	Timer CNT1 soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[8]	TIMER_SRST_N	RW	Timer APB soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x1
[7:5]	RESERVED_2	-	
[4]	BSM_SRST_N	RW	Bus monitor soft reset 0: Enter reset.

Bits	Field Name	Access	Description
			1: Release reset. Value After Reset: 0x1
[3]	DMA_SRST_N	RW	DMA soft reset 0: Enter reset. 1: Release reset. Value After Reset: 0x0
[2:0]	RESERVED_1	-	

6 Low Power

6.1 Overview

The power management system is used to manage power consumption of the entire chip and provide multiple power consumption modes to meet power consumption requirements in different scenarios.

6.2 Main Features

- Support normal run mode, idle mode, HW-VAD mode, and standby mode.
- Support clock gate and power down.
- Support the following wakeup sources: HW-VAD, RTC, and GPIO (keyboard, WIFI, etc.).

6.3 Function Description

6.3.1 Power Domain

The main power domains of the chip are divided into four, namely, AON SUBSYS, DDR SUBSYS, AP SUBSYS and C910. These power domains can be powered down with the external PMIC and follow a certain power-up sequence. Isolation protection is made inside the chip to support power up/power down.

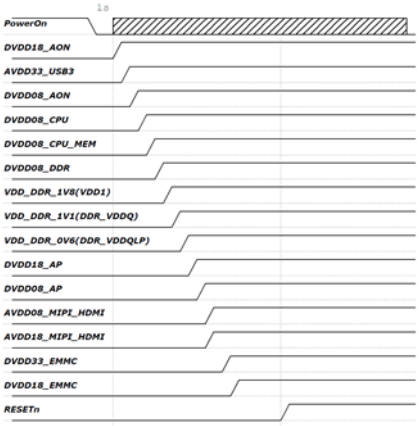


Figure & Table 6-1 Power-up sequence

AON SUBSYS is the power control switch of the entire system. It is used to control system power down and wakeup, regulate C910 voltage, and control DDR to enter the self-refresh mode before entering the standby mode. DDR SUBSYS supports LP2 and LP3/IO Retention low power mode. AP SUBSYS is mainly used for video related applications. C910 supports DVFS.

Other digital modules, such as AUDIO, VDEC, NPU, VENC, GPU, DSP and CPU CORE are powered down by the internal power switch according to leakage power estimation.

Figure & Table 6-2 Power domain division

Power Domain	Power Down Mode
AP SYS Island	External PMIC
AON SYS Island	External PMIC
DDR SYS Island	External PMIC
C910 TOP Island	External PMIC
AUDIO SYS Island	Internal Power Switch
VDEC Island	Internal Power Switch
NPU Island	Internal Power Switch
VENC Island	Internal Power Switch
GPU Island	Internal Power Switch
DSP0 Island	Internal Power Switch
DSP1 Island	Internal Power Switch
C910 CORE0 Island	Internal Power Switch
C910 CORE1 Island	Internal Power Switch
C910 CORE2 Island	Internal Power Switch
C910 CORE3 Island	Internal Power Switch

6.3.2 Power Architecture

The block diagram of the chip power control architecture is shown in Figure & Table 6-3. AON SUBSYS is the always-on domain and the rest are power-down domains. As the power control core SUBSYS of the whole system, AON SUBSYS integrates E902 low-power CPU and controls the external PMIC to power up/power down the whole chip through I2C interface. AON SUBSYS obtains chip temperature and voltage through PVTC, to regulate the chip voltage and frequency to control power consumption. The chip main CPU C910 supports DVFS.

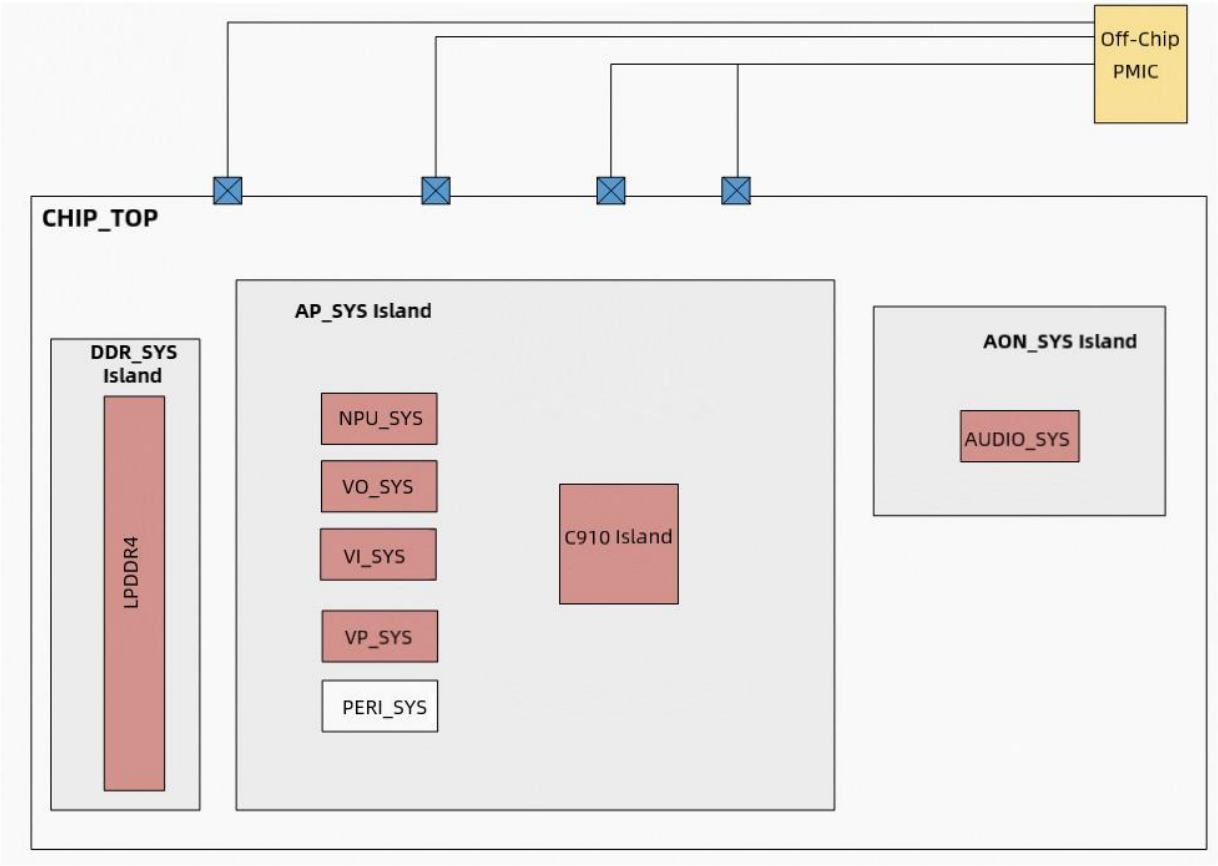


Figure & Table 6-3 Block diagram of power control architecture

6.3.3 Low Power Mode

Power states in each low power mode are shown in Figure & Table 6-4.

Figure & Table 6-4 Low power mode

Power Domain	Power Rail	OFF	STANDBY	HW-VAD	IDLE	RUN
AP SYS Island	DVDD08_AP	OFF	OFF	OFF	ON	ON
	DVDD18_AP1	OFF	OFF	ON	ON	ON
	DVDD18_AP2	OFF	OFF	ON	ON	ON
	DVDD18_RGM	OFF	OFF	ON	ON	ON
	TAVDD_TS	OFF	OFF	ON/OFF	ON	ON
	TAVDD_ADC	OFF	OFF	ON/OFF	ON	ON
	VP_USB3	OFF	ON	ON	ON	ON
	VPTX0_USB3	OFF	ON	ON	ON	ON
	DVDD_USB3	OFF	ON	ON	ON	ON
	VPH_USB3	OFF	ON	ON	ON	ON

Power Domain	Power Rail	OFF	STANDBY	HW-VAD	IDLE	RUN
	VDDH0_USB3	OFF	ON	ON	ON	ON
	VDD330_USB3	OFF	ON	ON	ON	ON
	VDD_CORE_EMMC	OFF	OFF	OFF	ON	ON
	VDDIO_EMMC	OFF	OFF	ON/OFF	ON	ON
	VDDIO33_EMMC	OFF	OFF	ON/OFF	ON	ON
	VDDIO_SDIO0	OFF	OFF	ON/OFF	ON	ON
	VDDIO33_SDIO0	OFF	OFF	ON/OFF	ON	ON
	VDDIO_SDIO1	OFF	OFF	ON/OFF	ON	ON
	VDDIO33_SDIO1	OFF	OFF	ON/OFF	ON	ON
	VDDHV_PLL_AP	OFF	OFF	ON/OFF	ON	ON
	VDDREF_PLL_AP	OFF	OFF	OFF	ON	ON
	VDDPOST_CPU_PLL0	OFF	OFF	OFF	ON	ON
	VDDPOST_CPU_PLL1	OFF	OFF	OFF	ON	ON
	VDDPOST_GMAC_PLL	OFF	OFF	OFF	ON	ON
	VDDPOST_VIDEO_PLL	OFF	OFF	OFF	ON	ON
	VDDPOST_DPU0_PLL	OFF	OFF	OFF	ON	ON
	VDDPOST_DPU1_PLL	OFF	OFF	OFF	ON	ON
	VDDPOST_TEE_PLL	OFF	OFF	OFF	ON	ON
	VQPS_EFUSE	OFF	OFF	OFF	ON	ON
	VP_MIPI_CSI2	OFF	OFF	OFF	ON	ON
	VPH_MIPI_CSI2	OFF	OFF	ON/OFF	ON	ON
	VP_MIPI_CSI0	OFF	OFF	OFF	ON	ON
	VPH_MIPI_CSI0	OFF	OFF	ON/OFF	ON	ON
	VP_MIPI_CSI1	OFF	OFF	OFF	ON	ON
	VPH_MIPI_CSI1	OFF	OFF	ON/OFF	ON	ON
	VP_MIPI_DSI0	OFF	OFF	OFF	ON	ON
	VPH_MIPI_DSI0	OFF	OFF	ON/OFF	ON	ON
	VP_MIPI_DSI1	OFF	OFF	OFF	ON	ON
	VPH_MIPI_DSI1	OFF	OFF	ON/OFF	ON	ON

Power Domain	Power Rail	OFF	STANDBY	HW-VAD	IDLE	RUN
	VP_HDMI	OFF	OFF	OFF	ON	ON
	VPH_HDMI	OFF	OFF	OFF	ON	ON
DDR SYS Island	VDD_DDR	OFF	OFF	OFF	ON	ON
	VDDQ_DDR	OFF	OFF	ON	ON	ON
	VDDQLP_DDR	OFF	OFF	ON	ON	ON
	VDD_PLL_DDR	OFF	OFF	OFF	ON	ON
	VDDHV_PLL_DDR	OFF	OFF	OFF	ON	ON
	VDDREF_PLL_DDR	OFF	OFF	OFF	ON	ON
	VDDPOST_DDR_PLL	OFF	OFF	OFF	ON	ON
	VDDQ_DDR1	OFF	OFF	ON	ON	ON
	VDDQLP_DDR1	OFF	OFF	ON	ON	ON
	VDD_PLL_DDR1	OFF	OFF	OFF	ON	ON
C910 TOP Island	DVDD_CPU	OFF	OFF	OFF	ON	0.8/0.7/0.55V
	DVDDM_CPU	OFF	OFF	OFF	ON	0.8/0.8/0.75V
AON SYS Island	DVDD08_AON	OFF	ON	ON	ON	ON
	DVDD18_AON	OFF	ON	ON	ON	ON
	TACVDD_RTC	OFF	ON	ON	ON	ON
	VDDHV_PLL_AON	OFF	ON	ON	ON	ON
	VDDREF_PLL_AON	OFF	ON	ON	ON	ON
	VDDPOST_AUDIO_PLL	OFF	ON	ON	ON	ON
	VDDPOST_SYS_PLL	OFF	ON	ON	ON	ON
	VDDIO_POR	OFF	ON	ON	ON	ON
	VDDHV_RC	OFF	ON	ON	ON	ON
AUDIO SYS Island	PD_AUDIO_SYS/ DVDD08_SW	OFF	OFF	ON	ON/OFF	ON
VDEC Island	PD_VDEC/ SS_VDEC	OFF	OFF	OFF	ON/OFF	ON
NPU Island	PD_NPU_SUBSYS/ DVDD08_SW	OFF	OFF	OFF	ON/OFF	ON

Power Domain	Power Rail	OFF	STANDBY	HW-VAD	IDLE	RUN
VENC Island	PD_VC8000E/ DVDD08_SW	OFF	OFF	OFF	ON/OFF	ON
GPU Island	PD_RGX_DUST_TOP/ DVDD08_SW	OFF	OFF	OFF	ON/OFF	ON
DSP0 Island	PD_DSP/DVDD08_SW	OFF	OFF	OFF	ON/OFF	ON
DSP1 Island	PD_DSP/DVDD08_SW	OFF	OFF	OFF	ON/OFF	ON
C910 CORE0 Island	PD_CT_TOP/ DVDD_CPU_SW	OFF	OFF	OFF	ON/OFF	0.8/0.7/0.55V
C910 CORE1 Island	PD_CT_TOP/ DVDD_CPU_SW	OFF	OFF	OFF	ON/OFF	0.8/0.7/0.55V
C910 CORE2 Island	PD_CT_TOP/ DVDD_CPU_SW	OFF	OFF	OFF	ON/OFF	0.8/0.7/0.55V
C910 CORE3 Island	PD_CT_TOP/ DVDD_CPU_SW	OFF	OFF	OFF	ON/OFF	0.8/0.7/0.55V

- OFF: Shutdown state. All power supplies are off.
- STANDBY: Deep sleep mode. All power supplies are off except for the necessary AON power supply. If the system does not run for a long time, it will enter this mode to save power and will be waked up in a timed manner.
- HW-VAD: Hardware VAD standby mode. AUDIO power supply must be on in addition to the always-on AON power supply. Voice wakeup is supported in this mode.
- IDLE: AP idle mode. In this mode, the system processes some lightweight transactions, such as playing music and showing logo, and controls power up/power down of C910 CORE, AUDIO, DSP, NPU, GPU, VENC and VDEC based on actual scenarios.
- RUN: Operation mode at full speed.

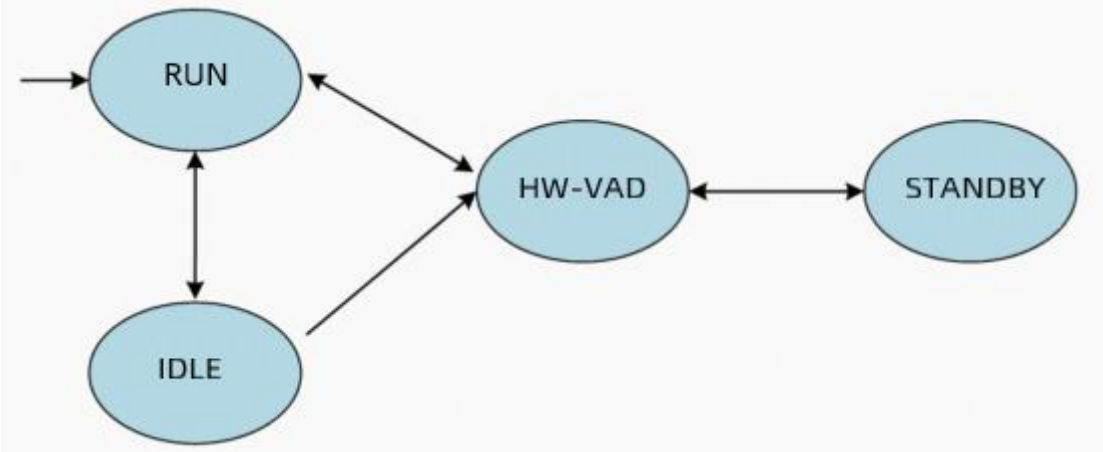


Figure & Table 6-5 Mode switch

Mode switch is shown in Figure & Table 6-5. Hardware supports the above mode switch that is carried out by software. Mode switch details are as follows:

- The system enters the RUN mode upon startup.
- RUN->HW-VAD: The system enters the HW-VAD mode if it does not work for a long time.
- HW-VAD->RUN: The system enters the RUN mode after it detects any voice activity and recognizes keywords.
- RUN->IDLE: AP does not work for a long time or the system only needs to play music after voice wakeup without the need of AP participation, AP enters the IDLE mode.
- IDLE->RUN: AP is waked up upon video phone access.
- IDLE->HW-VAD: The system enters the HW-VAD mode if AUDIO SUBSYS does not work for a long time.
- HW-VAD->STANDBY: The system enters the STANDBY mode if AUDIO SUBSYS does not work in specific scenarios.
- STANDBY->HW-VAD: The system enters the HW-VAD mode upon timed wakeup.

6.3.4 Wakeup Source

Wakeup sources include VAD wakeup, RTC wakeup, and GPIO wakeup (keyboard and WIFI). The architecture of the whole wakeup control is shown in Figure & Table 6-6. PMU is used to control the clock of E902. After entering the HW-VAD or STANDBY mode (APSYS, C910 and DDR power down), if E902 does not need to process other services, the clock of AONSYS can be turned off. At this time, E902 executes the WFI instruction, and LP_MODE[1:0] of E902 is 2'b00. After PMU receives this instruction, it turns off the clock of AONSYS.

After PMU receives the request from the wakeup source, it turns on the clock of AONSYS. E902 receives the corresponding wakeup interrupt and continues to execute PC from last stop.

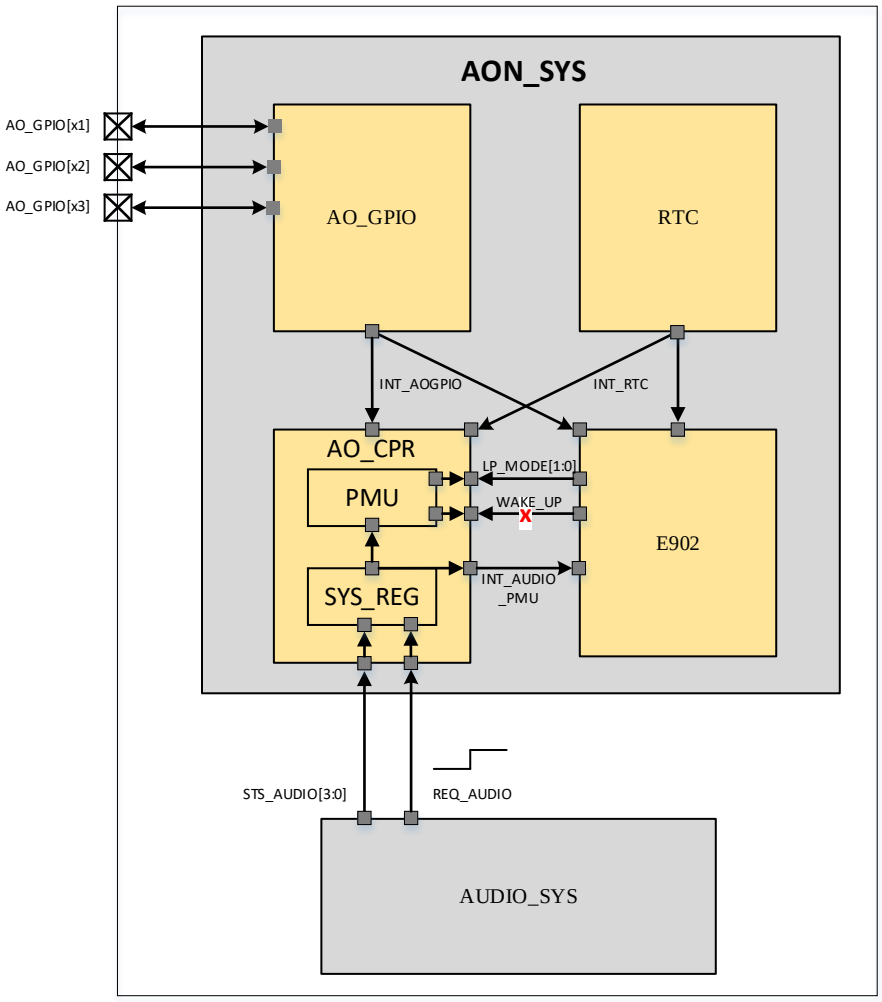


Figure & Table 6-6 Block diagram of wakeup architecture

As shown in Figure & Table 6-7, if in HW-VAD mode, when the clock of AONSYS is on, PMU does not need any wakeup source (E902 directly accepts the wakeup interrupt). E902 is active at this time. After E902 receives the wakeup interrupt, it starts to execute the corresponding command. When the clock of AONSYS is off, wakeup sources of PMU are INT_AOGPIO, INT_RTC and INT_AUDIO. When PMU receives the request from any wakeup source and the wakeup source is not shielded, PMU will turn on the clock of AONSYS. In STANDBY mode, AUDIO_SYS is powered down, so the wakeup sources are INT_AOGPIO and INT_RTC.

Figure & Table 6-7 Low power mode and wakeup source

Low Power Mode	AONSYS Clock State	PMU Wakeup Source	E902 Wakeup Source
HW-VAD	ON	N/A	INT_AOGPIO, INT_RTC, INT_AUDIO
	OFF	INT_AOGPIO, INT_RTC,	INT_AOGPIO, INT_RTC,

Low Power Mode	AONSYS Clock State	PMU Wakeup Source	E902 Wakeup Source
		INT_AUDIO	INT_AUDIO
STANDBY	OFF	INT_AOGPIO, INT_RTC	INT_AOGPIO, INT_RTC

Wakeup sources and their application are shown in Figure & Table 6-8. IN_AOGPIO is a level interrupt generated when the external AO_GPIO changes and this interrupt is used for wakeup. Level polarity is configurable. Please refer to the GPIO datasheet for details.

Figure & Table 6-8 Wakeup source and application

Wakeup Source	Application
INT_AOGPIO	When receiving any AO_GPIO request, an AOGPIO interrupt is generated to wake up PMU and E902. AO_GPIO[x1]: WIFI, wakeup through INT_AOGPIO. AO_GPIO[x2]: Keyboard, wakeup through INT_AOGPIO. AO_GPIO[x3]: Reserved, wakeup through INT_AOGPIO.
INT_RTC	RTC timed wakeup source
INT_AUDIO	Interrupt request from AUDIO_SYS. AO_CPR generates an interrupt after it receives the interrupt request from AUDIO_SYS. Please refer to 6.4.1 Communication between Cores for details.

6.4 Usage

6.4.1 Communication between Cores

This chapter mainly describes communication between AON_SYS (E902), AP_SYS (C910) and AUDIO_SYS (C906) in low power mode.

6.4.1.1 AON_SYS and AUDIO_SYS

AUDIO_SYS has the following request to AON_SYS: request to power up AP.
After AP_SYS is powered down, the bus channel between AUDIO_SYS and AON_SYS is disconnected and AUDIO_SYS cannot communicate with AON_SYS through Mailbox. AUDIO_SYS needs to provide a request signal AUDIO_PMU_REQ and a 32-bit state signal AUDIO_PMU_STS to AON_SYS. CPR generates an interrupt AUDIO_PMU_INTR to E902 after it receives the request signal AUDIO_PMU_REQ and the state signal AUDIO_PMU_STS. This interrupt can be cleared or shielded by the register in CPR.

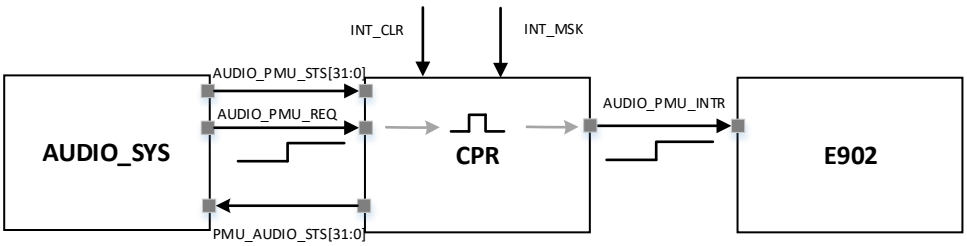


Figure & Table 6-9 Communication between AUDIO_SYS and AON_SYS

AUDIO_SYS sends requests to AON_SYS in the sequence as follows:

1. Write AUDIO_PMU_STS[31:0].
2. Pull AUDIO_PMU_REQ low.
3. Pull AUDIO_PMU_REQ high.

6.4.1.2 AON_SYS and AP_SYS

AP_SYS has the following requests to AON_SYS:

- Request to enter the HW-VAD mode
- Request to enter the STANDBY mode
- Request to regulate the voltage of C910

AP_SYS has no wakeup request to AON_SYS.

Communication between AP_SYS and AON_SYS is through Mailbox, as shown in Figure & Table 6-10.

Figure & Table 6-10 Communication between AP_SYS and AON_SYS

When C910 requests to enter the HW-VAD or STANDBY mode, it writes to Mailbox. Mailbox sends an interrupt to notify E902 and the latter reads CPU_LP_MODE of C910 and C906 and AXI state of DDR. E902 powers down AP_SYS (HW-VAD) or the whole system except for AON_SYS (STANDBY) when C910, C906 and DDR do not work.

6.4.2 Mode Switch Process

6.4.2.1 Module

6.4.2.1.1 C910 Core Power Up/Power Down

6.4.2.1.1.1 Power Down Process

The system can completely power down static power consumption of the core by turning off the power supply. The core power down process is as follows:

① C910 core to be powered down performs the operations as follows:

a) Shield all interrupt requests of the core, including external interrupt, soft interrupt, and timer interrupt and disable interrupt enable bits MIE and SIE of MSTATUS and SSTATUS registers and interrupt enable bits of MIE and SIE registers.
b) Disable data prefetch.
c) Execute INV&CLR D-Cache ALL and write dirty line back to L2C.
d) Disable D-Cache (No store instruction between cache clear and cache disable).
e) Disable the core snoop enable register to shield snoop on the core.
f) Execute fence iorw and iorw instructions.
g) Set the STANDBY mode register provided for the core in the system.
h) Execute the low power instruction WFI and enter the low power mode.

② The system performs the operations as follows (including external PMU and E902):

a) The system detects the core low power output signal corex_pad_lpmd_b is valid and the STANDBY mode register of the core is valid, triggering E902 to enter the C910 core power down process.
b) Set dbg_mask in the system debug shield register corresponding to the core to be powered down and send pad_corex_dbg_mask to C910.
c) Pull the reset signal pad_corex_rst_b of C910 core low to reset the CPU core.
d) Enable iso_en of the core output signal isolator.
e) After ensuring that the isolator works, the external PMU powers down the core.

6.4.2.1.1.2 Power Up Process

When the core is powered down, it can be restarted only through reset. The core power up process is as follows:

① When C910 operating core detects the system is overloaded and needs to wake up the CPU core, it will perform the operation as follows:

a) Notify E902 of the core to be waked up through mailbox. (Access addresses of secure and non-secure mailboxes are independent to ensure that the non-secure core cannot wake up the secure core.)

② E902:

a) Set the reset address rvbr corresponding to the core to be waked up (Reset addresses of secure and non-secure cores are independent to ensure that the non-secure core cannot modify the reset address of the secure core.).
b) Pull the core reset signal low.
c) Turn on the power supply, keep the reset signal not released, and PLL is stable.
d) Release iso_en of core output signal isolator.
e) Release the core reset signal.

③ Core to be waked up:

a) The core executes the initialization program, enables the SMPEN bit, and performs initialization operations such as enabling MMU and DCACHE. Isolator setting and power down support software and hardware modes. Other operations require software to write registers. For details, see 6.4.2.3 Block Power Up/Power Down.

6.4.2.1.2 VDEC/NPU/VENC/GPU/DSP Power Up/ Power Down

Follow 6.4.2.3 Block Power Up/Power Down.

6.4.2.2 System

6.4.2.2.1 Cold Start

① PMIC powers up AON, DDR, CPU and AP according to the power-up sequence of the chip.

② After the POR module detects power-up, it starts to reset that will last for about 10ms and releases reset, and then releases iso_en of AON, AP, DDR, and CPU isolators.

③ After reset, C910 enters BootROM, reads the system low power mode register and determines whether it is HW-VAD wakeup.

④ C910 configures the reset start addresses of E902 and C906, and releases reset of E902 and C906.

6.4.2.2.2 HW-VAD

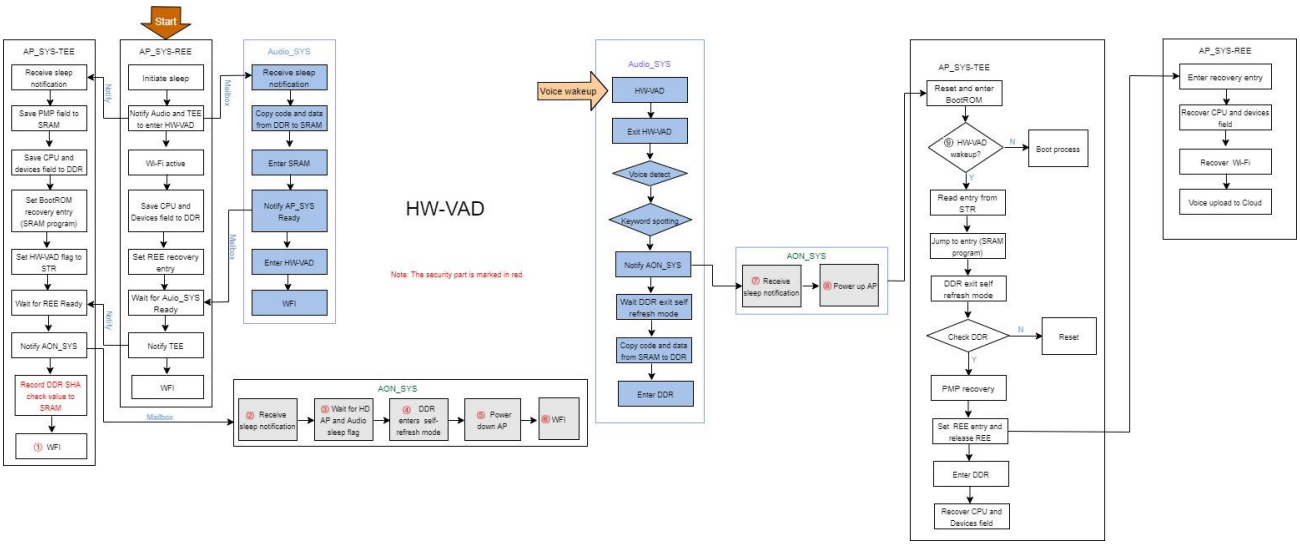


Figure & Table 6-11 HW-VAD sleep and wakeup flowchart

6.4.2.2.2.1 Enter the HW-VAD Mode

No.	Operation Process
①	**C910 slave core executes the core power down process (Refer to *"C910MP Power Management SPECV1.6"*):** a) Shield all interrupt requests of the core, including external interrupt, soft interrupt, and timer interrupt. Disable the interrupt enable bits MIE and SIE of MSTATUS and SSTATUS registers and interrupt enable bits of MIE and SIE registers. b) Disable data prefetch. c) Execute INV&CLR D-Cache ALL and write dirty line back to L2C. d) Disable D-Cache (No store instructions between cache clear and cache disable). e) Disable the core snoop enable register to shield snoop on the core. f) Execute fence iorw and iorw instructions. g) Set the STANDBY mode register provided for the core in the system (Mailbox). h) Execute the low power instruction WFI and enter the low power mode.
②	**C910 master core executes the core power down process (Refer to *"C910MP Power Management SPECV1.6"*):** a) Shield all interrupt requests of the core, including external interrupt, soft interrupt, and timer interrupt. Disable the interrupt enable bits MIE and SIE of MSTATUS and SSTATUS registers and interrupt enable bits of MIE and SIE registers. b) Disable data prefetch. c) Execute dcache inv&clr all. d) Disable D-Cache. e) Disable SMPEN of the core. f) Execute fence iorw and iorw instructions. g) Set the STANDBY mode register provided for the master core in the system (Mailbox). h) Execute the low power instruction WFI and enter the low power mode.
③	**C906 enters the low power mode (WFI).**
④	**E902 receives sleep notification (Mailbox).**
⑤	**E902 waits for sleep flags of C910 and C906, and performs the following system operations:** a) Read that the lpmd_b register of C910 and C906 is in low power mode. b) Set the debug shield control bit. c) Send pad_cpu_l2cache_flush_req to C910. d) Waits C910 returns cpu_pad_l2cache_flush_done. e) Pull pad_cpu_l2cache_flush_req low. f) Pull cpu_pad_l2cache_flush_done low. g) Wait C910 returns cpu_pad_no_op. h) Activate the SD signal of C910 dual-rail Memory.

No.	Operation Process
⑥	**Before powering down DDR, CPU, AP and AUDIO, E902 needs to perform the following operations:** a) Control DDR to enter the self-refresh mode. b) Enable DDR reset (DDR clock off) and activate the input isolator signal of DDR. c) Enable AP reset and turn off AP clock. d) Activate the input isolator signals of USB PHY, C910 TOP, and AON. e) Configure the STR_INDICATOR register and mark hot start. f) Configure board level components to enter the low power mode. g) Configure 1.5MB Share SRAM to enter the SD or DSLP mode. h) Enable 1.5M SRAM AXI Port reset and PVTC reset. i) Control the external PMIC to power down AP, DDR and C910 in sequence.
⑦	**Before executing WFI, E902 needs to perform the following operations:** a) Turn off unnecessary AUDIO clocks: （a） Turn off clkgen_audio_subsys_sys_pll clock. （b） Turn off clkgen_audio_subsys_aclk_ap2cp clock. （c） Turn off clkgen_audio_subsys_aclk_cp2sram clock. （d） Turn off clkgen_audio_subsys_aclk_cp2ap clock. b) Configure AONSYS clock to the RC low frequency mode: （a） Configure RC to the low frequency mode. （b） Switch the clock to RC FOUT. （c） Switch the clock to 8 frequency division. c) Turn off unnecessary AONSYS clocks: （a） Turn of the clocks of UART, I2C, ADC, WDT, TIMER, PAD, PVTC, and Share SRAM. （b） Turn off SYS_PLL and switch AUDIO_PLL clock to 884.736MHz. d) Shield interrupts of E902 except for wakeup interrupts sent from PMU to prevent false wakeup. e) Configure PMU and not shield necessary wakeup interrupt sources, for example, only enable GPIO, RTC and VAD wakeup sources. f) Configure PMU and initiate E902 clock gate request. g) Execute the WFI instruction.

6.4.2.2.2.2 Exit the HW-VAD Mode

No.	Operation Process
①	**After receiving a wakeup request, AONSYS performs the following operations:** a) After PMU receives a wakeup interrupt, turn on the clock of E902. b) E902 clears PMU interrupts and shield PMU wakeup interrupt sources. c) Not shield E902 interrupts. d) E902 turn on the clocks of AONSYS modules. （a） Enable IO of OSC_CLK. （b） Turn on SYS_PLL. （c） Turn on the clocks of UART, I2C, ADC, WDT, TIMER, PAD, PVTC and Share SRAM. e) E902 configures AONSYS clock to AUDIO_PLL. （a） Switch the clock to 1 frequency division. （b） Switch the clock to AUDIO_PLL. （c） Configure RC to the high frequency mode. f) E902 turns on AUDIO clocks: （a） Turn on clkgen_audio_subsys_sys_pll. （b） Turn on clkgen_audio_subsys_aclk_cp2sram. （c） Switch clkgen_audio_subsys_sys_pll to audio_pll_foutvco. （d） Switch clkgen_audio_subsys_aclk_cp2sram to audio_pll_foutvco. （e） Switch share_sram_clk to audio_pll_foutvco.
②	**After powering up AP, CPU and DDR, E902 performs the following operations:** a) Configure 1.5MB Share SRAM to exit the SD or DSLP mode. b) Control the external PMIC to power up C910, DDR and AP in sequence, and ensure that the power supply is stable before performing subsequent operations. c) Configure board level components to exit the low power mode. d) Release the input isolator signals of USB PHY, C910 TOP and AON. e) Configure C910 dual-rail Memory to exit the SD mode. f) Release the input isolator signal of DDR and release DDR reset. g) Turn on AP clock and release AP reset. h) Release 1.5M SRAM AXI Port reset and PVTC reset.
③	**C910 checks whether it is a low power wakeup through BootRom.** a) Read the STR_INDICATOR register and checks whether it is a low power wakeup. b) Configure the STR_INDICATOR register and delete the hot start flag.
④	**C910 controls DDR to exit the self-refresh mode through Uboot.**

No.	Operation Process
⑤	**Start C910 slave core** a) C910 master core set the reset start address of the core to be waked up. b) C910 master core releases the reset signal of the core. c) The core executes the initialization program, enables the SMPEN bit and performs initialization operations such as enabling MMU and DCACHE.

6.4.2.2.3 STANDBY

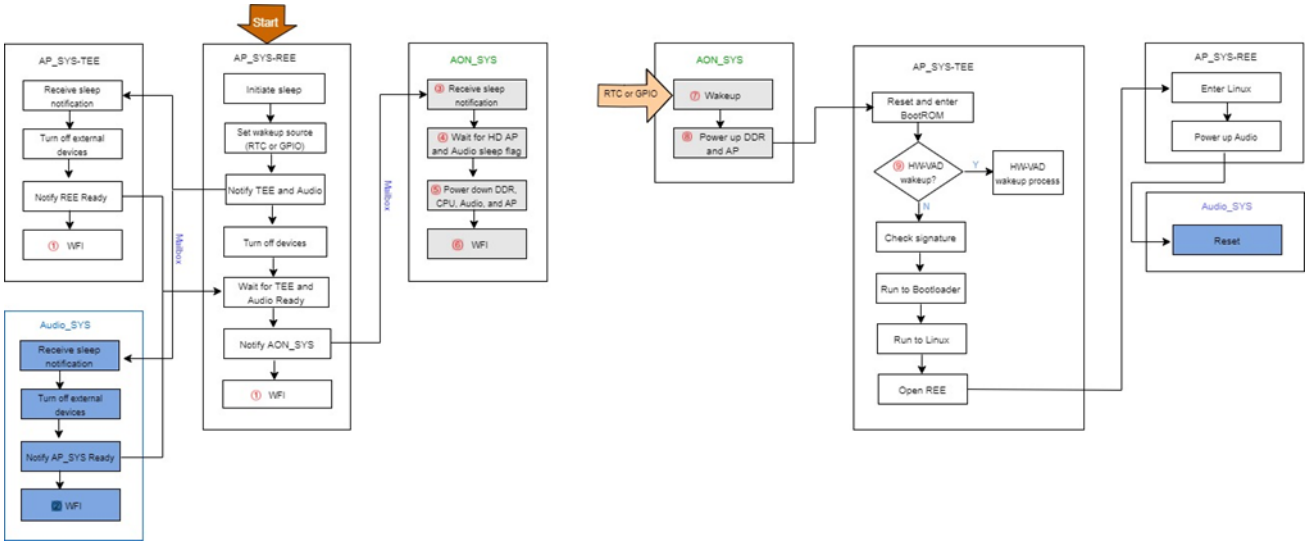


Figure & Table 6-12 STANDBY sleep and wakeup flowchart

6.4.2.2.3.1 Enter the STANDBY Mode

No.	Operation Process
①	**C910 slave core executes the core power down process (Refer to *"C910MP Power Management SPECV1.6"*)** a) Shield all interrupt requests of the core, including external interrupt, soft interrupt, and timer interrupt. Disable the interrupt enable bits MIE and SIE of MSTATUS and SSTATUS registers and the interrupt enable bits of MIE and SIE registers. b) Disable data prefetch. c) Execute INV&CLR D-Cache ALL and write dirty line back to L2C. d) Disable D-Cache. (No store instruction between cache clear and cache disable) e) Disable the core snoop enable register to shield snoop on the core. f) Execute fence iorw and iorw instructions. g) Set the deep sleep mode register provided for the core in the system. h) Execute the low power instruction WFI and enter the low power mode.

No.	Operation Process
②	**C910 master core executes the core power down process (Refer to "*C910MP Power Management SPECV1.6*")** a) Shield all interrupt requests of the core, including external interrupt, soft interrupt, and time interrupt. Disable the interrupt enable bits MIE and SIE of MSTATUS and SSTATUS registers and the interrupt enable bits of MIE and SIE registers. b) Disable data prefetch. c) Execute dcache inv&clr all. d) Disable Dcache. e) Disable the SMPEN bit of the core. f) Execute fence iorw and iorw instructions. g) Set the deep sleep mode register provided for the master core in the system. h) Execute the low power instruction WFI and enter the low power mode.
③	**C906 enters the low power mode (WFI)**
④	**E902 receives sleep notification (Mailbox)**
⑤	**E902 waits for sleep flags of C910 and C906, and performs the following operations:** a) Read that the lpmd_b register of C910 and C906 is in low power mode. b) Set the debug shield control bit. c) Send pad_cpu_l2cache_flush_req to C910. d) Wait C910 returns cpu_pad_l2cache_flush_done. e) Pull pad_cpu_l2cache_flush_req low. f) Pull cpu_pad_l2cache_flush_done low. g) Wait C910 returns cpu_pad_no_op. h) Activate the SD signal of C910 dual-rail Memory.
⑥	**Before powering down DDR, CPU, AP and AUDIO, E902 needs to perform the following operations:** a) Control DDR to enter the self-refresh mode. b) Enable DDR reset (DDR clock off) and activate the input isolator signal of DDR. c) Enable AP reset and turn off AP clock. d) Activate the input isolator signals of USB PHY, C910 TOP, and AON. e) Configure the STR_INDICATOR register and mark hot start. f) Configure board level components to enter the low power mode. g) Configure 1.5MB Share SRAM to enter the SD or DSLP mode. h) Enable 1.5M SRAM AXI Port reset and PVTC reset. i) Control the external PMIC to power down AP, DDR and C910 in sequence. j) Turn off the Audio Power Switch.

No.	Operation Process
⑦	**Before executing WFI, E902 needs to perform the following operations:** a) Configure AONSYS clock to enter the RC low frequency mode: （a） Configure RC to the low frequency mode. （b） Switch the clock to RC FOUT. （c） Switch the clock to 8 frequency division. b) Turn off unnecessary AONSYS clocks: （a） Turn off the clocks of UART, I2C, ADC, WDT, TIMER, PAD, PVTC and Share SRAM. （b） Turn off AUDIO_PLL and SYS_PLL. （c） Disable IO of OSC_CLK. c) Shield E902 interrupts except for wakeup interrupts sent by PMU to prevent false wakeup. d) Configure PMU and not shield necessary wakeup interrupt sources, for example, only enable GPIO and RTC wakeup sources. e) Configure PMU and initiate E902 clock gate request. f) Execute the WFI instruction.

6.4.2.2.3.2 Exit the STANDBY Mode

No.	Operation Process
①	**After receiving a wakeup request, AONSYS performs the following operations:** a) After PMU receives a wakeup interrupt, turn on the clock of E902. b) E902 clears PMU interrupts and shields PMU wakeup interrupt sources. c) Not shield E902 interrupts. d) E902 turns on the clocks of AONSYS modules. （a） Enable IO of OSC_CLK. （b） Turn on AUDIO_PLL and SYS_PLL. （c） Turn on the clocks of UART, I2C, ADC, WDT, TIMER, PAD, PVTC and Share SRAM. e) E902 configures AONSYS clock to AUDIO_PLL. （a） Switch the clock to 1 frequency division. （b） Switch the clock to AUDIO_PLL. （c） Configure RC to the high frequency mode.

No.	Operation Process
②	**After powering up AP, CPU and DDR, E902 performs the following operations:** a) Configure 1.5MB Share SRAM to exit the SD or DSLP mode. b) Control the external PMIC to power up C910, DDR and AP and ensure that the power supply is stable before performing subsequent operations. c) Configure board level components to exit the low power mode. d) Release the input isolator signals of USB PHY, C910 TOP and AON. e) Configure C910 dual-rail Memory to exit the SD mode. f) Release the input isolator signal of DDR and release DDR reset. g) Turn on AP clock and release AP reset. h) Release 1.5M SRAM AXI Port reset and PVTC reset. i) Turn on the Audio Power Switch.
③	**C910 checks whether it is a low power wakeup through BootRom.** a) Read STR_INDICATOR register and check whether it is a low power wakeup. b) Configure the STR_INDICATOR register and delete the hot start flag.
④	**C910 controls DDR to exit the self-refresh mode through the kernel.**
⑤	**Start C910 slave core.** a) C910 master core sets the reset start address of the core to be waked up. b) C910 master core releases the reset signal of the core. c) The core executes the initialization program, enables the SMPEN bit and performs initialization operations such as enabling MMU and DCACHE.
⑥	**Start C906.** a) Load C906 start code. b) Configure the reset start address of C906. c) Turn on C906 clock. d) Release C906 reset.

6.4.2.2.4 DVFS

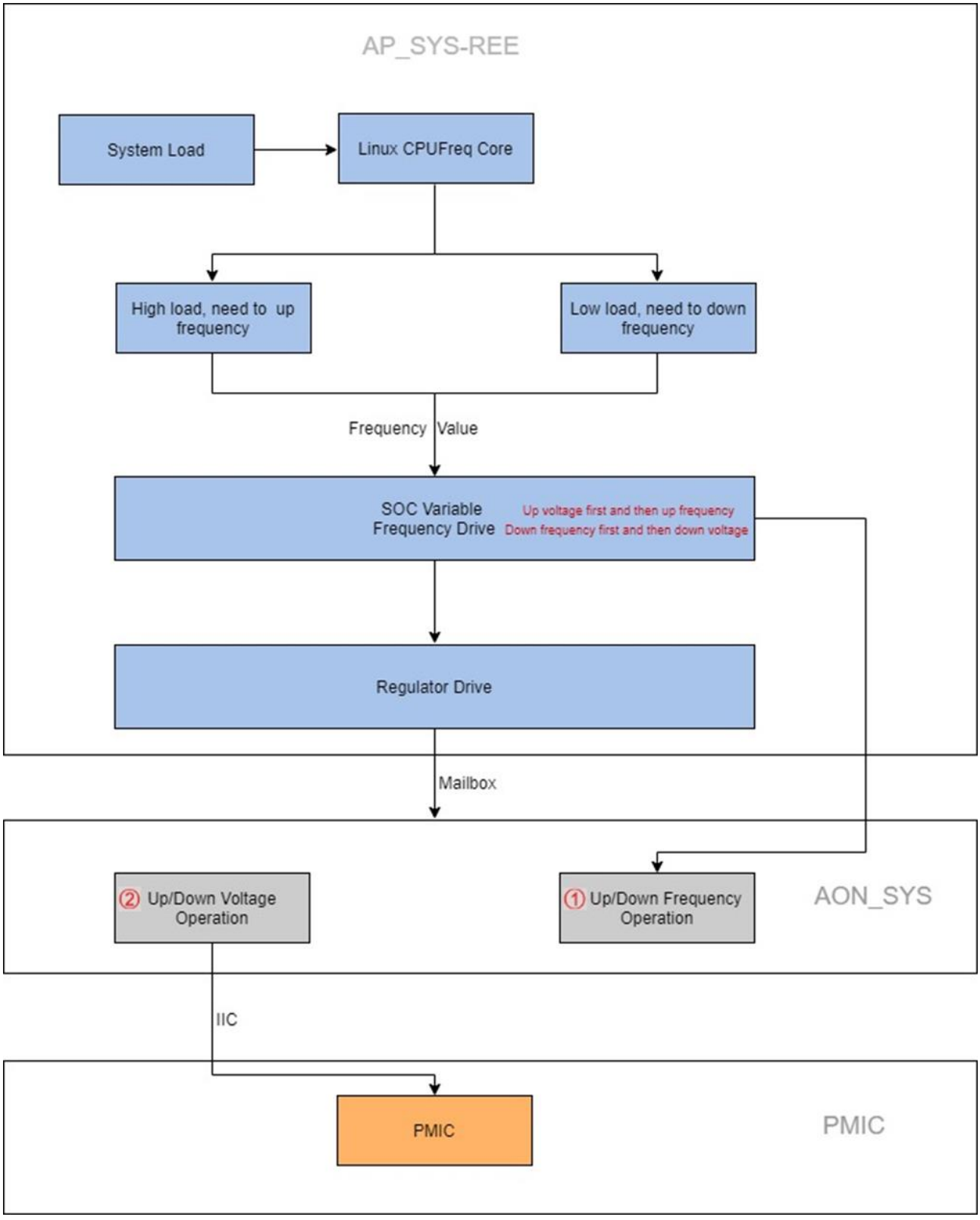


Figure & Table 6-13 DVFS flowchart

① Software configures and switches two CPU PLLs to change frequency.

② Regulate voltage according to the selected PMIC step, such as 20mV/step.
During the DVFS process, C910 supports idle and active modes. DVDD_CPU cannot be 50 mV larger than DVDDM_CPU.

6.4.2.3 Block Power Up/Power Down

Block power up/power down supports hardware mode and software mode.

6.4.2.3.1 Hardware Mode

In the hardware mode, power up, power down and isolation of the module are controlled by the hardware state machine. The configuration process is as follows:

Module power down sequence is as follows:

① CPU requests the rst_mgr module to enable Module reset.
② CPU requests the clk_mgr module to turn off Module clock.
③ CPU requests PMU to power down Module.
④ PMU pulls pd_iso_en high and requests to enable Isolation Clamp.
⑤ PMU waits for a while.
⑥ PMU pulls pd_sw_en[0] high and requests to power down Module Part One.
⑦ PMU checks pd_sw_ack[0] until Module Part One is powered down.
⑧ PMU waits for a while.
⑨ PMU pulls pd_sw_en[1] high and requests to power down the remaining part of Module.
⑩ PMU checks pd_sw_ack[1] until the remaining part of Module is powered down.
⑪ PMU sets the Module power down done Status Register and sends interrupt to CPU.

Module power on sequence is as follows:

① CPU requests the rst_mgr module to reset Module.
② CPU requests PMU to power up Module.
③ PMU pull pd_sw_en[0] low and requests to power up Module Part One.
④ PMU checks pd_sw_ack[0] until Module Part One is powered up.
⑤ PMU waits for a while.
⑥ PMU pulls pd_sw_en[1] low and requests to power up the remaining part of Module.
⑦ PMU checks pd_sw_ack[1] until the remaining part of Module is powered up.
⑧ PMU waits for a while.
⑨ PMU pulls pd_iso_en low and requests to disable Isolation Clamp.
⑩ PMU waits for a while.
⑪ PMU sets the Module power up done Status Register and sends interrupt to CPU.
⑫ After receiving Module power up done interrupt, CPU requests the clk_mgr module to turn on Module clock.
⑬ CPU requests the rst_mgr module to release Module reset.

6.4.2.3.2 Software Mode

The hardware state machine is not required in software mode. Power up, power down and isolation of Module are controlled by software. The configuration process is as follows:

Module power down sequence is as follows:

① CPU requests the rst_mgr module to reset Module.
② CPU requests the clk_mgr module to power down Module clock.
③ CPU writes the PD_ISO_EN_SET register to enable isolation. Each Module occupies 1 bit, writes 1.
④ CPU writes the PD_SW_EN_SET register to enable Module power down. Each Module occupies 2 bits, writes 1 to the 2 bits.
⑤ CPU checks the PD_SW_ACK register. Each Module occupies 2 bits. Read the 2 bits as 0, indicating Module power down is done.

Module Power Up sequence is as follows:

① CPU requests the rst_mgr module to reset Module.
② CPU writes the PD_SW_EN_CLR register to enable Module power up. Each module occupies 2 bits, writes 1 to the 2 bits.
③ CPU checks the PD_SW_ACK register. Each Module occupies 2 bits. Read the 2 bits as 1, indicating Module power up is done.
④ CPU writes the PD_ISO_EN_CLR register to release isolation. Each Module occupies 1 bit, writes 1.
⑤ CPU requests the clk_mgr module to turn on Module clock.
⑥ CPU requests the rst_mgr module to release Module reset.

6.5 Register Description

6.5.1 Register Memory Map

6.5.1.1 AO_PMU

Register	Offset	Description	Section/Page
PMU_CFG	0x0	PMU configuration register	6.5.2.1.1/595
GPIO_INT_MASK_CFG	0x10	GPIO wakeup source shield register, reserved, not used by software	6.5.2.1.2/596
INTC_INT_MASK_CFG_L	0x14	Interrupt wake source shield register, lower 32 bits	6.5.2.1.3/597
INTC_INT_MASK_CFG_H	0x18	Interrupt wake source shield register, upper 32 bits	6.5.2.1.4/597
GPIO_INT_POLARITY_CFG	0x20	GPIO wakeup source polarity configuration	6.5.2.1.5/597

Register	Offset	Description	Section/Page
		register, reserved, not used by software	
PMU_INT_CLR_CFG	0x28	Wakeup interrupt clear register	6.5.2.1.6/598
GPIO_INT_STS	0x30	GPIO wakeup source status register, reserved, not used by software	6.5.2.1.7/598
INTC_INT_STS_L	0x34	Interrupt wake source status register, lower 32 bits	6.5.2.1.8/598
INTC_INT_STS_H	0x38	Interrupt wake source status register, upper 32 bits	6.5.2.1.9/598
PMU_STATUS_L	0x40	PMU status register, lower 32 bits	6.5.2.1.10/599
PMU_STATUS_H	0x44	PMU status register, upper 32 bits	6.5.2.1.11/599
WAIT_CNT	0x50	Reset counter, reserved, not used by software	6.5.2.1.12/600
PD_CPU_SW_CNT	0x54	Power up and down delay counter, reserved, not used by software	6.5.2.1.13/600
PD_CPU_INTV_CNT	0x58	Isolation delay counter, reserved, not used by software	6.5.2.1.14/600
PD_SW_POLARITY	0x5c	Power switch feedback polarity register, reserved, not used by software	6.5.2.1.15/601
PMU_RESERVED_REG_0	0x60	Reserved register 0	6.5.2.1.16/601
PMU_RESERVED_REG_1	0x64	Reserved register 1	6.5.2.1.17/601
PMU_RESERVED_REG_3	0x6c	Reserved register 2	6.5.2.1.18/602

6.5.1.2 AO_SYSREG

Register	Offset	Description	Section/Page
CPU_LP_MODE	0x00	CPU low power mode register	6.5.2.2.1/602
CHIP_LP_MODE	0x04	SoC low power mode register	6.5.2.2.2/603
AO_SERAM_TRN	0x10	AO_SERAM scrambler register	6.5.2.2.3/603
AO_SERAM_INT	0x14	AO_SERAM interrupt register	6.5.2.2.4/603
STR_SERAM_TRN	0x18	STR_SERAM scrambler register	6.5.2.2.5/604
STR_SERAM_INT	0x1c	STR_SRAM interrupt register	6.5.2.2.6/604
STR_INDICATOR_0	0x20	Low power startup marker register 0	6.5.2.2.7/604
STR_INDICATOR_1	0x24	Low power startup marker register 1	6.5.2.2.8/604

Register	Offset	Description	Section/Page
STR_INDICATOR_2	0x28	Low power startup marker register 2	6.5.2.2.9/604
STR_INDICATOR_3	0x2c	Low power startup marker register 3	6.5.2.2.10/605
PVTC_WR_LOCK	0x30	PVTC write lock	6.5.2.2.11/605
PVTC_TS_ALARM	0x34	Temperature monitoring alarm register	6.5.2.2.12/605
PVTC_VM_ALARM	0x38	Voltage monitoring alarm register	6.5.2.2.13/606
PVTC_PD_ALARM	0x3c	Process monitoring alarm register	6.5.2.2.14/606
E902_CNT_CLR	0x40	E902 timer counter clears register	6.5.2.2.15/606
E902_RST_ADDR	0x44	E902 reset start address register	6.5.2.2.16/606
C906_RST_ADDR_L	0x48	C906 reset start address register, lower 32 bits	6.5.2.2.17/607
C906_RST_ADDR_H	0x4c	C906 reset start address register, upper 32 bits	6.5.2.2.18/607
RESERVED_REG_0	0x50	Reserve register 0 for STR ADDR, upper 32 bits	6.5.2.2.19/607
RESERVED_REG_1	0x54	Reserve register 1 for STR ADDR, lower 32 bits	6.5.2.2.20/607
RESERVED_REG_2	0x58	Reserved register 2	6.5.2.2.21/608
RESERVED_REG_3	0x5c	Reserved register 3	6.5.2.2.22/608
AON_AHB_ADEXT	0x60	AON AHB address extension register	6.5.2.2.23/608
RC_EN	0x70	RC enable register	6.5.2.2.24/608
RC_FCAL	0x74	RC calibration register	6.5.2.2.25/609
RC_MODE	0x78	RC mode register	6.5.2.2.26/609
RC_READY	0x7c	RC ready register	6.5.2.2.27/609
ISO_CFG	0x80	ISO control register	6.5.2.2.28/610
OCRAM_ERR	0x90	OCRAM check error register	6.5.2.2.29/610
TIMER_LINK	0x100	Timer link register	6.5.2.2.30/610
PD_REQ	0x110	Module power up and down request register	6.5.2.2.31/611
PD_ISO_EN_SET	0x114	Module ISO enable register	6.5.2.2.32/612
PD_ISO_EN_CLR	0x118	Module ISO clear register	6.5.2.2.33/612

Register	Offset	Description	Section/Page
PD_SW_EN_SET	0x11c	Module power down enable register	6.5.2.2.34/613
PD_SW_EN_CLR	0x120	Module power-on enabling register	6.5.2.2.35/613
PD_SW_ACK	0x124	Module power up and down feedback register	6.5.2.2.36/614
PD_SW_CNT_EN	0x128	Module power up and down feedback wait count enable register	6.5.2.2.37/615
PD_FSM_RST	0x12c	Module PMU state machine reset register	6.5.2.2.38/615
PD_INT_MASK	0x130	Module PMU interrupt shield register	6.5.2.2.39/616
PD_FSM_STS_L	0x134	Module PMU state machine status register, lower 32 bits	6.5.2.2.40/617
PD_FSM_STS_H	0x138	Module PMU state machine status register, upper 32 bits	6.5.2.2.41/617
PD_INT_STS	0x13c	Module PMU interrupt status register	6.5.2.2.42/618
PD_INT_CLR	0x140	Module PMU interrupt clear register	6.5.2.2.43/618
PD_BLK0_SW_CNT	0x144	Modular down/up feedback wait count register 0	6.5.2.2.44/619
PD_BLK1_SW_CNT	0x148	Modular down/up feedback wait count register 1	6.5.2.2.45/619
PD_BLK2_SW_CNT	0x14c	Modular down/up feedback wait count register 2	6.5.2.2.46/620
PD_BLK3_SW_CNT	0x150	Modular down/up feedback wait count register3	6.5.2.2.47/620
PD_BLK4_SW_CNT	0x154	Modular down/up feedback wait count register 4	6.5.2.2.48/620
PD_BLK5_SW_CNT	0x158	Modular down/up feedback wait count register 5	6.5.2.2.49/621
PD_BLK6_SW_CNT	0x15c	Modular down/up feedback wait count register 6	6.5.2.2.50/621
PD_BLK7_SW_CNT	0x160	Modular down/up feedback wait count register 7	6.5.2.2.51/621
PD_BLK8_SW_CNT	0x164	Modular down/up feedback wait count register 8	6.5.2.2.52/622
PD_BLK9_SW_CNT	0x168	Modular down/up feedback wait count register 9	6.5.2.2.53/622

Register	Offset	Description	Section/Page
PD_BLK10_SW_CNT	0x16c	Modular down/up feedback wait count register 10	6.5.2.2.54/623
PD_BLK0_INTV_CNT	0x180	Module PMU state transition wait count register 0	6.5.2.2.55/623
PD_BLK1_INTV_CNT	0x184	Module PMU state transition wait count register 1	6.5.2.2.56/623
PD_BLK2_INTV_CNT	0x188	Module PMU state transition wait count register 2	6.5.2.2.57/624
PD_BLK3_INTV_CNT	0x18c	Module PMU state transition wait count register 3	6.5.2.2.58/624
PD_BLK4_INTV_CNT	0x190	Module PMU state transition wait count register 4	6.5.2.2.59/625
PD_BLK5_INTV_CNT	0x194	Module PMU state transition wait count register 5	6.5.2.2.60/625
PD_BLK6_INTV_CNT	0x198	Module PMU state transition wait count register 6	6.5.2.2.61/625
PD_BLK7_INTV_CNT	0x19c	Module PMU state transition wait count register 7	6.5.2.2.62/626
PD_BLK8_INTV_CNT	0x1a0	Module PMU state transition wait count register 8	6.5.2.2.63/626
PD_BLK9_INTV_CNT	0x1a4	Module PMU state transition wait count register 9	6.5.2.2.64/627
PD_BLK10_INTV_CNT	0x1a8	Module PMU state transition wait count register 10	6.5.2.2.65/627
AUDIO_PMU_REQ	0x1f8	AUDIO->E902 request register	6.5.2.2.66/628
AUDIO_PMU_STS	0x1fc	AUDIO->E902 request register	6.5.2.2.67/628
AUDIO_PMU_INTR	0x204	AUDIO->E902 request register	6.5.2.2.68/628
PMU_AUDIO_REQ	0x208	E902->AUDIO request register	6.5.2.2.69/629
PMU_AUDIO_STS	0x20c	E902->AUDIO request register	6.5.2.2.70/629
MEM_LP_MODE	0x210	Memory low power mode register	6.5.2.2.71/629
C910_DBG_MASK	0x214	C910 debug shield register	6.5.2.2.72/631
C910_L2CACHE	0x218	C910 L2CACHE flush register	6.5.2.2.73/631
BISR_CTRL	0x220	Reserved, not used	6.5.2.2.74/632

Register	Offset	Description	Section/Page
EFUSE_PRELOAD_DONE	0x224	eFuse preload completion status register	6.5.2.2.75/632
GPIO_RTE	0x228	Reserved, not used	6.5.2.2.76/632
PLL_DSKEW_LOCK	0x22c	PLL calibration lock register	6.5.2.2.77/633
SRAM_AXI_CFG	0x230	SRAM_AXI configuration register	6.5.2.2.78/633
SRAM_AXI_ST	0x234	SRAM_AXI configuration register	6.5.2.2.79/634
SRAM_AXI_ERR_STS_0	0x238	SRAM_AXI check error register 0	6.5.2.2.80/634
SRAM_AXI_ERR_STS_1	0x23c	SRAM_AXI check error register 1	6.5.2.2.81/634
SRAM_AXI_ERR_STS_2	0x240	SRAM_AXI check error register 2	6.5.2.2.82/635
SRAM_AXI_ERR_STS_3	0x244	SRAM_AXI check error register 3	6.5.2.2.83/635
SRAM_AXI_ERR_STS_4	0x248	SRAM_AXI check error register 4	6.5.2.2.84/635
SE_MUX_LOCK	0x24c	Secure IO MUX lock register	6.5.2.2.85/635
CPU_DBG_DIS_LOCK	0x270	CPU debug lock disable register	6.5.2.2.86/636
RESERVED_REG_4	0x300	RESERVED_REG_4	6.5.2.2.87/636
RESERVED_REG_5	0x304	RESERVED_REG_5	6.5.2.2.88/636
RESERVED_REG_6	0x308	RESERVED_REG_6	6.5.2.2.89/636
RESERVED_REG_7	0x30c	RESERVED_REG_7	6.5.2.2.90/637
RESERVED_REG_8	0x400	RESERVED_REG_8	6.5.2.2.91/637
RESERVED_REG_9	0x404	RESERVED_REG_9	6.5.2.2.92/637
RESERVED_REG_10	0x408	RESERVED_REG_10	6.5.2.2.93/637
RESERVED_REG_11	0x40c	RESERVED_REG_11	6.5.2.2.94/638
RESERVED_REG_12	0x500	RESERVED_REG_12	6.5.2.2.95/638
RESERVED_REG_13	0x504	RESERVED_REG_13	6.5.2.2.96/638
RESERVED_REG_14	0x508	RESERVED_REG_14	6.5.2.2.97/638
RESERVED_REG_15	0x50c	RESERVED_REG_15	6.5.2.2.98/638
RESERVED_REG_16	0x600	RESERVED_REG_16	6.5.2.2.99/639
RESERVED_REG_17	0x604	RESERVED_REG_17	6.5.2.2.100/639
RESERVED_REG_18	0x608	RESERVED_REG_18	6.5.2.2.101/639
RESERVED_REG_19	0x60c	RESERVED_REG_19	6.5.2.2.102/639

6.5.2 Register and Field Description

6.5.2.1 AO_PMU

6.5.2.1.1 PMU_CFG

- Description: PMU configuration register
- Offset: 0x0
- Default Value: 0x5000

Bits	Field Name	Access	Description
[31:17]	RESERVED_2	-	
[16]	PD_FLAG	RW	When chip cold power on, the flag is reset to 0. Before CPU enters power down mode, CPU should set the flag to differentiate cold power on. Value After Reset: 0x0
[15]	BUS_CLKEN	RW	CPU bus clock enable.（apsys）if disabled, CPU PMU will control CPU bus clock and core clock simultaneously. If enabled, CPU bus clock can't be changed by CPU PMU. Value After Reset: 0x0
[14]	BUS_CLKON_WR	RW	CPU bus clock on, used for bypass mode and bus_clken is set. Value After Reset: 0x1
[13]	PD_SW_WAIT_CNT_EN	RW	Power down/power up ack wait count enable If enabled, CPU PMU FSM will ignore pd_sw_ack signal from CPU block and use internal ack generated by register PD_CPU_SW_CNT. Value After Reset: 0x0
[12]	CLK_ON	RW	Clock on, used for bypass mode. Value After Reset: 0x1
[11:8]	CLK_SEL	RW	Clock_switch. [11:10]: not used, [9:8]: 0: cpu_pll 1: cpu_pll/2 2: cpu_pll/4 3: pmu_clk Value After Reset: 0x0
[7]	BUS_RST_EN	RW	CPU bus reset enable.(ap_sys) If enabled, CPU PMU will assert/release CPU core reset

Bits	Field Name	Access	Description
			and bus reset simultaneously. If disabled, CPU PMU just assert/release CPU. Value After Reset: 0x0
[6]	RESERVED_1	-	
[5:3]	MODE	RW	Low power mode, used for low power state change securely. 0: Clock switch 1: Clock gate, ---> stop_mode 2: CPU PLL frequency update 3: CPU PLL power down 4: CPU power down 5 : CPU and PLL power down, --->ext_mode Value After Reset: 0x0
[2]	BYPASS	RW	Low power bypass mode If set, PMU will bypass configuration values to clock gate/clock switch/PLL directly and don't execute low power state change securely. Bypass mode can be used for fast clock switch. Value After Reset: 0x0
[1]	REQ	WC	Low power request, auto cleared by hardware. Value After Reset: 0x0
[0]	EXIT	WC	Low power exit, auto cleared by hardware. If CPU has sent low power request, CPU can set this bit to exit low power before wait/stop instruction. Value After Reset: 0x0

6.5.2.1.2 GPIO_INT_MASK_CFG

- Description: GPIO wakeup source shield register, reserved, not used by software
- Offset: 0x10
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	GPIO_INT_MASK	RW	Bitmap mask for 3 pad GPIO wakeup interrupt source. 0: Enable interrupt. 1: Disable interrupt.

Bits	Field Name	Access	Description
			Value After Reset: 0xFFFF

6.5.2.1.3 INTC_INT_MASK_CFG_L

- Description: Interrupt wake source shield register, lower 32 bits
- Offset: 0x14
- Default Value: 0xffffffff

Bits	Field Name	Access	Description
[31:0]	INTC_INT_MASK_L	RW	Mask for intc wakeup interrupt source 1: Enable interrupt. 0: Disable interrupt. Value After Reset: 0xFFFFFFFF

6.5.2.1.4 INTC_INT_MASK_CFG_H

- Description: Interrupt wake source shield register, upper 32 bits
- Offset: 0x18
- Default Value: 0xffffffff

Bits	Field Name	Access	Description
[31:0]	INTC_INT_MASK_H	RW	Mask for intc wakeup interrupt source 1: Enable interrupt. 0: Disable interrupt. Value After Reset: 0xFFFFFFFF

6.5.2.1.5 GPIO_INT_POLARITY_CFG

- Description: GPIO wakeup source polarity configuration register, reserved, not used by software
- Offset: 0x20
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	INT_POL	RW	Bitmap polarity for 3 pad GPIO wakeup interrupt source 1: Active high 0: Active low Value After Reset: 0xFFFF

6.5.2.1.6 PMU_INT_CLR_CFG

- Description: Wakeup interrupt clear register
- Offset: 0x28
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_CLR	WC	Wakeup interrupt clear, auto cleared by hardware. Value After Reset: 0x0

6.5.2.1.7 GPIO_INT_STS

- Description: GPIO wakeup source status register, reserved, not used by software
- Offset: 0x30
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	GPIO_INT	RO	Bitmap for 3 pad GPIO wakeup interrupt status Value After Reset: 0x0

6.5.2.1.8 INTC_INT_STS_L

- Description: Interrupt wake source status register, lower 32 bits
- Offset: 0x34
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	INTC_INT_L	RO	INTC wakeup interrupt status Value After Reset: 0x0

6.5.2.1.9 INTC_INT_STS_H

- Description: Interrupt wake source status register, upper 32 bits
- Offset: 0x38
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	INTC_INT_H	RO	INTC wakeup interrupt status Value After Reset: 0x0

6.5.2.1.10 PMU_STATUS_L

- Description: PMU status register, lower 32 bits
- Offset: 0x40
- Default Value: 0x30

Bits	Field Name	Access	Description
[31:28]	RESERVED_3	-	
[27:12]	CNT	RO	CPU PMU internal counter Value After Reset: 0x0
[11:8]	FSM	RO	CPU PMU FSM state Value After Reset: 0x0
[7:6]	RESERVED_2	-	
[5]	BUS_CLKON_RD	RO	CPU bus clk on (ap_sys) Value After Reset: 0x1
[4]	CLKON	RO	CPU core clk on Value After Reset: 0x1
[3:0]	RESERVED_1	-	

6.5.2.1.11 PMU_STATUS_H

- Description: PMU status register, upper 32 bits
- Offset: 0x44
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:6]	RESERVED_2	-	
[5:4]	CPU_LPMD_B	RO	CPU LP mode 00: Stop 01: Wait 10: Doze 11: Normal Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	CPU_WAKEUP	RO	CPU wake up when it is 1. Value After Reset: 0x1

6.5.2.1.12 WAIT_CNT

- Description: Reset counter, reserved, not used by software
- Offset: 0x50
- Default Value: 0x108c6467

Bits	Field Name	Access	Description
[31:24]	PD_RST_CNT	RW	Power down/up reset wait counter Value After Reset: 0x10
[23:16]	RST_CNT	RW	PLL reset wait counter Value After Reset: 0x8C
[15]	RESERVED_1	-	
[14:10]	PD_CNT	RW	CPU reset's enable counter Value After Reset: 0x19
[9:5]	GATE_CNT	RW	The CNT value determines the following two factors: 1. CPU clock gating enablement --> CPU clock switching/wait interrupt/PLL reset (or power off) enablement/CPU reset enabled interval count value. 2. CPU Clock Gating does not enable --> CPU reset enable interval count value; Clock gate wait counter. Value After Reset: 0x3
[4:0]	SWITCH_CNT	RW	CPU clock switch counter Value After Reset: 0x7

6.5.2.1.13 PD_CPU_SW_CNT

- Description: Power up and down delay counter, reserved, not used by software
- Offset: 0x54
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	PD_CPU_SW_CNT	RW	CPU power down/up ack wait counter Used when PMU_CFG[13] is set. Value After Reset: 0xFFFF

6.5.2.1.14 PD_CPU_INTV_CNT

- Description: Isolation delay counter, reserved, not used by software
- Offset: 0x58

- Default Value: 0xffffff

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:12]	ISO_WAIT_CNT	RW	Wait counter between isolation state and clock on state for power up sequencer Value After Reset: 0xFFF
[11:0]	ISO_SW_WAIT_CNT	RW	Wait counter between isolation state and power up/down state. Value After Reset: 0xFFF

6.5.2.1.15 PD_SW_POLARITY

- Description: Power switch feedback polarity register, reserved, not used by software
- Offset: 0x5c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	PD_SW_ACK_POLARITY	RW	Power switch feedback signal polarity control 0: Active low 1: Active high Value After Reset: 0x0
[0]	PD_SW_EN_POLARITY	RW	Power switch enable signal polarity control 0: Active low 1: Active high Value After Reset: 0x0

6.5.2.1.16 PMU_RESERVED_REG_0

- Description: Reserved register 0
- Offset: 0x60
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PMU_RESERVED_REG_0	RW	Reserved register 0 Value After Reset: 0x0

6.5.2.1.17 PMU_RESERVED_REG_1

- Description: Reserved register 1

- Offset: 0x64
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PMU_RESERVED_REG_1	RW	Reserved register 1 Value After Reset: 0x0

6.5.2.1.18 PMU_RESERVED_REG_2

- Description: Reserved register 2
- Offset: 0x6c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PMU_RESERVED_REG_2	RW	Reserved register 2 Value After Reset: 0x0

6.5.2.2 AO_SYSREG

6.5.2.2.1 CPU_LP_MODE

- Description: CPU low power mode register
- Offset: 0x00
- Default Value: 0x3ff

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9:8]	C906_CORE_LPMD_B	RO	C906 CORE0 low power mode register 00/01/10: Low power mode 11: Normal mode Value After Reset: 0x3
[7:6]	C910_CORE3_LPMD_B	RO	C910 CORE3 low power mode register 00/01/10: Low power mode 11: Normal mode Value After Reset: 0x3
[5:4]	C910_CORE2_LPMD_B	RO	C910 CORE2 low power mode register 00/01/10: Low power mode 11:Normal mode Value After Reset: 0x3
[3:2]	C910_CORE1_LPMD_B	RO	C910 CORE1 low power mode register

Bits	Field Name	Access	Description
			00/01/10: Low power mode 11: Normal mode Value After Reset: 0x3
[1:0]	C910_CORE0_LPMD_B	RO	C910 CORE0 low power mode register 00/01/10: Low power mode 11: Normal mode Value After Reset: 0x3

6.5.2.2.2 CHIP_LP_MODE

- Description: SoC low power mode register
- Offset: 0x04
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	CHIP_LP_MODE	RW	SoC low power mode register, used by software to mark the low power state of the chip, mode customization. Value After Reset: 0x0

6.5.2.2.3 AO_SERAM_TRN

- Description: AO_SERAM scrambler register
- Offset: 0x10
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	AO_SERAM_TRN	RW	AO_SERAM scrambling key Value After Reset: 0x0

6.5.2.2.4 AO_SERAM_INT

- Description: AO_SRAM interrupt register
- Offset: 0x14
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	AO_SRAM_INIT	RW	AO_SERAM interrupt Value After Reset: 0x0

6.5.2.2.5 STR_SERAM_TRN

- Description: STR_SERAM scrambler register
- Offset: 0x18
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	STR_SERAM_TRN	RW	STR_SERAM scrambling key Value After Reset: 0x0

6.5.2.2.6 STR_SERAM_INT

- Description: STR_SRAM interrupt register
- Offset: 0x1c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	STR_SRAM_INIT	RW	STR_SERAM interrupt Value After Reset: 0x0

6.5.2.2.7 STR_INDICATOR_0

- Description: Low power startup marker register 0
- Offset: 0x20
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	STR_INDICATOR_0	RW	Low power start tag Value After Reset: 0x0

6.5.2.2.8 STR_INDICATOR_1

- Description: Low power startup marker register 1
- Offset: 0x24
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	STR_INDICATOR_1	RW	Low power start tag Value After Reset: 0x0

6.5.2.2.9 STR_INDICATOR_2

- Description: Low power startup marker register 2

- Offset: 0x28
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	STR_INDICATOR_2	RW	Low power start tag Value After Reset: 0x0

6.5.2.2.10 STR_INDICATOR_3

- Description: Low power startup marker register 3
- Offset: 0x2c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	STR_INDICATOR_3	RW	Low power start tag Value After Reset: 0x0

6.5.2.2.11 PVTC_WR_LOCK

- Description: PVTC write lock
- Offset: 0x30
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	PVTC_WR_LOCK	RW	PVTC write lock Value After Reset: 0x0

6.5.2.2.12 PVTC_TS_ALARM

- Description: Temperature monitoring alarm register
- Offset: 0x34
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3:2]	PVTC_TS_ALARMA	RO	Temperature monitoring alarm Value After Reset: 0x0
[1:0]	PVTC_TS_ALARMB	RO	Temperature monitoring alarm Value After Reset: 0x0

6.5.2.2.13 PVTC_VM_ALARM

- Description: Voltage monitoring alarm register
- Offset: 0x38
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	PVTC_VM_ALARMA	RO	Voltage monitoring alarm Value After Reset: 0x0
[15:0]	PVTC_VM_ALARMB	RO	Voltage monitoring alarm Value After Reset: 0x0

6.5.2.2.14 PVTC_PD_ALARM

- Description: Process monitoring alarm register
- Offset: 0x3c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:23]	RESERVED_2	-	
[22:12]	PVTC_PD_ALARMA	RO	Process monitoring alarm Value After Reset: 0x0
[11]	RESERVED_1	-	
[10:0]	PVTC_PD_ALARMB	RO	Process monitoring alarm Value After Reset: 0x0

6.5.2.2.15 E902_CNT_CLR

- Description: E902 timer counter clear register
- Offset: 0x40
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	E902_CNT_CLR	RW	E902 timer counter clear Value After Reset: 0x0

6.5.2.2.16 E902_RST_ADDR

- Description: E902 reset start address register
- Offset: 0x44

- Default Value: 0xffef8000

Bits	Field Name	Access	Description
[31:0]	E902_CPU_RST_ADDR	RW	E902 reset start address Value After Reset: 0xFFEF8000

6.5.2.2.17 C906_RST_ADDR_L

- Description: C906 reset start address register, lower 32 bits
- Offset: 0x48
- Default Value: 0xc0000000

Bits	Field Name	Access	Description
[31:0]	C906_CPU_RST_ADDR_L	RW	C906 reset start address, lower 32bits Value After Reset: 0xC0000000

6.5.2.2.18 C906_RST_ADDR_H

- Description: C906 reset start address register, upper 32 bits
- Offset: 0x4c
- Default Value: 0xff

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	C906_CPU_RST_ADDR_H	RW	C906 reset start address, upper 32 bits Value After Reset: 0xFF

6.5.2.2.19 RESERVED_REG_0

- Description: Reserve register 0 for STR ADDR, upper 32 bits
- Offset: 0x50
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_0	RW	STR address, upper 32 bits Value After Reset: 0x0

6.5.2.2.20 RESERVED_REG_1

- Description: Reserved register 1 for STR ADDR, lower 32 bits
- Offset: 0x54
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_1	RW	STR address, upper 32 bits Value After Reset: 0x0

6.5.2.2.21 RESERVED_REG_2

- Description: Reserved register 2
- Offset: 0x58
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_2	RW	RESERVED_REG_2 Value After Reset: 0x0

6.5.2.2.22 RESERVED_REG_3

- Description: Reserved register 3
- Offset: 0x5c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_3	RW	RESERVED_REG_3 Value After Reset: 0x0

6.5.2.2.23 AON_AHB_ADEXT

- Description: AON AHB address extension register
- Offset: 0x60
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9:0]	AONSYS_AHB_SPACE_SEL	RW	AON AHB address extension register Value After Reset: 0x0

6.5.2.2.24 RC_EN

- Description: RC enable register
- Offset: 0x70
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	RC_EN	RW	RC enable register Value After Reset: 0x1

6.5.2.2.25 RC_FCAL

- Description: RC calibration register
- Offset: 0x74
- Default Value: 0x77f

Bits	Field Name	Access	Description
[31:12]	RESERVED_1	-	
[11:0]	RC_FCAL	RW	RC calibration register Value After Reset: 0x77F

6.5.2.2.26 RC_MODE

- Description: RC mode register
- Offset: 0x78
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	RC_MODE	RW	RC mode register 0: Low frequency FOSC=0.9MHz to 2.0MHz 1: High frequency FOSC=24MHz to26MHz Value After Reset: 0x1

6.5.2.2.27 RC_READY

- Description: RC ready register
- Offset: 0x7c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	RC_READY	RO	RC ready register Value After Reset: 0x0

6.5.2.2.28 ISO_CFG

- Description: ISO control register
- Offset: 0x80
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	USB3_ISOLATION_EN	RW	USB3 PHY input isolation enable register Value After Reset: 0x0
[2]	DDR_ISOLATION_EN	RW	DDR input isolation enable register Value After Reset: 0x0
[1]	C910_ISOLATION_EN	RW	C910 input isolation enable register Value After Reset: 0x0
[0]	AON_ISOLATION_EN	RW	AON_ SUBSYS input isolation enable register Value After Reset: 0x0

6.5.2.2.29 OCRAM_ERR

- Description: OCRAM check error register
- Offset: 0x90
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_SERAM_ERR	RO	OCRAM check failure register Value After Reset: 0x0

6.5.2.2.30 TIMER_LINK

- Description: Timer link register
- Offset: 0x100
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	TIMER_3_4_LINK	RW	TIMER_3_4_LINK Value After Reset: 0x0
[1]	TIMER_2_3_LINK	RW	TIMER_2_3_LINK

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[0]	TIMER_1_2_LINK	RW	TIMER_1_2_LINK Value After Reset: 0x0

6.5.2.2.31 PD_REQ

- Description: Module power up and down request register
- Offset: 0x110
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:27]	RESERVED_2	-	
[26:16]	PU_REQ	W1S	Module power-on request register, hardware auto-clear 0, for module power-off hardware mode: 16: AUDIO 17: VDEC 18: NPU 19: VENC 20: GPU 21: DSP0 22: DSP1 23: C910 CORE0 24: C910 CORE1 25: C910 CORE2 26: C910 CORE3 Value After Reset: 0x0
[15:11]	RESERVED_1	-	
[10:0]	PD_REQ	W1S	Modular power-off request register, hardware auto-clear 0, for module power-off hardware mode: 0: AUDIO 1: VDEC 2: NPU 3: VENC 4: GPU 5: DSP0 6: DSP1 7: C910 CORE0

Bits	Field Name	Access	Description
			8: C910 CORE1 9: C910 CORE2 10: C910 CORE3 Value After Reset: 0x0

6.5.2.2.32 PD_ISO_EN_SET

- Description: Module ISO enable register
- Offset: 0x114
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:0]	PD_ISO_EN_SET	W1S	Module isolation enable register, hardware auto-clear 0, for module power-off software mode: 0: AUDIO 1: VDEC 2: NPU 3: VENC 4: GPU 5: DSP0 6: DSP1 7: C910 CORE0 8: C910 CORE1 9: C910 CORE2 10: C910 CORE3 Value After Reset: 0x0

6.5.2.2.33 PD_ISO_EN_CLR

- Description: Module ISO clear register
- Offset: 0x118
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:0]	PD_ISO_EN_CLR	W1S	Module isolation clear register, hardware auto clear 0 for module power down software mode: 0: AUDIO

Bits	Field Name	Access	Description
			1: VDEC 2: NPU 3: VENC 4: GPU 5: DSP0 6: DSP1 7: C910 CORE0 8: C910 CORE1 9: C910 CORE2 10: C910 CORE3 Value After Reset: 0x0

6.5.2.2.34 PD_SW_EN_SET

- Description: Module power down enable register
- Offset: 0x11c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:22]	RESERVED_1	-	
[21:0]	PD_SW_EN_SET	W1S	Module power-off enable register, hardware auto-clean 0, for module power-off software mode, each module occupies 2 bits: [1:0]: AUDIO [3:2]: VDEC [5:4]: NPU [7:6]: VENC [9:8]: GPU [11:10]: DSP0 [13:12]: DSP1 [15:14]: C910 CORE0 [17:16]: C910 CORE1 [19:18]: C910 CORE2 [21:20]: C910 CORE3 Value After Reset: 0x0

6.5.2.2.35 PD_SW_EN_CLR

- Description: Module power-on enable register

- Offset: 0x120
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:22]	RESERVED_1	-	
[21:0]	PD_SW_EN_CLR	W1S	Module power-on enable register, hardware auto-clean 0, for module power-off software mode, each module occupies 2 bits: [1:0]: AUDIO [3:2]: VDEC [5:4]: NPU [7:6]: VENC [9:8]: GPU [11:10]: DSP0 [13:12]: DSP1 [15:14]: C910 CORE0 [17:16]: C910 CORE1 [19:18]: C910 CORE2 [21:20]: C910 CORE3 Value After Reset: 0x0

6.5.2.2.36 PD_SW_ACK

- Description: Module power up and down feedback register
- Offset: 0x124
- Default Value: 0x3fffff

Bits	Field Name	Access	Description
[31:22]	RESERVED_1	-	
[21:0]	PD_SW_ACK	RO	Module power-off/power-on feedback status, each module occupies 2 bits. You must wait until both bitacks are low before performing subsequent operations. 0 means the module is in power-off mode, otherwise in power-on mode. [1:0]: AUDIO [3:2]: VDEC [5:4]: NPU [7:6]: VENC [9:8]: GPU [11:10]: DSP0

Bits	Field Name	Access	Description
			[13:12]: DSP1 [15:14]: C910 CORE0 [17:16]: C910 CORE1 [19:18]: C910 CORE2 [21:20]: C910 CORE3 Value After Reset: 0x3FFFFF

6.5.2.2.37 PD_SW_CNT_EN

- Description: Module power up and down feedback wait count enable register
- Offset: 0x128
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:22]	RESERVED_1	-	
[21:0]	PD_SW_CNT_EN	RW	Module power down/power up feedback wait count enable registers with 2 bits per module. If enabled, PMU will ignore the feedback signal from power switch and use register PD_BLKn_SW_Internal feedback signal generated by CNT. Used in hardware mode. [1:0]: AUDIO [3:2]: VDEC [5:4]: NPU [7:6]: VENC [9:8]: GPU [11:10]: DSP0 [13:12]: DSP1 [15:14]: C910 CORE0 [17:16]: C910 CORE1 [19:18]: C910 CORE2 [21:20]: C910 CORE3 Value After Reset: 0x0

6.5.2.2.38 PD_FSM_RST

- Description: Module PMU state machine reset register
- Offset: 0x12c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:0]	PD_FSM_RST	W1S	Module PMU state machine reset control, hardware auto-clear 0. 0: AUDIO 1: VDEC 2: NPU 3: VENC 4: GPU 5: DSP0 6: DSP1 7: C910 CORE0 8: C910 CORE1 9: C910 CORE2 10: C910 CORE3 Value After Reset: 0x0

6.5.2.2.39 PD_INT_MASK

- Description: Module PMU interrupt shield register
- Offset: 0x130
- Default Value: 0x3fffff

Bits	Field Name	Access	Description
[31:22]	RESERVED_1	-	
[21:0]	PD_INT_MASK	RW	Module PMU interrupt screen register, each module occupies 2 bits. 0: Unshielded 1: Shielded [1:0]: AUDIO [3:2]: VDEC [5:4]: NPU [7:6]: VENC [9:8]: GPU [11:10]: DSP0 [13:12]: DSP1 [15:14]: C910 CORE0 [17:16]: C910 CORE1

Bits	Field Name	Access	Description
			[19:18]: C910 CORE2 [21:20]: C910 CORE3 Value After Reset: 0x3FFFFF

6.5.2.2.40 PD_FSM_STS_L

- Description: Module PMU state machine status register, lower 32 bits
- Offset: 0x134
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PD_FSM_ST_L	RO	Module PMU status register, lower 32 bits, 4 bits per module. [3:0]: AUDIO [7:4]: VDEC [11:8]: NPU [15:12]: VENC [19:16]: GPU [23:20]: DSP0 [27:24]: DSP1 [31:28]: C910 CORE0 Value After Reset: 0x0

6.5.2.2.41 PD_FSM_STS_H

- Description: Module PMU state machine status register, upper 32 bits
- Offset: 0x138
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:12]	RESERVED_1	-	
[11:0]	PD_FSM_ST_H	RO	Module PMU status register, upper 32 bits, 4 bits per module. [3:0]: C910 CORE1 [7:4]: C910 CORE2 [11:8]: C910 CORE3 [31:12]: Reserved Value After Reset: 0x0

6.5.2.2.42 PD_INT_STS

- Description: Module PMU interrupt status register
- Offset: 0x13c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:22]	RESERVED_1	-	
[21:0]	PD_INT_ST	RO	Module PMU interrupt state register, each module occupies 2 bits. [1:0]: AUDIO [3:2]: VDEC [5:4]: NPU [7:6]: VENC [9:8]: GPU [11:10]: DSP0 [13:12]: DSP1 [15:14]: C910 CORE0 [17:16]: C910 CORE1 [19:18]: C910 CORE2 [21:20]: C910 CORE3 Value After Reset: 0x0

6.5.2.2.43 PD_INT_CLR

- Description: Module PMU interrupt clear register
- Offset: 0x140
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:22]	RESERVED_1	-	
[21:0]	PD_INT_CLR	RW	Module PMU interrupt clear register, each module occupies 2 bits. 1 means clear interrupt. No hardware auto-clear 0 function. [1:0]: AUDIO [3:2]: VDEC [5:4]: NPU [7:6]: VENC [9:8]: GPU [11:10]: DSP0

Bits	Field Name	Access	Description
			[13:12]: DSP1 [15:14]: C910 CORE0 [17:16]: C910 CORE1 [19:18]: C910 CORE2 [21:20]: C910 CORE3 Value After Reset: 0x0

6.5.2.2.44 PD_BLK0_SW_CNT

- Description: Modular down/up feedback wait count register 0
- Offset: 0x144
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_0	RW	AUDIO Module Part Two Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n =0,1) is valid. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_0	RW	AUDIO Module Part One Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF

6.5.2.2.45 PD_BLK1_SW_CNT

- Description: Modular down/up feedback wait count register 1
- Offset: 0x148
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_1	RW	VDEC Module Part Two Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_1	RW	VDEC Module Part One Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF

6.5.2.2.46 PD_BLK2_SW_CNT

- Description: Modular down/up feedback wait count register 2
- Offset: 0x14c
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_2	RW	NPU Module Part Two Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_2	RW	NPU Module Part One Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF

6.5.2.2.47 PD_BLK3_SW_CNT

- Description: Modular down/up feedback wait count register 3
- Offset: 0x150
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_3	RW	VENC Module Part Two Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_3	RW	VENC Module Part One Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF

6.5.2.2.48 PD_BLK4_SW_CNT

- Description: Modular down/up feedback wait count register 4
- Offset: 0x154
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_4	RW	GPU Module Part Two Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF

Bits	Field Name	Access	Description
[15:0]	SW0_WAIT_CNT_4	RW	GPU Module Part One Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF

6.5.2.2.49 PD_BLK5_SW_CNT

- Description: Modular down/up feedback wait count register 5
- Offset: 0x158
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_5	RW	DSP0 Module Part Two Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_5	RW	DSP0 Module Part One Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF

6.5.2.2.50 PD_BLK6_SW_CNT

- Description: Modular down/up feedback wait count register 6
- Offset: 0x15c
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_6	RW	DSP1 Module Part Two Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_6	RW	DSP1 Module Part One Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF

6.5.2.2.51 PD_BLK7_SW_CNT

- Description: Modular down/up feedback wait count register 7
- Offset: 0x160
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_7	RW	C910 CORE0 Module Part Two Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_7	RW	C910 CORE0 Module Part One Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF

6.5.2.2.52 PD_BLK8_SW_CNT

- Description: Modular down/up feedback wait count register 8
- Offset: 0x164
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_8	RW	C910 CORE1 Module Part Two Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_8	RW	C910 CORE1 Module Part One Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF

6.5.2.2.53 PD_BLK9_SW_CNT

- Description: Modular down/up feedback wait count register 9
- Offset: 0x168
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_9	RW	C910 CORE2 Module Part Two Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_9	RW	C910 CORE2 Module Part One Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF

6.5.2.2.54 PD_BLK10_SW_CNT

- Description: Modular down/up feedback wait count register 10
- Offset: 0x16c
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_10	RW	C910 CORE3 Module Part Two Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_10	RW	C910 CORE3 Module Part One Power Down/Power Up Feedback Wait Register, which is in use when PD_SW_CNT_EN [2n] (n=0,1) is valid. Value After Reset: 0xFF

6.5.2.2.55 PD_BLK0_INTV_CNT

- Description: Module PMU state transition wait count register 0
- Offset: 0x180
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_0	RW	AUDIO wait count between module isolation release and open clock. Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_0	RW	AUDIO module isolation enables the wait count between power up and power down. Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_0	RW	AUDIO Module Part One Power on/off and Part Two Wait Count between Power on/off. Value After Reset: 0xFF

6.5.2.2.56 PD_BLK1_INTV_CNT

- Description: Module PMU state transition wait count register 1
- Offset: 0x184
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_1	RW	VDEC wait count between module isolation release and open clock.

Bits	Field Name	Access	Description
			Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_1	RW	VDEC module isolation enables the wait count between power up and power down. Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_1	RW	VDEC Module Part One Power on/off and Part Two Wait Count between Power on/off. Value After Reset: 0xFF

6.5.2.2.57 PD_BLK2_INTV_CNT

- Description: Module PMU state transition wait count register 2
- Offset: 0x188
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_2	RW	NPU wait count between module isolation release and open clock. Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_2	RW	NPU module isolation enables the wait count between power up and power down. Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_2	RW	NPU Module Part One Power on/off and Part Two Wait Count between Power on/off. Value After Reset: 0xFF

6.5.2.2.58 PD_BLK3_INTV_CNT

- Description: Module PMU state transition wait count register 3
- Offset: 0x18c
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_3	RW	VENC wait count between module isolation release and open clock. Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_3	RW	VENC module isolation enables the wait count between power up and power down. Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_3	RW	VENC Module Part One Power on/off and Part Two Wait

Bits	Field Name	Access	Description
			Count between Power on/off. Value After Reset: 0xFF

6.5.2.2.59 PD_BLK4_INTV_CNT

- Description: Module PMU state transition wait count register 4
- Offset: 0x190
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_4	RW	GPU wait count between module isolation release and open clock. Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_4	RW	GPU module isolation enables the wait count between power up and power down. Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_4	RW	GPU Module Part One Power on/off and Part Two Wait Count between Power on/off. Value After Reset: 0xFF

6.5.2.2.60 PD_BLK5_INTV_CNT

- Description: Module PMU state transition wait count register 5
- Offset: 0x194
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_5	RW	DSP0 wait count between module isolation release and open clock. Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_5	RW	DSP0 module isolation enables the wait count between power up and power down. Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_5	RW	DSP0 Module Part One Power on/off and Part Two Wait Count between Power on/off. Value After Reset: 0xFF

6.5.2.2.61 PD_BLK6_INTV_CNT

- Description: Module PMU state transition wait count register 6

- Offset: 0x198
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_6	RW	DSP1 wait count between module isolation release and open clock. Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_6	RW	DSP1 module isolation enables the wait count between power up and power down. Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_6	RW	DSP1 Module Part One Power on/off and Part Two Wait Count between Power on/off. Value After Reset: 0xFF

6.5.2.2.62 PD_BLK7_INTV_CNT

- Description: Module PMU state transition wait count register 7
- Offset: 0x19c
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_7	RW	C910 CORE0 wait count between module isolation release and open clock. Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_7	RW	C910 CORE0 module isolation enables the wait count between power up and power down. Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_7	RW	C910 CORE0 Module Part One Power on/off and Part Two Wait Count between Power on/off. Value After Reset: 0xFF

6.5.2.2.63 PD_BLK8_INTV_CNT

- Description: Module PMU state transition wait count register 8
- Offset: 0x1a0
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_8	RW	C910 CORE1 wait count between module isolation release and open clock. Value After Reset: 0xFF

Bits	Field Name	Access	Description
[19:8]	ISO_SW_WAIT_CNT_8	RW	C910 CORE1 module isolation enables the wait count between power up and power down. Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_8	RW	C910 CORE1 Module Part One Power on/off and Part Two Wait Count between Power on/off. Value After Reset: 0xFF

6.5.2.2.64 PD_BLK9_INTV_CNT

- Description: Module PMU state transition wait count register 9
- Offset: 0x1a4
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_9	RW	C910 CORE2 wait count between module isolation release and open clock. Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_9	RW	C910 CORE2 module isolation enables the wait count between power up and power down. Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_9	RW	C910 CORE2 Module Part One Power on/off and Part Two Wait Count between Power on/off. Value After Reset: 0xFF

6.5.2.2.65 PD_BLK10_INTV_CNT

- Description: Module PMU state transition wait count register 10
- Offset: 0x1a8
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_10	RW	C910 CORE3 wait count between module isolation release and open clock. Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_10	RW	C910 CORE3 module isolation enables the wait count between power up and power down. Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_10	RW	C910 CORE3 Module Part One Power on/off and Part Two Wait Count between Power on/off.

Bits	Field Name	Access	Description
			Value After Reset: 0xFF

6.5.2.2.66 AUDIO_PMU_REQ

- Description: AUDIO->E902 request register
- Offset: 0x1f8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	AUDIO_PMU_REQ	RO	AUDIO->E902 request register Value After Reset: 0x0

6.5.2.2.67 AUDIO_PMU_STS

- Description: AUDIO->E902 request register
- Offset: 0x1fc
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	AUDIO_PMU_STS	RO	AUDIO->E902 request register Value After Reset: 0x0

6.5.2.2.68 AUDIO_PMU_INTR

- Description: AUDIO->E902 request register
- Offset: 0x204
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	AUDIO_PMU_INTR_MSK	RW	AUDIO->E902 interrupt screen register 0: Shielded 1: Unshielded Value After Reset: 0x0
[2]	AUDIO_PMU_INTR_CLR	W1S	AUDIO->E902 interrupt clear register, hardware auto clear 0. Value After Reset: 0x0
[1]	AUDIO_PMU_INTR_STS	RO	AUDIO->E902 interrupt status register

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[0]	AUDIO_PMU_INTR_STS_RAW	RO	AUDIO->E902 interrupt raw status register Value After Reset: 0x0

6.5.2.2.69 PMU_AUDIO_REQ

- Description: E902->AUDIO request register
- Offset: 0x208
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	PMU_AUDIO_REQ	RW	E902->AUDIO request register Value After Reset: 0x0

6.5.2.2.70 PMU_AUDIO_STS

- Description: E902->AUDIO request register
- Offset: 0x20c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PMU_AUDIO_STS	RW	E902->AUDIO request register Value After Reset: 0x0

6.5.2.2.71 MEM_LP_MODE

- Description: Memory low power mode register
- Offset: 0x210
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:23]	RESERVED_6	-	
[22]	SRAM_AXI_AXI_SRAM_SD	RW	SRAM_AXI memory shutdown register Value After Reset: 0x0
[21]	SRAM_AXI_AXI_SRAM_SLP	RW	SRAM_AXI memory sleep register Value After Reset: 0x0
[20]	SRAM_AXI_AXI_SRAM_DSLP	RW	SRAM_AXI memory deep sleep register Value After Reset: 0x0

Bits	Field Name	Access	Description
[19]	RESERVED_5	-	
[18]	C910_CPU_MEM_SD	RW	C910 top memory shutdown register Value After Reset: 0x0
[17]	C910_CPU_MEM_SLP	RW	C910 top memory sleep register Value After Reset: 0x0
[16]	C910_CPU_MEM_DSLP	RW	C910 top memory deep sleep register Value After Reset: 0x0
[15]	RESERVED_4	-	
[14]	C910_CORE3_MEM_SD	RW	C910 CORE3 memory shutdown register Value After Reset: 0x0
[13]	C910_CORE3_MEM_SLP	RW	C910 CORE3 memory sleep register Value After Reset: 0x0
[12]	C910_CORE3_MEM_DSLP	RW	C910 CORE3 memory deep sleep register Value After Reset: 0x0
[11]	RESERVED_3	-	
[10]	C910_CORE2_MEM_SD	RW	C910 CORE2 memory shutdown register Value After Reset: 0x0
[9]	C910_CORE2_MEM_SLP	RW	C910 CORE2 memory sleep register Value After Reset: 0x0
[8]	C910_CORE2_MEM_DSLP	RW	C910 CORE2 memory deep sleep register Value After Reset: 0x0
[7]	RESERVED_2	-	
[6]	C910_CORE1_MEM_SD	RW	C910 CORE1 memory shutdown register Value After Reset: 0x0
[5]	C910_CORE1_MEM_SLP	RW	C910 CORE1 memory sleep register Value After Reset: 0x0
[4]	C910_CORE1_MEM_DSLP	RW	C910 CORE1 memory deep sleep register Value After Reset: 0x0
[3]	RESERVED_1	-	
[2]	C910_CORE0_MEM_SD	RW	C910 CORE0 memory shutdown register Value After Reset: 0x0

Bits	Field Name	Access	Description
[1]	C910_CORE0_MEM_SLP	RW	C910 CORE0 memory sleep register Value After Reset: 0x0
[0]	C910_CORE0_MEM_DSLP	RW	C910 CORE0 memory deep sleep register Value After Reset: 0x0

6.5.2.2.72 C910_DBG_MASK

- Description: C910 debug shield register
- Offset: 0x214
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	C910_CORE3_DBG_MASK	RW	C910 CORE3 debug shield register Value After Reset: 0x0
[2]	C910_CORE2_DBG_MASK	RW	C910 CORE2 debug shield register Value After Reset: 0x0
[1]	C910_CORE1_DBG_MASK	RW	C910 CORE1 debug shield register Value After Reset: 0x0
[0]	C910_CORE0_DBG_MASK	RW	C910 CORE0 debug shield register Value After Reset: 0x0

6.5.2.2.73 C910_L2CACHE

- Description: C910 L2CACHE flush register
- Offset: 0x218
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	C910_CPU_NO_OP	RO	C910 no operation register Value After Reset: 0x0
[1]	C910_CPU_L2CACHE_FLUSH_DONE	RO	C910 L2Cache flush completion register Value After Reset: 0x0
[0]	C910_CPU_L2CACHE_FLUSH_REQ	RW	C910 L2Cache flush request register Value After Reset: 0x0

6.5.2.2.74 BISR_CTRL

- Description: Reserved, not used
- Offset: 0x220
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:7]	RESERVED_1	-	
[6]	PAD_BISR_BYPASS	RO	Reserved Value After Reset: 0x0
[5]	BISR_SRAM_CDE_REG	RO	Reserved Value After Reset: 0x0
[4]	BISR_L2_CDE_REG	RO	Reserved Value After Reset: 0x0
[3]	BISR_SRAM_DONE_REG	RO	Reserved Value After Reset: 0x0
[2]	BISR_L2_DONE_REG	RO	Reserved Value After Reset: 0x0
[1]	BISR_BYPASS_REG	RW	Reserved Value After Reset: 0x0
[0]	BISR_BYPASS_LOCK_REG	RW	Reserved Value After Reset: 0x0

6.5.2.2.75 EFUSE_PRELOAD_DONE

- Description: eFuse preload completion status register
- Offset: 0x224
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	EFUSE_PRELOAD_DONE_REG	RO	eFuse preload completion register Value After Reset: 0x0

6.5.2.2.76 GPIO_RTE

- Description: Reserved, not used
- Offset: 0x228
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	GPIO2_PAD_IRTE	RW	Reserved Value After Reset: 0x0
[0]	GPIO1_PAD_IRTE	RW	Reserved Value After Reset: 0x0

6.5.2.2.77 PLL_DSKEW_LOCK

- Description: PLL calibration lock register
- Offset: 0x22c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	PLL_DSKEWCAL_BYPASS_REG	RW	PLL calibration bypass register, software reads pad_Pll_Dskewcal_After bypass, write the read value to the bit. Value After Reset: 0x0
[1]	PAD_PLL_DSKEWCAL_BYPASS	RO	PLL calibration bypass register from PAD Value After Reset: 0x0
[0]	PLL_DSKEWCAL_BYPASS_LOCK	RW	PLL calibration bypass lock register for locking pll_Dskewcal_Bypass_Reg Value After Reset: 0x0

6.5.2.2.78 SRAM_AXI_CFG

- Description: SRAM_AXI configuration register
- Offset: 0x230
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_2	-	
[15:8]	SRAMC_PCHK_MODE	W1S	Parity check mode, close parity_0 check, any bit is 1 enabled parity check. Value After Reset: 0x0
[7:3]	RESERVED_1	-	
[2]	SRAMC_ACG_EN	RW	Auto clock gating enable, controlled by software.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[1]	SRAMC_OVCAP_DET	RW	Memory region accesses the boundary detection capability, which is configured by software. Value After Reset: 0x0
[0]	SRAMC_INIT	RW	Soft reset signal of SRAM controller, controlled by software. Value After Reset: 0x0

6.5.2.2.79 SRAM_AXI_ST

- Description: SRAM_AXI configuration register
- Offset: 0x234
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SRAMC_OVCAP_ALARM	RO	Memory region accesses the out-of-bounds warning signal Value After Reset: 0x0

6.5.2.2.80 SRAM_AXI_ERR_STS_0

- Description: SRAM_AXI check error register 0
- Offset: 0x238
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SRAMC_ERR_STS_0	RO	Debug signal indicating a logical failure of module Value After Reset: 0x0

6.5.2.2.81 SRAM_AXI_ERR_STS_1

- Description: SRAM_AXI check error register 1
- Offset: 0x23c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SRAMC_ERR_STS_1	RO	Debug signal indicating a logical failure of module Value After Reset: 0x0

6.5.2.2.82 SRAM_AXI_ERR_STS_2

- Description: SRAM_AXI check error register 2
- Offset: 0x240
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SRAMC_ERR_STS_2	RO	Debug signal indicating a logical failure of module Value After Reset: 0x0

6.5.2.2.83 SRAM_AXI_ERR_STS_3

- Description: SRAM_AXI check error register 3
- Offset: 0x244
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SRAMC_ERR_STS_3	RO	Debug signal indicating a logical failure of module Value After Reset: 0x0

6.5.2.2.84 SRAM_AXI_ERR_STS_4

- Description: SRAM_AXI check error register 4
- Offset: 0x248
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SRAMC_ERR_STS_4	RO	Debug signal indicating a logical failure of module Value After Reset: 0x0

6.5.2.2.85 SE_MUX_LOCK

- Description: Secure IO MUX lock register
- Offset: 0x24c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:7]	RESERVED_1	-	
[6:1]	SE_IO_MUX_LOCK	RW	SE IO MUX lock Value After Reset: 0x0
[0]	SE_RST_MUX_LOCK	RW	SE_RSTN IO MUX lock Value After Reset: 0x0

6.5.2.2.86 CPU_DBG_DIS_LOCK

- Description: CPU debug lock disable register
- Offset: 0x270
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	CPU_DBG_DIS_LOCK	RW	CPU debug lock signal BIT0: E902 BIT1: C906 BIT2: C910 Value After Reset: 0x0

6.5.2.2.87 RESERVED_REG_4

- Description: RESERVED_REG_4
- Offset: 0x300
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_4	RW	RESERVED_REG_4 Value After Reset: 0x0

6.5.2.2.88 RESERVED_REG_5

- Description: RESERVED_REG_5
- Offset: 0x304
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_5	RW	RESERVED_REG_5 Value After Reset: 0x0

6.5.2.2.89 RESERVED_REG_6

- Description: RESERVED_REG_6
- Offset: 0x308
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_6	RW	RESERVED_REG_6

Bits	Field Name	Access	Description
			Value After Reset: 0x0

6.5.2.2.90 RESERVED_REG_7

- Description: RESERVED_REG_7
- Offset: 0x30c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_7	RW	RESERVED_REG_7 Value After Reset: 0x0

6.5.2.2.91 RESERVED_REG_8

- Description: RESERVED_REG_8
- Offset: 0x400
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_8	RW	RESERVED_REG_8 Value After Reset: 0x0

6.5.2.2.92 RESERVED_REG_9

- Description: RESERVED_REG_9
- Offset: 0x404
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_9	RW	RESERVED_REG_9 Value After Reset: 0x0

6.5.2.2.93 RESERVED_REG_10

- Description: RESERVED_REG_10
- Offset: 0x408
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_10	RW	RESERVED_REG_10 Value After Reset: 0x0

6.5.2.2.94 RESERVED_REG_11

- Description: RESERVED_REG_11
- Offset: 0x40c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_11	RW	RESERVED_REG_11 Value After Reset: 0x0

6.5.2.2.95 RESERVED_REG_12

- Description: RESERVED_REG_12
- Offset: 0x500
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_12	RW	RESERVED_REG_12 Value After Reset: 0x0

6.5.2.2.96 RESERVED_REG_13

- Description: RESERVED_REG_13
- Offset: 0x504
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_13	RW	RESERVED_REG_13 Value After Reset: 0x0

6.5.2.2.97 RESERVED_REG_14

- Description: RESERVED_REG_14
- Offset: 0x508
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_14	RW	RESERVED_REG_14 Value After Reset: 0x0

6.5.2.2.98 RESERVED_REG_15

- Description: RESERVED_REG_15
- Offset: 0x50c

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_15	RW	RESERVED_REG_15 Value After Reset: 0x0

6.5.2.2.99 RESERVED_REG_16

- Description: RESERVED_REG_16
- Offset: 0x600
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_16	RW	RESERVED_REG_16 Value After Reset: 0x0

6.5.2.2.100 RESERVED_REG_17

- Description: RESERVED_REG_17
- Offset: 0x604
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_17	RW	RESERVED_REG_17 Value After Reset: 0x0

6.5.2.2.101 RESERVED_REG_18

- Description: RESERVED_REG_18
- Offset: 0x608
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_18	RW	RESERVED_REG_18 Value After Reset: 0x0

6.5.2.2.102 RESERVED_REG_19

- Description: RESERVED_REG_19
- Offset: 0x60c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_19	RW	RESERVED_REG_19 Value After Reset: 0x0

7 Boot

The chip has a built-in BootROM that not only supports boot from eMMC flash, SD card, NAND flash, and NOR flash, but also supports image loading from USB, namely Fastboot mode. In addition, it also supports CCT (UART) mode. In CCT mode, it programs the image to SRAM or an external storage medium through the UART interface. Different boot modes are selected through BOOT_SEL pins, as shown in Figure & Table 7-1.

Figure & Table 7-1 Boot mode select

BOOT_SEL[2]	BOOT_SEL[1:0]	Boot Media	Boot Interface
0	xx	USB	USB
1	00	eMMC Flash	eMMC
	01	SD/TF	SDIO
	10	SPI NAND Flash	QSPI
	11	SPI NOR Flash	QSPI

Where:

- USB OTG: Load image through USB interface;
- eMMC Flash: Load image from eMMC flash through eMMC interface;
- SD/TF: Load image from SD/TF card through SDIO interface;
- SPI NAND Flash/SPI NOR Flash: Load image through QSPI interface;
- Method to enter the CCT mode: The CCT tool on PC is keeping sending connection requests to SoC. After SoC is reset, BootROM detects the CCT connection request and enters the CCT mode.

Different flash page sizes are selected through GPIO pins, as shown in Figure & Table 7-2.

Figure & Table 7-2 Flash page size select

GPIO3-3	GPIO3-2	Description
0	0	page size = 2k
0	1	page size = 4k
1	0	page size = 8k
1	1	page size = 16k

8 Processor

SoC has three processors: C910, C906 and E902. C910 is a multi-core architecture. C906 and E902 are single-core architectures. C910/C906/E902 are heterogeneous architectures. C910 is the main control of the system, which is used to run the operating system and application programs. C906 is used for voice signal processing and E902 is used for low power control. After the chip is reset, C910 starts first, C906/E902 needs to be waked up by C910. In low power mode, E902 is active and C910/C906 can be powered down.

Main Features of C910 Multi-Core Architecture

- The homogeneous multi-core architecture consists of four cores. Core0 defaults to TEE core. Core1-3 attributes can be configured through Core0.
- AXI4.0 bus interface, address width 40 bits, data width 128 bits.
- A two-level cache structure: Harvard architecture L1 Cache and share L2 Cache.
- L1 Cache supports MESI protocol and L2 Cache supports MOESI protocol.
- 1MB L2 Cache, 16-way set associativity, and the cache line size is 64B.
- Supports built-in processor core local interrupt controller (CLINT) and platform-level interrupt controller (PLIC), and the number of external interrupt sources is 240.
- Supports built-in timer, clocked with a 3MHz clock.
- Supports custom and interface RISC-V compliant multi-core debug architecture.
- Compatible with RISC-V PMP memory protection standard and supports 32 matching entries.
- Supports interrupt security extension, debug security extension, and L2 Cache security extension.

Main Features of C910 Core

- RISC-V 64GCV instruction architecture
- Supports little-endian mode.
- 9-12 stage deep pipeline architecture
- 3-issue and 8-execution superscalar architecture, completely transparent to software
- In-order instruction fetch, out-of-order issue, out-of-order completion, and in-order retirement
- SV39 memory management unit realizes virtual-to-physical address translation and memory management, supports two-level TLB, of which jTLB 1024 entries.
- Instruction cache 64KB, data cache 64KB and cache behavior 64B
- Instruction prefetch function, hardware auto detect and dynamic start
- Low-power consumption strategy for instruction cache based on way-access track
- Low power execution technology for the short loop buffer
- 64Kb two-stage multi-way parallel branch predictor
- 1024 entry branch target buffer
- Supports 12-tier hardware return address stack

- 256 entry indirect jump branch predictor
- Non-blocking issue and speculative execution
- Physical register-based rename technology
- Supports 0 delay move instruction.
- Double-issue, full out-of-order execution load and store instructions
- Supports read/write 8-way concurrent bus access.
- Supports write combining.
- Supports 8-way data cache hardware prefetch and stride prefetch mode.
- The floating point processing unit is configurable, and supports half precision and single precision.

Main Features of C910 Vector

- Complies with RISC-V V vector extension (revision 0.7.1).
- The computing power can reach 16Gflops (@2core, 2Ghz).
- Supports vector execution unit, supports half-precision/single-precision floating-point and 8-bit/16-bit/32-bit/64-bit integer vector operations.
- The vector data access unit provides a maximum data width of 128 bits.
- Supports segment load and store instructions.
- Performance-optimized non-aligned memory access

Main Features of C906

- RV64IMA[FD]C[V] instruction architecture
- 5-stage single-issue in-order pipeline
- Instruction and data cache of the first-level Harvard architecture, instruction cache 32KB, data cache 32KB, cache behavior 64B
- SV39 memory management unit, realizes virtual-to-physical address translation and memory management, supports two-level TLB, of which jTLB 256 entries.
- AXI4.0 bus interface, address width 40 bits, data width 128 bits
- Supports built-in processor core local interrupt controller (CLINT) and platform-level interrupt controller (PLIC), and the number of external interrupt sources is 80.
- Supports built-in timer, clocked with a 3MHz clock.
- Compatible with RISC-V PMP memory protection standard, supports eight regions.

Main Features of C906 Vector

- Complies with RISC-V V vector extension standard (revision 0.7.1).
- The computing power can reach 4GFlops (@1GHz).
- Vector execution unit operation width 128 bits
- Supports INT8/INT16/INT32/INT64/FP16/FP32/BFP16 vector operations.

Main Features of E902

- Supports RISC-V RV32E[M]C instruction set.

- 16 32-bit general-purpose registers
- 2-stage in-order pipeline
- Supports RISC-V machine mode and user mode.
- Configurable single-cycle hardware multiplier, multi-cycle hardware divider
- Compatible with RISC-V CLIC interrupt standard, supports interrupt nesting, and the number of external interrupt sources is 32.
- Supports built-in timer, clocked with a 3MHz clock.
- Supports AHB-Lite bus protocol, instruction bus and system bus.
- Instruction and data share 32KB external SRAM space

9 DSP

9.1 Overview

The Vision Q7 DSP is a high-performance embedded digital signal processor (DSP) optimized for vision, image, and video processing. It is based on the NX pipeline designed for 3-cycle memory access.

The instruction set architecture and memory subsystem provide easy programmability in C/C++ and deliver the high sustained pixel processing performance required for advanced vision, image and video processing and analysis applications.

Figure & Table 9-1shows DSP block diagram.

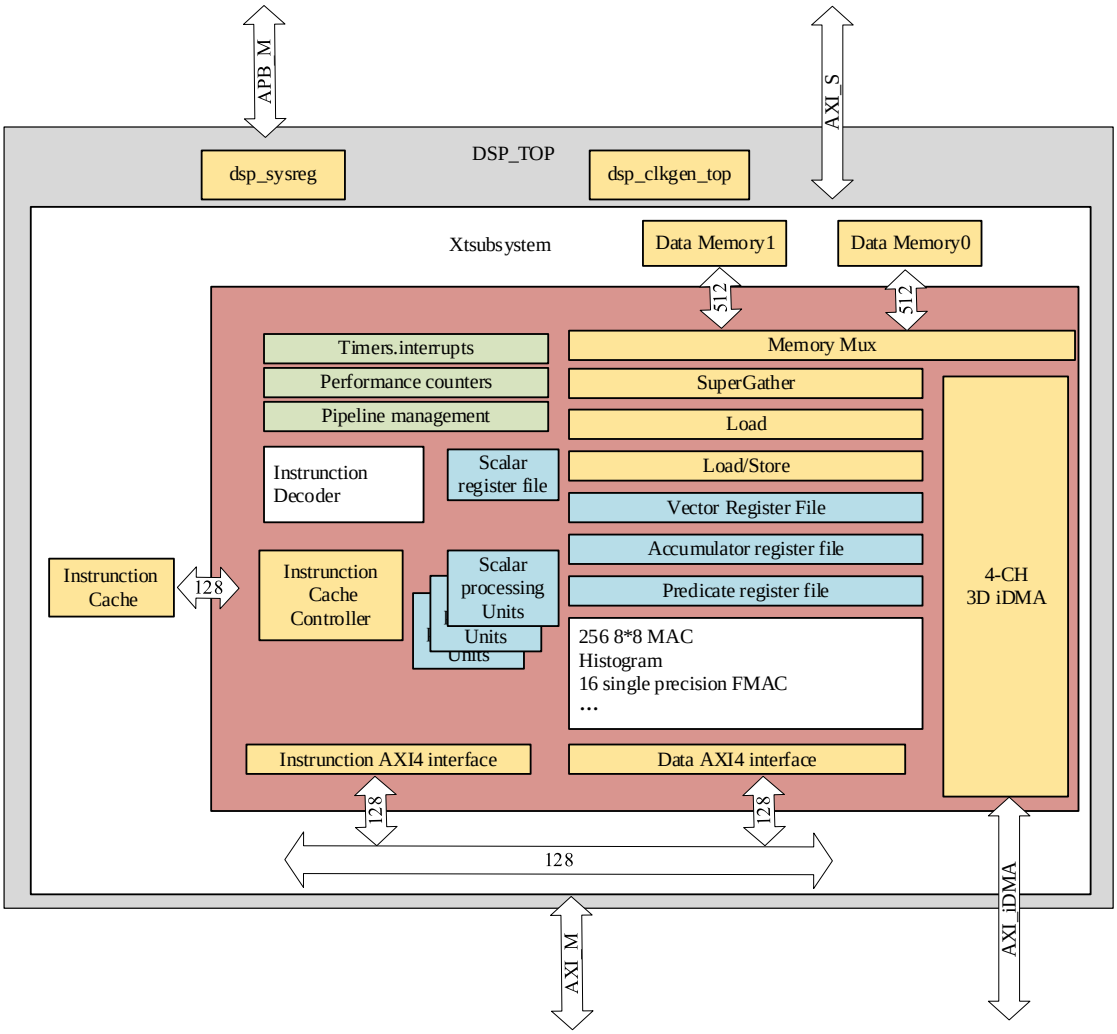


Figure & Table 9-1 DSP block diagram

9.2 Main Features

The key features of DSP are as follows:

- Support histogram
- 256 8*8 MAC
- 16 single precision FMAC
- 32KB instruction cache
- Two 128K data RAM
- Vector pipeline
- Scalar pipeline
- iDMA
  - 4 channels
- SIMD
- SuperGather

9.3 Interface

This section summarizes the TAP standard. Complete details of the JTAG TAP standard are outside the scope of this document. The interested reader is referred to the *IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std. 1149.1a-1993*.

Figure & Table 9-2 JTAG interface

Pin Name	Direction	Width	Description
DSP_JTG_TCLK	I	1	Clock that controls sampling of TMS, TDI and update of TDO
DSP_JTG_TMS	I	1	Input to TAP controller state machine
DSP_JTG_TRST	I	1	Active low reset input for asynchronous initialization of the TAP controller
DSP_JTG_TDI	I	1	Selected serial instruction/data shift register input
DSP_JTG_TDO	O	1	Selected serial instruction/data shift register tri-state output

9.4 Function Description

The Xtensa NX processor consists of four major blocks: instruction fetch, scalar pipeline, vector pipeline, and memory subsystem.

9.4.1 Instruction Fetch

The instruction fetch reads instruction data, and forms aligned instructions to dispatch. Following are some of the instruction fetch major features:

- Branch prediction. A table of branch targets and prediction bits are maintained to improve branch performance.
- Return address stack. Subroutines may be called from different locations with a program, and the return address stack is used in lieu of the branch target stored in the branch predictor.
- Zero overhead loops. One level of zero overhead loops are supported.

- Loop buffer. A loop buffer holds a configurable number of instruction bytes in order to reduce the power that would be required to read instruction memories.
- Variable length instructions. Multiple instruction lengths are supported, leading to a reduction in code size.

9.4.2 Scalar and Vector Pipelines

The execution pipeline is divided into a scalar and vector pipeline. The scalar pipeline implements the base instruction set and scalar integer pipeline. The vector pipeline implements the vector register files and all associated instructions. These units decode and then execute the instruction using the format specification of Xtensa instructions. Note that a Controller memory system does not have a vector pipeline. The scalar and vector units determine when an instruction is committed and architectural state is updated. In the case of interrupts or exceptions that occur before an instruction is committed these units prevent the instruction from modifying architectural state.

9.4.3 Memory Subsystem

The memory subsystem is comprised of two parts:

- Level 1 instruction memories
- Level 1 data memories

9.5 Usage

9.5.1 DSP Register

DSP registers consist of two parts, DSP internal registers and DSP wrapper registers. DSP internal registers are used for debugging, its base address is DSP0_APB for DSP0; DSP wrapper registers are used for controlling, its base address is DSP0_APB+0x4000. DSP1 is similar to DSP0.

9.5.2 DSP Configuration Flow

The reference configuration of DSP0 is as follows.

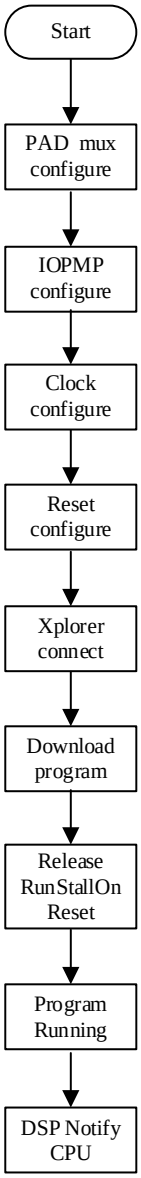


Figure & Table 9-3 DSP configuration flow

1. PAD MUX configuration:

   DSP JTAG interface signals mux with other signals，if use DSP JTAG, you must configure PAD.

   The following configuration is used for DSP0:

   - Configure MUX_CFG_003.GPIO0_22_MUX_CFG to 0x1.
   - Configure MUX_CFG_003.GPIO0_23_MUX_CFG to 0x1.
   - Configure MUX_CFG_004. GPIO0_24_MUX_CFG to 0x1.
   - Configure MUX_CFG_004. GPIO0_25_MUX_CFG to 0x1.
   - Configure MUX_CFG_004. GPIO0_26_MUX_CFG to 0x1.

2. IOPMP:

   Before using AXI bus, you must configure IOPMP correctly. Detailed descriptions are not described in this document.

3. Clock configuration:

   Configure the DSPSYS_CLK_GATE_EN register to enable DSP clocks.

4. Reset configuration:
   Configure the DSPSYS_SW_RST register to release DSP resets.
5. Xplorer connect and download program.
   Detailed descriptions of Xplorer are not described in this document.
   If you don't use Xplorer, you must prepare program in memory before releasing RunStallOnReset.
6. Release RunStallOnReset:
   Configure the RunStallOnReset register.
7. After Releasing RunStallOnReset, DSP will fetch instructions and run as program control.
8. After DSP completes its work, it notifies the CPU by sending an interrupt. Detailed information can be referred at Section 9.5.3.

DSP1 configuration is similar to DSP0.

9.5.3 DSP Interacts with CPU

The DSP and CPU can communicate in interrupt mode. The reference configuration of DSP0 is as follows.

If DSP0 wants to send some messages to CPU, DPS0 can write DSP0_CPU_INT_STA register to send an interrupt to CPU. The detailed flow can be referred as the following.

1. Disable interrupt mask. DSP0 write 4'h0 to the DSP0_CPU_INT_MASK register, the corresponding interrupt mask "dsp0_cpu_int_sta3/dsp0_cpu_int_sta3/dsp0_cpu_int_sta1/dsp0_cpu_int_sta0" are disabled.
2. Sent interrupt. DSP0 writes 1 to DSP0_CPU_INT_STA. "dsp0_cpu_int_sta0" interrupt will be sent to CPU. Other interrupts are similar to dsp0_cpu_int_sta0.
3. Get interrupt. CPU gets the interrupt, then executes Interrupt Service Routines (ISR).
4. Clear interrupt. After CPU finishes ISR, CPU writes 1 to DSP0_CPU_INT_CLR.dsp0_cpu_int_clr0 to clear the interrupt.

If CPU wants to send some messages to DSP0, CPU can write the CPU_DSP0_INT_STA register to send an interrupt to DSP0. The detailed flow can be referred from "DSP0 wants to send some messages to CPU".

If DSP0 wants to send some messages to DSP1, DPS0 can write DSP0_DSP1_INT_STA register to send an interrupt to DSP1. The detailed flow can be referred from "DSP0 wants to send some messages to CPU".

DSP1 is similar to DSP0.

10 MBOX

10.1 Overview

In a multi-core SoC, inter-core communication is the guarantee of multi-core cooperative work. MBOX is a module that provides inter-core communication in an interrupt-triggered manner. For the four CPU cores of C910T, E902, C906 and C910R in this chip, there are four MBOX units whose corresponding CPU_IDX are 0, 1, 2, and 3 respectively. Figure & Table 10-1 shows the structures of the decentralized four mailboxes.

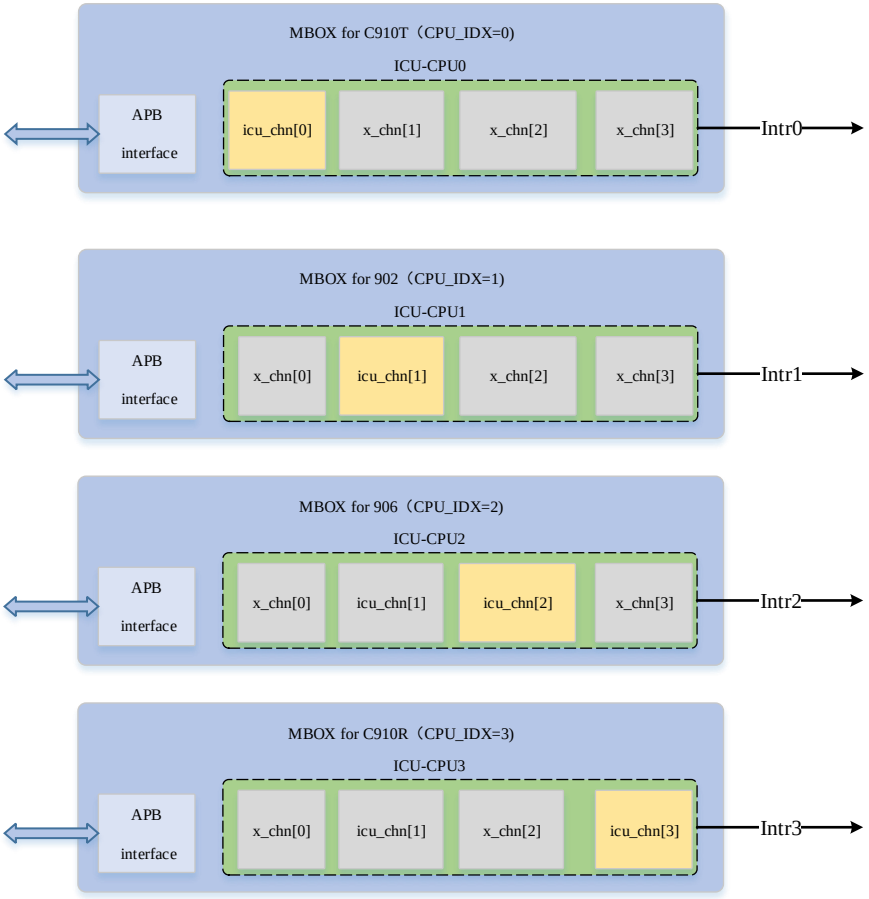


Figure & Table 10-1 MAILBOX diagram

10.2 Main Features

The main features of MBOX are as follows:

- Supports software-controlled multi-core communication of single-send single-receive, multi-send single-receive, single-send multi-receive, and multi-send multi-receive.
- Supports the sender CPU to transmit information other than interrupt events to the receiver CPU, which is reflected in the form of information register group.

- Supports software to check the interrupt status, that is, software to check the current communication status.
- Supports software to mask interrupt generation, that is, software to cut off the communication channel.
- Supports software to clear interrupt status (a prerequisite for ending a communication).
- The amount of information (the number of 32bit registers) transmitted by the sender CPU is 8.
- This module does not provide protection function. If the sender CPU still sends new information to the receiver CPU when the receiver CPU has not completed the reception, the previous information will be overwritten, resulting in information errors. In order to ensure that information is transmitted correctly, it is necessary to establish a software handshake mechanism.
- During the running process of this module, it enters the low power mode and it is not guaranteed to support the on-site protection function.
- This module is reset during operation, all information will be cleared, and the on-site protection function is not supported.

10.3 Function Description

The information that needs to be transmitted for multi-core communication is as follows:

- Which CPU is the receiver of information.
- Which CPU is the sender of information.
- Specific information to be transmitted after the two CPUs shake hands.

The following takes the communication between CPU1 and CPU0 as an example to briefly describe the communication process as follows:

1. Select the Interrupt Control Unit (ICU) of MBOX: The sender CPU1 selects ICU-CPU0 corresponding to the receiver CPU0.
2. Store information to be transmitted: The sender CPU1 stores the information to be transmitted in ICU-CPU0.
3. The sender triggers an interrupt: The sender CPU1 configures ICU-CPU0 to generate an interrupt.
4. The receiver receives interrupt: The receiver CPU0 receives the interrupt generated by ICU-CPU0 and enters the interrupt processing function.
5. The receiver determines the sender: By reading the interrupt status in ICU-CPU0, the receiver CPU0 knows that it is the interrupt sent by CPU1.
6. The receiver receives information: The receiver CPU0 reads contents stored by CPU1 from ICU-CPU0.
7. The receiver clears interrupt: The receiver CPU0 configures ICU-CPU0 to clear the interrupt.

10.4 Usage

The steps of using MBOX are as follows (the core index of the receiver is X, the core index of the sender is Y, and the index Z[] of the information register group is a list):

1. All the cores enable their mailbox interrupt during power-on initialization.

2. The sender CPU writes information to be transmitted to the information register group of the channel (Y) of ICU (X).
3. The sender CPU writes 1 to the bit in the generate register corresponding to the information register group of the channel (Y) of ICU (X). If there are multiple information register groups, write 1 to multiple corresponding bits.
4. After the channel (Y) detects that there is 1 in the generate register, an interrupt is generated.
5. The receiver CPU receives the interrupt, reads the interrupt status register of ICU(X) in the interrupt response program, and learns that it is information of the sender CPU (Y).
6. The receiver CPU reads the generate information from the channel (Y) of ICU (X) according to the received information of the sender CPU (Y), and learns the information register group index list (Z[]).
7. The receiver CPU reads the information that the sender CPU (Y) transmitted to the receiver CPU (X) from the information register group index list (Z[]) of the channel (Y) of ICU (X) according to the received information of the sender CPU (Y).
8. After information transmission is completed, the receiver CPU clears the raw interrupt register (write 1 to the corresponding bit) of the channel (Y) of ICU (X) according to the received information of the sender CPU (Y).

NOTE

If the sender CPU writes information again when the receiver has not read out information, it will overwrite information previously transmitted, which may cause information fragments. Therefore, corresponding software protection measures are required to ensure that information fragments do not appear. There are two options here (Option 1 is recommended)

Option 1: Before sending information, the sender CPU reads the channel (Y) of ICU (X) to see whether the raw interrupt register has been cleared by the receiver CPU. If it has been cleared, the sender CPU can send new information. If not, wait for a while and check the raw interrupt register again.

Option 2: The receiver CPU sends a response through Mailbox to inform the sender CPU that it has finished receiving the data it sent. After the sender CPU receives ACK from the receiver CPU, it marks the receiver CPU as a receivable state. When the sender CPU intends to send information again, it will check its internal tag status. If it can send information, it will send. If not, it will wait for a while and check its internal tag status. Option 2 needs to avoid shock of information sent by the receiver CPU, that is, the ACK sent by the receiver CPU cannot be regarded as a new transmission. Of course, the ACK sent by the receiver has the risk of being overwritten by information of its own other processes.

10.5 Register Description

10.5.1 Register Memory Map

Register	Offset	Description	Section/Page
M0_INTR_STA	0x0	Interrupt status register of ICU0	10.5.2.1/659
M0_INTR_CLR	0x4	Clear interrupt register of ICU0	10.5.2.2/659
M0_INTR_RAW	0x8	ICU0's raw interrupt status register	10.5.2.3/660

Register	Offset	Description	Section/Page
M0_INTR_MASK	0xC	ICU0 interrupt mask register	10.5.2.4/660
M0_C1_INTR_STA	0x1000	Channel1 interrupt status register of ICU0	10.5.2.5/660
M0_C1_INTR_CLR	0x1004	Channel1 clear interrupt register of ICU0	10.5.2.6/660
M0_C1_INTR_RAW	0x1008	Channel1 ICU0's raw interrupt status register	10.5.2.7/661
M0_C1_INTR_MASK	0x100C	Channel1 ICU0 interrupt mask register	10.5.2.8/661
M0_C1_GEN	0x1010	Interrupt generation register of channel 1 of ICU0	10.5.2.9/661
M0_C1_INFO0	0x1014	Information register 0 of channel 1 of ICU0	10.5.2.10/662
M0_C1_INFO1	0x1018	Information register 1 of channel 1 of ICU0	10.5.2.11/662
M0_C1_INFO2	0x101C	Information register 2 of channel 1 of ICU0	10.5.2.12/662
M0_C1_INFO3	0x1020	Information register 3 of channel 1 of ICU0	10.5.2.13/662
M0_C1_INFO4	0x1024	Information register 4 of channel 1 of ICU0	10.5.2.14/662
M0_C1_INFO5	0x1028	Information register 5 of channel 1 of ICU0	10.5.2.15/663
M0_C1_INFO6	0x102C	Information register 6 of channel 1 of ICU0	10.5.2.16/663
M0_C1_INFO7	0x1030	Information register 7 of channel 1 of ICU0	10.5.2.17/663
M0_C2_INTR_STA	0x2000	Channel2 Interrupt status register of ICU0	10.5.2.18/663
M0_C2_INTR_CLR	0x2004	Channel2 Clear interrupt register of ICU0	10.5.2.19/664
M0_C2_INTR_RAW	0x2008	Channel2 ICU0's raw interrupt status register	10.5.2.20/664
M0_C2_INTR_MASK	0x200C	Channel2 ICU0 interrupt mask register	10.5.2.21/664
M0_C2_GEN	0x2010	Interrupt generation register of channel 2 of ICU0	10.5.2.22/664
M0_C2_INFO0	0x2014	Information register 0 of channel 2 of ICU0	10.5.2.23/665
M0_C2_INFO1	0x2018	Information register 1 of channel 2 of ICU0	10.5.2.24/665
M0_C2_INFO2	0x201C	Information register 2 of channel 2 of ICU0	10.5.2.25/665
M0_C2_INFO3	0x2020	Information register 3 of channel 2 of ICU0	10.5.2.26/665
M0_C2_INFO4	0x2024	Information register 4 of channel 2 of ICU0	10.5.2.27/666
M0_C2_INFO5	0x2028	Information register 5 of channel 2 of ICU0	10.5.2.28/666
M0_C2_INFO6	0x202C	Information register 6 of channel 2 of ICU0	10.5.2.29/666

Register	Offset	Description	Section/Page
M0_C2_INFO7	0x2030	Information register 7 of channel 2 of ICU0	10.5.2.30/666
M0_C3_INTR_STA	0x3000	Channel3 interrupt status register of ICU0	10.5.2.31/667
M0_C3_INTR_CLR	0x3004	Channel3 clear interrupt register of ICU0	10.5.2.32/667
M0_C3_INTR_RAW	0x3008	Channel3 ICU0's raw interrupt status register	10.5.2.33/667
M0_C3_INTR_MASK	0x300C	Channel3 ICU0 interrupt mask register	10.5.2.34/667
M0_C3_GEN	0x3010	Interrupt generation register of channel3 of ICU0	10.5.2.35/668
M0_C3_INFO0	0x3014	Information register 0 of channel 3 of ICU0	10.5.2.36/668
M0_C3_INFO1	0x3018	Information register 1 of channel 3 of ICU0	10.5.2.37/668
M0_C3_INFO2	0x301C	Information register 2 of channel 3 of ICU0	10.5.2.38/668
M0_C3_INFO3	0x3020	Information register 3 of channel 3 of ICU0	10.5.2.39/669
M0_C3_INFO4	0x3024	Information register 4 of channel 3 of ICU0	10.5.2.40/669
M0_C3_INFO5	0x3028	Information register 5 of channel 3 of ICU0	10.5.2.41/669
M0_C3_INFO6	0x302C	Information register 6 of channel 3 of ICU0	10.5.2.42/669
M0_C3_INFO7	0x3030	Information register 7 of channel 3 of ICU0	10.5.2.43/670
M1_C0_INTR_STA	0x4000	Interrupt status register of ICU1	10.5.2.44/670
M1_C0_INTR_CLR	0x4004	Clear interrupt register of ICU1	10.5.2.45/670
M1_C0_INTR_RAW	0x4008	ICU1's raw interrupt status register	10.5.2.46/670
M1_C0_INTR_MASK	0x400C	ICU1 interrupt mask register	10.5.2.47/671
M1_C0_GEN	0x4010	Interrupt generation register of channel 1 of ICU1	10.5.2.48/671
M1_C0_INFO0	0x4014	Information register 0 of channel 1 of ICU1	10.5.2.49/671
M1_C0_INFO1	0x4018	Information register 1 of channel 1 of ICU1	10.5.2.50/671
M1_C0_INFO2	0x401C	Information register 2 of channel 1 of ICU1	10.5.2.51/672
M1_C0_INFO3	0x4020	Information register 3 of channel 1 of ICU1	10.5.2.52/672
M1_C0_INFO4	0x4024	Information register 4 of channel 1 of ICU1	10.5.2.53/672
M1_C0_INFO5	0x4028	Information register 5 of channel 1 of ICU1	10.5.2.54/672
M1_C0_INFO6	0x402C	Information register 6 of channel 1 of ICU1	10.5.2.55/673
M1_C0_INFO7	0x4030	Information register 7 of channel 1 of ICU1	10.5.2.56/673

Register	Offset	Description	Section/Page
M1_INTR_STA	0x5000	Channel1 interrupt status register of ICU1	10.5.2.57/673
M1_INTR_CLR	0x5004	Channel1 clear interrupt register of ICU1	10.5.2.58/673
M1_INTR_RAW	0x5008	Channel1 ICU1's raw interrupt status register	10.5.2.59/674
M1_INTR_MASK	0x500C	Channel1 ICU1 interrupt mask register	10.5.2.60/674
M1_C2_INTR_STA	0x6000	Channel2 interrupt status register of ICU1	10.5.2.61/674
M1_C2_INTR_CLR	0x6004	Channel2 clear interrupt register of ICU1	10.5.2.62/674
M1_C2_INTR_RAW	0x6008	channel2 ICU1's raw interrupt status register	10.5.2.63/675
M1_C2_INTR_MASK	0x600C	Channel2 ICU1 interrupt mask register	10.5.2.64/675
M1_C2_GEN	0x6010	Interrupt generation register of channel 2 of ICU1	10.5.2.65/675
M1_C2_INFO0	0x6014	Information register 0 of channel 2 of ICU1	10.5.2.66/676
M1_C2_INFO1	0x6018	Information register 1 of channel 2 of ICU1	10.5.2.67/676
M1_C2_INFO2	0x601C	Information register 2 of channel 2 of ICU1	10.5.2.68/676
M1_C2_INFO3	0x6020	Information register 3 of channel 2 of ICU1	10.5.2.69/676
M1_C2_INFO4	0x6024	Information register 4 of channel 2 of ICU1	10.5.2.70/676
M1_C2_INFO5	0x6028	Information register 5 of channel 2 of ICU1	10.5.2.71/677
M1_C2_INFO6	0x602C	Information register 6 of channel 2 of ICU1	10.5.2.72/677
M1_C2_INFO7	0x6030	Information register 7 of channel 2 of ICU1	10.5.2.73/677
M1_C3_INTR_STA	0x7000	Channel3 interrupt status register of ICU1	10.5.2.74/677
M1_C3_INTR_CLR	0x7004	Channel3 clear interrupt register of ICU1	10.5.2.75/678
M1_C3_INTR_RAW	0x7008	Channel3 ICU1's raw interrupt status register	10.5.2.76/678
M1_C3_INTR_MASK	0x700C	Channel3 ICU1 interrupt mask register	10.5.2.77/678
M1_C3_GEN	0x7010	Interrupt generation register of channel3 of ICU1	10.5.2.78/678
M1_C3_INFO0	0x7014	Information register 0 of channel 3 of ICU1	10.5.2.79/679
M1_C3_INFO1	0x7018	Information register 1 of channel 3 of ICU1	10.5.2.80/679
M1_C3_INFO2	0x701C	Information register 2 of channel 3 of ICU1	10.5.2.81/679

Register	Offset	Description	Section/Page
M1_C3_INFO3	0x7020	Information register 3 of channel 3 of ICU1	10.5.2.82/679
M1_C3_INFO4	0x7024	Information register 4 of channel 3 of ICU1	10.5.2.83/680
M1_C3_INFO5	0x7028	Information register 5 of channel 3 of ICU1	10.5.2.84/680
M1_C3_INFO6	0x702C	Information register 6 of channel 3 of ICU1	10.5.2.85/680
M1_C3_INFO7	0x7030	Information register 7 of channel 3 of ICU1	10.5.2.86/680
M2_C0_INTR_STA	0x8000	Channel1 interrupt status register of ICU2	10.5.2.87/681
M2_C0_INTR_CLR	0x8004	Channel1 clear interrupt register of ICU2	10.5.2.88/681
M2_C0_INTR_RAW	0x8008	Channel1 ICU2's raw interrupt status register	10.5.2.89/681
M2_C0_INTR_MASK	0x800C	Channel1 ICU2 interrupt mask register	10.5.2.90/681
M2_C0_GEN	0x8010	Interrupt generation register of channel 1 of ICU2	10.5.2.91/682
M2_C0_INFO0	0x8014	Information register 0 of channel 1 of ICU2	10.5.2.92/682
M2_C0_INFO1	0x8018	Information register 1 of channel 1 of ICU2	10.5.2.93/682
M2_C0_INFO2	0x801C	Information register 2 of channel 1 of ICU2	10.5.2.94/682
M2_C0_INFO3	0x8020	Information register 3 of channel 1 of ICU2	10.5.2.95/683
M2_C0_INFO4	0x8024	Information register 4 of channel 1 of ICU2	10.5.2.96/683
M2_C0_INFO5	0x8028	Information register 5 of channel 1 of ICU2	10.5.2.97/683
M2_C0_INFO6	0x802C	Information register 6 of channel 1 of ICU2	10.5.2.98/683
M2_C0_INFO7	0x8030	Information register 7 of channel 1 of ICU2	10.5.2.99/684
M2_C1_INTR_STA	0x9000	Channel2 interrupt status register of ICU2	10.5.2.100/684
M2_C1_INTR_CLR	0x9004	Channel2 clear interrupt register of ICU2	10.5.2.101/684
M2_C1_INTR_RAW	0x9008	Channel2 ICU2's raw interrupt status register	10.5.2.102/684
M2_C1_INTR_MASK	0x900C	Channel2 ICU2 interrupt mask register	10.5.2.103/685
M2_C1_GEN	0x9010	Interrupt generation register of channel 2 of ICU2	10.5.2.104/685
M2_C1_INFO0	0x9014	Information register 0 of channel 2 of ICU2	10.5.2.105/685
M2_C1_INFO1	0x9018	Information register 1 of channel 2 of ICU2	10.5.2.106/685
M2_C1_INFO2	0x901C	Information register 2 of channel 2 of ICU2	10.5.2.107/686

Register	Offset	Description	Section/Page
M2_C1_INFO3	0x9020	Information register 3 of channel 2 of ICU2	10.5.2.108/686
M2_C1_INFO4	0x9024	Information register 4 of channel 2 of ICU2	10.5.2.109/686
M2_C1_INFO5	0x9028	Information register 5 of channel 2 of ICU2	10.5.2.110/686
M2_C1_INFO6	0x902C	Information register 6 of channel 2 of ICU2	10.5.2.111/687
M2_C1_INFO7	0x9030	Information register 7 of channel 2 of ICU2	10.5.2.112/687
M2_INTR_STA	0xA000	Interrupt status register of ICU2	10.5.2.113/687
M2_INTR_CLR	0xA004	Clear interrupt register of ICU2	10.5.2.114/687
M2_INTR_RAW	0xA008	ICU2's raw interrupt status register	10.5.2.115/688
M2_INTR_MASK	0xA00C	ICU2 interrupt mask register	10.5.2.116/688
M2_C3_INTR_STA	0xB000	Channel3 interrupt status register of ICU2	10.5.2.117/688
M2_C3_INTR_CLR	0xB004	Channel3 clear interrupt register of ICU2	10.5.2.118/688
M2_C3_INTR_RAW	0xB008	Channel3 ICU2's raw interrupt status register	10.5.2.119/689
M2_C3_INTR_MASK	0xB00C	Channel3 ICU2 interrupt mask register	10.5.2.120/689
M2_C3_GEN	0xB010	Interrupt generation register of channel3 of ICU2	10.5.2.121/689
M2_C3_INFO0	0xB014	Information register 0 of channel 3 of ICU2	10.5.2.122/690
M2_C3_INFO1	0xB018	Information register 1 of channel 3 of ICU2	10.5.2.123/690
M2_C3_INFO2	0xB01C	Information register 2 of channel 3 of ICU2	10.5.2.124/690
M2_C3_INFO3	0xB020	Information register 3 of channel 3 of ICU2	10.5.2.125/690
M2_C3_INFO4	0xB024	Information register 4 of channel 3 of ICU2	10.5.2.126/690
M2_C3_INFO5	0xB028	Information register 5 of channel 3 of ICU2	10.5.2.127/691
M2_C3_INFO6	0xB02C	Information register 6 of channel 3 of ICU2	10.5.2.128/691
M2_C3_INFO7	0xB030	Information register 7 of channel 3 of ICU2	10.5.2.129/691
M3_C0_INTR_STA	0xC000	Channel1 interrupt status register of ICU3	10.5.2.130/691
M3_C0_INTR_CLR	0xC004	Channel1 clear interrupt register of ICU3	10.5.2.131/692
M3_C0_INTR_RAW	0xC008	Channel1 ICU3's raw interrupt status register	10.5.2.132/692
M3_C0_INTR_MASK	0xC00C	Channel1 ICU3 interrupt mask register	10.5.2.133/692
M3_C0_GEN	0xC010	Interrupt generation register of channel 1	10.5.2.134/692

Register	Offset	Description	Section/Page
		of ICU3	
M3_C0_INFO0	0xC014	Information register 0 of channel 1 of ICU3	10.5.2.135/693
M3_C0_INFO1	0xC018	Information register 1 of channel 1 of ICU3	10.5.2.136/693
M3_C0_INFO2	0xC01C	Information register 2 of channel 1 of ICU3	10.5.2.137/693
M3_C0_INFO3	0xC020	Information register 3 of channel 1 of ICU3	10.5.2.138/693
M3_C0_INFO4	0xC024	Information register 4 of channel 1 of ICU3	10.5.2.139/694
M3_C0_INFO5	0xC028	Information register 5 of channel 1 of ICU3	10.5.2.140/694
M3_C0_INFO6	0xC02C	Information register 6 of channel 1 of ICU3	10.5.2.141/694
M3_C0_INFO7	0xC030	Information register 7 of channel 1 of ICU3	10.5.2.142/694
M3_C1_INTR_STA	0xD000	Channel2 interrupt status register of ICU3	10.5.2.143/695
M3_C1_INTR_CLR	0xD004	Channel2 clear interrupt register of ICU3	10.5.2.144/695
M3_C1_INTR_RAW	0xD008	Channel2 ICU3's raw interrupt status register	10.5.2.145/695
M3_C1_INTR_MASK	0xD00C	Channel2 ICU3 interrupt mask register	10.5.2.146/695
M3_C1_GEN	0xD010	Interrupt generation register of channel 2 of ICU3	10.5.2.147/696
M3_C1_INFO0	0xD014	Information register 0 of channel 2 of ICU3	10.5.2.148/696
M3_C1_INFO1	0xD018	Information register 1 of channel 2 of ICU3	10.5.2.149/696
M3_C1_INFO2	0xD01C	Information register 2 of channel 2 of ICU3	10.5.2.150/696
M3_C1_INFO3	0xD020	Information register 3 of channel 2 of ICU3	10.5.2.151/697
M3_C1_INFO4	0xD024	Information register 4 of channel 2 of ICU3	10.5.2.152/697
M3_C1_INFO5	0xD028	Information register 5 of channel 2 of ICU3	10.5.2.153/697
M3_C1_INFO6	0xD02C	Information register 6 of channel 2 of ICU3	10.5.2.154/697
M3_C1_INFO7	0xD030	Information register 7 of channel 2 of ICU3	10.5.2.155/698
M3_C2_INTR_STA	0xE000	Channel3 interrupt status register of ICU3	10.5.2.156/698
M3_C2_INTR_CLR	0xE004	Channel3 clear interrupt register of ICU3	10.5.2.157/698
M3_C2_INTR_RAW	0xE008	Channel3 ICU3's raw interrupt status register	10.5.2.158/698
M3_C2_INTR_MASK	0xE00C	Channel3 ICU3 interrupt mask register	10.5.2.159/699
M3_C2_GEN	0xE010	Interrupt generation register of channel3	10.5.2.160/699

Register	Offset	Description	Section/Page
		of ICU3	
M3_C2_INFO0	0xE014	Information register 0 of channel 3 of ICU3	10.5.2.161/699
M3_C2_INFO1	0xE018	Information register 1 of channel 3 of ICU3	10.5.2.162/699
M3_C2_INFO2	0xE01C	Information register 2 of channel 3 of ICU3	10.5.2.163/700
M3_C2_INFO3	0xE020	Information register 3 of channel 3 of ICU3	10.5.2.164/700
M3_C2_INFO4	0xE024	Information register 4 of channel 3 of ICU3	10.5.2.165/700
M3_C2_INFO5	0xE028	Information register 5 of channel 3 of ICU3	10.5.2.166/700
M3_C2_INFO6	0xE02C	Information register 6 of channel 3 of ICU3	10.5.2.167/701
M3_C2_INFO7	0xE030	Information register 7 of channel 3 of ICU3	10.5.2.168/701
M3_INTR_STA	0xF000	Interrupt status register of ICU3	10.5.2.169/701
M3_INTR_CLR	0xF004	Clear interrupt register of ICU3	10.5.2.170/701
M3_INTR_RAW	0xF008	ICU3's raw interrupt status register	10.5.2.171/702
M3_INTR_MASK	0xF00C	ICU3 interrupt mask register	10.5.2.172/702
IP_ID	0xFFFC	IP_ID	10.5.2.173/702

10.5.2 Register and Field Description

10.5.2.1 M0_INTR_STA

- Description: Interrupt status register of ICU0
- Offset: 0x0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M0_INTR_STA	RO	M0_INTR_STA Value After Reset: 0x0

10.5.2.2 M0_INTR_CLR

- Description: Clear interrupt register of ICU0
- Offset: 0x4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M0_INTR_CLR	WO	M0_INTR_CLR Value After Reset: 0x0

10.5.2.3 M0_INTR_RAW

- Description: ICU0's raw interrupt status register
- Offset: 0x8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M0_INTR_RAW	RO	M0_INTR_RAW Value After Reset: 0x0

10.5.2.4 M0_INTR_MASK

- Description: ICU0 interrupt mask register
- Offset: 0xC
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M0_INTR_MASK	RW	M0_INTR_MASK Value After Reset: 0x0

10.5.2.5 M0_C1_INTR_STA

- Description: Channel1 interrupt status register of ICU0
- Offset: 0x1000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M0_C1_INTR_STA	RO	M0_C1_INTR_STA Value After Reset: 0x0

10.5.2.6 M0_C1_INTR_CLR

- Description: Channel1 clear interrupt register of ICU0

- Offset: 0x1004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M0_C1_INTR_CLR	WO	M0_C1_INTR_CLR Value After Reset: 0x0

10.5.2.7 M0_C1_INTR_RAW

- Description: Channel1 ICU0's raw interrupt status register
- Offset: 0x1008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M0_C1_INTR_RAW	RO	M0_C1_INTR_RAW Value After Reset: 0x0

10.5.2.8 M0_C1_INTR_MASK

- Description: Channel1 ICU0 interrupt mask register
- Offset: 0x100C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M0_C1_INTR_MASK	RW	M0_C1_INTR_MASK Value After Reset: 0x0

10.5.2.9 M0_C1_GEN

- Description: Interrupt generation register of channel 1 of ICU0
- Offset: 0x1010
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	M0_C1_GEN	RW	M0_C1_GEN Value After Reset: 0x0

10.5.2.10 M0_C1_INFO0

- Description: Information register 0 of channel 1 of ICU0
- Offset: 0x1014
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C1_INFO0	RW	M0_C1_INFO0 Value After Reset: 0x0

10.5.2.11 M0_C1_INFO1

- Description: Information register 1 of channel 1 of ICU0
- Offset: 0x1018
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C1_INFO1	RW	M0_C1_INFO1 Value After Reset: 0x0

10.5.2.12 M0_C1_INFO2

- Description: Information register 2 of channel 1 of ICU0
- Offset: 0x101C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C1_INFO2	RW	M0_C1_INFO2 Value After Reset: 0x0

10.5.2.13 M0_C1_INFO3

- Description: Information register 3 of channel 1 of ICU0
- Offset: 0x1020
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C1_INFO3	RW	M0_C1_INFO3 Value After Reset: 0x0

10.5.2.14 M0_C1_INFO4

- Description: Information register 4 of channel 1 of ICU0

- Offset: 0x1024
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C1_INFO4	RW	M0_C1_INFO4 Value After Reset: 0x0

10.5.2.15 M0_C1_INFO5

- Description: Information register 5 of channel 1 of ICU0
- Offset: 0x1028
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C1_INFO5	RW	M0_C1_INFO5 Value After Reset: 0x0

10.5.2.16 M0_C1_INFO6

- Description: Information register 6 of channel 1 of ICU0
- Offset: 0x102C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C1_INFO6	RW	M0_C1_INFO6 Value After Reset: 0x0

10.5.2.17 M0_C1_INFO7

- Description: Information register 7 of channel 1 of ICU0
- Offset: 0x1030
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C1_INFO7	RW	M0_C1_INFO7 Value After Reset: 0x0

10.5.2.18 M0_C2_INTR_STA

- Description: Channel2 interrupt status register of ICU0
- Offset: 0x2000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M0_C2_INTR_STA	RO	M0_C2_INTR_STA Value After Reset: 0x0

10.5.2.19 M0_C2_INTR_CLR

- Description: Channel2 clear interrupt register of ICU0
- Offset: 0x2004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M0_C2_INTR_CLR	WO	M0_C2_INTR_CLR Value After Reset: 0x0

10.5.2.20 M0_C2_INTR_RAW

- Description: Channel2 ICU0's raw interrupt status register
- Offset: 0x2008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M0_C2_INTR_RAW	RO	M0_C2_INTR_RAW Value After Reset: 0x0

10.5.2.21 M0_C2_INTR_MASK

- Description: Channel2 ICU0 interrupt mask register
- Offset: 0x200C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M0_C2_INTR_MASK	RW	M0_C2_INTR_MASK Value After Reset: 0x0

10.5.2.22 M0_C2_GEN

- Description: Interrupt generation register of channel 2 of ICU0

- Offset: 0x2010
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	M0_C2_GEN	RW	M0_C2_GEN Value After Reset: 0x0

10.5.2.23 M0_C2_INFO0

- Description: Information register 0 of channel 2 of ICU0
- Offset: 0x2014
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C2_INFO0	RW	M0_C2_INFO0 Value After Reset: 0x0

10.5.2.24 M0_C2_INFO1

- Description: Information register 1 of channel 2 of ICU0
- Offset: 0x2018
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C2_INFO1	RW	M0_C2_INFO1 Value After Reset: 0x0

10.5.2.25 M0_C2_INFO2

- Description: Information register 2 of channel 2 of ICU0
- Offset: 0x201C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C2_INFO2	RW	M0_C2_INFO2 Value After Reset: 0x0

10.5.2.26 M0_C2_INFO3

- Description: Information register 3 of channel 2 of ICU0
- Offset: 0x2020

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C2_INFO3	RW	M0_C2_INFO3 Value After Reset: 0x0

10.5.2.27 M0_C2_INFO4

- Description: Information register 4 of channel 2 of ICU0
- Offset: 0x2024
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C2_INFO4	RW	M0_C2_INFO4 Value After Reset: 0x0

10.5.2.28 M0_C2_INFO5

- Description: Information register 5 of channel 2 of ICU0
- Offset: 0x2028
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C2_INFO5	RW	M0_C2_INFO5 Value After Reset: 0x0

10.5.2.29 M0_C2_INFO6

- Description: Information register 6 of channel 2 of ICU0
- Offset: 0x202C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C2_INFO6	RW	M0_C2_INFO6 Value After Reset: 0x0

10.5.2.30 M0_C2_INFO7

- Description: Information register 7 of channel 2 of ICU0
- Offset: 0x2030
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C2_INFO7	RW	M0_C2_INFO7 Value After Reset: 0x0

10.5.2.31 M0_C3_INTR_STA

- Description: Channel3 interrupt status register of ICU0
- Offset: 0x3000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M0_C3_INTR_STA	RO	M0_C3_INTR_STA Value After Reset: 0x0

10.5.2.32 M0_C3_INTR_CLR

- Description: Channel3 clear interrupt register of ICU0
- Offset: 0x3004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M0_C3_INTR_CLR	WO	M0_C3_INTR_CLR Value After Reset: 0x0

10.5.2.33 M0_C3_INTR_RAW

- Description: Channel3 ICU0's raw interrupt status register
- Offset: 0x3008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M0_C3_INTR_RAW	RO	M0_C3_INTR_RAW Value After Reset: 0x0

10.5.2.34 M0_C3_INTR_MASK

- Description: Channel3 ICU0 interrupt mask register
- Offset: 0x300C

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M0_C3_INTR_MASK	RW	M0_C3_INTR_MASK Value After Reset: 0x0

10.5.2.35 M0_C3_GEN

- Description: Interrupt generation register of channel3 of ICU0
- Offset: 0x3010
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	M0_C3_GEN	RW	M0_C3_GEN Value After Reset: 0x0

10.5.2.36 M0_C3_INFO0

- Description: Information register 0 of channel 3 of ICU0
- Offset: 0x3014
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C3_INFO0	RW	M0_C3_INFO0 Value After Reset: 0x0

10.5.2.37 M0_C3_INFO1

- Description: Information register 1 of channel 3 of ICU0
- Offset: 0x3018
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C3_INFO1	RW	M0_C3_INFO1 Value After Reset: 0x0

10.5.2.38 M0_C3_INFO2

- Description: Information register 2 of channel 3 of ICU0
- Offset: 0x301C

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C3_INFO2	RW	M0_C3_INFO2 Value After Reset: 0x0

10.5.2.39 M0_C3_INFO3

- Description: Information register 3 of channel 3 of ICU0
- Offset: 0x3020
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C3_INFO3	RW	M0_C3_INFO3 Value After Reset: 0x0

10.5.2.40 M0_C3_INFO4

- Description: Information register 4 of channel 3 of ICU0
- Offset: 0x3024
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C3_INFO4	RW	M0_C3_INFO4 Value After Reset: 0x0

10.5.2.41 M0_C3_INFO5

- Description: Information register 5 of channel 3 of ICU0
- Offset: 0x3028
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C3_INFO5	RW	M0_C3_INFO5 Value After Reset: 0x0

10.5.2.42 M0_C3_INFO6

- Description: Information register 6 of channel 3 of ICU0
- Offset: 0x302C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C3_INFO6	RW	M0_C3_INFO6 Value After Reset: 0x0

10.5.2.43 M0_C3_INFO7

- Description: Information register 7 of channel 3 of ICU0
- Offset: 0x3030
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M0_C3_INFO7	RW	M0_C3_INFO7 Value After Reset: 0x0

10.5.2.44 M1_C0_INTR_STA

- Description: Interrupt status register of ICU1
- Offset: 0x4000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M1_C0_INTR_STA	RO	M1_C0_INTR_STA Value After Reset: 0x0

10.5.2.45 M1_C0_INTR_CLR

- Description: Clear interrupt register of ICU1
- Offset: 0x4004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M1_C0_INTR_CLR	WO	M1_C0_INTR_CLR Value After Reset: 0x0

10.5.2.46 M1_C0_INTR_RAW

- Description: ICU1's raw interrupt status register
- Offset: 0x4008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M1_C0_INTR_RAW	RO	M1_C0_INTR_RAW Value After Reset: 0x0

10.5.2.47 M1_C0_INTR_MASK

- Description: ICU1 interrupt mask register
- Offset: 0x400C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M1_C0_INTR_MASK	RW	M1_C0_INTR_MASK Value After Reset: 0x0

10.5.2.48 M1_C0_GEN

- Description: Interrupt generation register of channel 1 of ICU1
- Offset: 0x4010
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	M1_C0_GEN	RW	M1_C0_GEN Value After Reset: 0x0

10.5.2.49 M1_C0_INFO0

- Description: Information register 0 of channel 1 of ICU1
- Offset: 0x4014
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C0_INFO0	RW	M1_C0_INFO0 Value After Reset: 0x0

10.5.2.50 M1_C0_INFO1

- Description: Information register 1 of channel 1 of ICU1
- Offset: 0x4018

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C0_INFO1	RW	M1_C0_INFO1 Value After Reset: 0x0

10.5.2.51 M1_C0_INFO2

- Description: Information register 2 of channel 1 of ICU1
- Offset: 0x401C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C0_INFO2	RW	M1_C0_INFO2 Value After Reset: 0x0

10.5.2.52 M1_C0_INFO3

- Description: Information register 3 of channel 1 of ICU1
- Offset: 0x4020
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C0_INFO3	RW	M1_C0_INFO3 Value After Reset: 0x0

10.5.2.53 M1_C0_INFO4

- Description: Information register 4 of channel 1 of ICU1
- Offset: 0x4024
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C0_INFO4	RW	M1_C0_INFO4 Value After Reset: 0x0

10.5.2.54 M1_C0_INFO5

- Description: Information register 5 of channel 1 of ICU1
- Offset: 0x4028
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C0_INFO5	RW	M1_C0_INFO5 Value After Reset: 0x0

10.5.2.55 M1_C0_INFO6

- Description: Information register 6 of channel 1 of ICU1
- Offset: 0x402C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C0_INFO6	RW	M1_C0_INFO6 Value After Reset: 0x0

10.5.2.56 M1_C0_INFO7

- Description: Information register 7 of channel 1 of ICU1
- Offset: 0x4030
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C0_INFO7	RW	M1_C0_INFO7 Value After Reset: 0x0

10.5.2.57 M1_INTR_STA

- Description: Channel1 interrupt status register of ICU1
- Offset: 0x5000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M1_INTR_STA	RO	M1_INTR_STA Value After Reset: 0x0

10.5.2.58 M1_INTR_CLR

- Description: Channel1 clear interrupt register of ICU1
- Offset: 0x5004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M1_INTR_CLR	WO	M1_INTR_CLR Value After Reset: 0x0

10.5.2.59 M1_INTR_RAW

- Description: Channel1 ICU1's raw interrupt status register
- Offset: 0x5008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M1_INTR_RAW	RO	M1_INTR_RAW Value After Reset: 0x0

10.5.2.60 M1_INTR_MASK

- Description: Channel1 ICU1 interrupt mask register
- Offset: 0x500C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M1_INTR_MASK	RW	M1_INTR_MASK Value After Reset: 0x0

10.5.2.61 M1_C2_INTR_STA

- Description: Channel2 interrupt status register of ICU1
- Offset: 0x6000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M1_C2_INTR_STA	RO	M1_C2_INTR_STA Value After Reset: 0x0

10.5.2.62 M1_C2_INTR_CLR

- Description: Channel2 clear interrupt register of ICU1

- Offset: 0x6004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M1_C2_INTR_CLR	WO	M1_C2_INTR_CLR Value After Reset: 0x0

10.5.2.63 M1_C2_INTR_RAW

- Description: Channel2 ICU1's raw interrupt status register
- Offset: 0x6008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M1_C2_INTR_RAW	RO	M1_C2_INTR_RAW Value After Reset: 0x0

10.5.2.64 M1_C2_INTR_MASK

- Description: Channel2 ICU1 interrupt mask register
- Offset: 0x600C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M1_C2_INTR_MASK	RW	M1_C2_INTR_MASK Value After Reset: 0x0

10.5.2.65 M1_C2_GEN

- Description: Interrupt generation register of channel 2 of ICU1
- Offset: 0x6010
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	M1_C2_GEN	RW	M1_C2_GEN Value After Reset: 0x0

10.5.2.66 M1_C2_INFO0

- Description: Information register 0 of channel 2 of ICU1
- Offset: 0x6014
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C2_INFO0	RW	M1_C2_INFO0 Value After Reset: 0x0

10.5.2.67 M1_C2_INFO1

- Description: Information register 1 of channel 2 of ICU1
- Offset: 0x6018
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C2_INFO1	RW	M1_C2_INFO1 Value After Reset: 0x0

10.5.2.68 M1_C2_INFO2

- Description: Information register 2 of channel 2 of ICU1
- Offset: 0x601C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C2_INFO2	RW	M1_C2_INFO2 Value After Reset: 0x0

10.5.2.69 M1_C2_INFO3

- Description: Information register 3 of channel 2 of ICU1
- Offset: 0x6020
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C2_INFO3	RW	M1_C2_INFO3 Value After Reset: 0x0

10.5.2.70 M1_C2_INFO4

- Description: Information register 4 of channel 2 of ICU1

- Offset: 0x6024
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C2_INFO4	RW	M1_C2_INFO4 Value After Reset: 0x0

10.5.2.71 M1_C2_INFO5

- Description: Information register 5 of channel 2 of ICU1
- Offset: 0x6028
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C2_INFO5	RW	M1_C2_INFO5 Value After Reset: 0x0

10.5.2.72 M1_C2_INFO6

- Description: Information register 6 of channel 2 of ICU1
- Offset: 0x602C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C2_INFO6	RW	M1_C2_INFO6 Value After Reset: 0x0

10.5.2.73 M1_C2_INFO7

- Description: Information register 7 of channel 2 of ICU1
- Offset: 0x6030
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C2_INFO7	RW	M1_C2_INFO7 Value After Reset: 0x0

10.5.2.74 M1_C3_INTR_STA

- Description: Channel3 interrupt status register of ICU1
- Offset: 0x7000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M1_C3_INTR_STA	RO	M1_C3_INTR_STA Value After Reset: 0x0

10.5.2.75 M1_C3_INTR_CLR

- Description: Channel3 clear interrupt register of ICU1
- Offset: 0x7004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M1_C3_INTR_CLR	WO	M1_C3_INTR_CLR Value After Reset: 0x0

10.5.2.76 M1_C3_INTR_RAW

- Description: Channel3 ICU1's raw interrupt status register
- Offset: 0x7008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M1_C3_INTR_RAW	RO	M1_C3_INTR_RAW Value After Reset: 0x0

10.5.2.77 M1_C3_INTR_MASK

- Description: Channel3 ICU1 interrupt mask register
- Offset: 0x700C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M1_C3_INTR_MASK	RW	M1_C3_INTR_MASK Value After Reset: 0x0

10.5.2.78 M1_C3_GEN

- Description: Interrupt generation register of channel3 of ICU1

- Offset: 0x7010
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	M1_C3_GEN	RW	M1_C3_GEN Value After Reset: 0x0

10.5.2.79 M1_C3_INFO0

- Description: Information register 0 of channel 3 of ICU1
- Offset: 0x7014
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C3_INFO0	RW	M1_C3_INFO0 Value After Reset: 0x0

10.5.2.80 M1_C3_INFO1

- Description: Information register 1 of channel 3 of ICU1
- Offset: 0x7018
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C3_INFO1	RW	M1_C3_INFO1 Value After Reset: 0x0

10.5.2.81 M1_C3_INFO2

- Description: Information register 2 of channel 3 of ICU1
- Offset: 0x701C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C3_INFO2	RW	M1_C3_INFO2 Value After Reset: 0x0

10.5.2.82 M1_C3_INFO3

- Description: Information register 3 of channel 3 of ICU1
- Offset: 0x7020

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C3_INFO3	RW	M1_C3_INFO3 Value After Reset: 0x0

10.5.2.83 M1_C3_INFO4

- Description: Information register 4 of channel 3 of ICU1
- Offset: 0x7024
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C3_INFO4	RW	M1_C3_INFO4 Value After Reset: 0x0

10.5.2.84 M1_C3_INFO5

- Description: Information register 5 of channel 3 of ICU1
- Offset: 0x7028
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C3_INFO5	RW	M1_C3_INFO5 Value After Reset: 0x0

10.5.2.85 M1_C3_INFO6

- Description: Information register 6 of channel 3 of ICU1
- Offset: 0x702C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C3_INFO6	RW	M1_C3_INFO6 Value After Reset: 0x0

10.5.2.86 M1_C3_INFO7

- Description: Information register 7 of channel 3 of ICU1
- Offset: 0x7030
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M1_C3_INFO7	RW	M1_C3_INFO7 Value After Reset: 0x0

10.5.2.87 M2_C0_INTR_STA

- Description: Channel1 interrupt status register of ICU2
- Offset: 0x8000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M2_C0_INTR_STA	RO	M2_C0_INTR_STA Value After Reset: 0x0

10.5.2.88 M2_C0_INTR_CLR

- Description: Channel1 clear interrupt register of ICU2
- Offset: 0x8004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M2_C0_INTR_CLR	WO	M2_C0_INTR_CLR Value After Reset: 0x0

10.5.2.89 M2_C0_INTR_RAW

- Description: Channel1 ICU2's raw interrupt status register
- Offset: 0x8008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M2_C0_INTR_RAW	RO	M2_C0_INTR_RAW Value After Reset: 0x0

10.5.2.90 M2_C0_INTR_MASK

- Description: Channel1 ICU2 interrupt mask register
- Offset: 0x800C

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M2_C0_INTR_MASK	RW	M2_C0_INTR_MASK Value After Reset: 0x0

10.5.2.91 M2_C0_GEN

- Description: Interrupt generation register of channel 1 of ICU2
- Offset: 0x8010
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	M2_C0_GEN	RW	M2_C0_GEN Value After Reset: 0x0

10.5.2.92 M2_C0_INFO0

- Description: Information register 0 of channel 1 of ICU2
- Offset: 0x8014
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C0_INFO0	RW	M2_C0_INFO0 Value After Reset: 0x0

10.5.2.93 M2_C0_INFO1

- Description: Information register 1 of channel 1 of ICU2
- Offset: 0x8018
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C0_INFO1	RW	M2_C0_INFO1 Value After Reset: 0x0

10.5.2.94 M2_C0_INFO2

- Description: Information register 2 of channel 1 of ICU2
- Offset: 0x801C

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C0_INFO2	RW	M2_C0_INFO2 Value After Reset: 0x0

10.5.2.95 M2_C0_INFO3

- Description: Information register 3 of channel 1 of ICU2
- Offset: 0x8020
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C0_INFO3	RW	M2_C0_INFO3 Value After Reset: 0x0

10.5.2.96 M2_C0_INFO4

- Description: Information register 4 of channel 1 of ICU2
- Offset: 0x8024
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C0_INFO4	RW	M2_C0_INFO4 Value After Reset: 0x0

10.5.2.97 M2_C0_INFO5

- Description: Information register 5 of channel 1 of ICU2
- Offset: 0x8028
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C0_INFO5	RW	M2_C0_INFO5 Value After Reset: 0x0

10.5.2.98 M2_C0_INFO6

- Description: Information register 6 of channel 1 of ICU2
- Offset: 0x802C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C0_INFO6	RW	M2_C0_INFO6 Value After Reset: 0x0

10.5.2.99 M2_C0_INFO7

- Description: Information register 7 of channel 1 of ICU2
- Offset: 0x8030
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C0_INFO7	RW	M2_C0_INFO7 Value After Reset: 0x0

10.5.2.100 M2_C1_INTR_STA

- Description: Channel2 interrupt status register of ICU2
- Offset: 0x9000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M2_C1_INTR_STA	RO	M2_C1_INTR_STA Value After Reset: 0x0

10.5.2.101 M2_C1_INTR_CLR

- Description: Channel2 clear interrupt register of ICU2
- Offset: 0x9004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M2_C1_INTR_CLR	WO	M2_C1_INTR_CLR Value After Reset: 0x0

10.5.2.102 M2_C1_INTR_RAW

- Description: Channel2 ICU2's raw interrupt status register
- Offset: 0x9008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M2_C1_INTR_RAW	RO	M2_C1_INTR_RAW Value After Reset: 0x0

10.5.2.103 M2_C1_INTR_MASK

- Description: Channel2 ICU2 interrupt mask register
- Offset: 0x900C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M2_C1_INTR_MASK	RW	M2_C1_INTR_MASK Value After Reset: 0x0

10.5.2.104 M2_C1_GEN

- Description: Interrupt generation register of channel 2 of ICU2
- Offset: 0x9010
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	M2_C1_GEN	RW	M2_C1_GEN Value After Reset: 0x0

10.5.2.105 M2_C1_INFO0

- Description: Information register 0 of channel 2 of ICU2
- Offset: 0x9014
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C1_INFO0	RW	M2_C1_INFO0 Value After Reset: 0x0

10.5.2.106 M2_C1_INFO1

- Description: Information register 1 of channel 2 of ICU2
- Offset: 0x9018

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C1_INFO1	RW	M2_C1_INFO1 Value After Reset: 0x0

10.5.2.107 M2_C1_INFO2

- Description: Information register 2 of channel 2 of ICU2
- Offset: 0x901C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C1_INFO2	RW	M2_C1_INFO2 Value After Reset: 0x0

10.5.2.108 M2_C1_INFO3

- Description: Information register 3 of channel 2 of ICU2
- Offset: 0x9020
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C1_INFO3	RW	M2_C1_INFO3 Value After Reset: 0x0

10.5.2.109 M2_C1_INFO4

- Description: Information register 4 of channel 2 of ICU2
- Offset: 0x9024
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C1_INFO4	RW	M2_C1_INFO4 Value After Reset: 0x0

10.5.2.110 M2_C1_INFO5

- Description: Information register 5 of channel 2 of ICU2
- Offset: 0x9028
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C1_INFO5	RW	M2_C1_INFO5 Value After Reset: 0x0

10.5.2.111 M2_C1_INFO6

- Description: Information register 6 of channel 2 of ICU2
- Offset: 0x902C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C1_INFO6	RW	M2_C1_INFO6 Value After Reset: 0x0

10.5.2.112 M2_C1_INFO7

- Description: Information register 7 of channel 2 of ICU2
- Offset: 0x9030
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C1_INFO7	RW	M2_C1_INFO7 Value After Reset: 0x0

10.5.2.113 M2_INTR_STA

- Description: Interrupt status register of ICU2
- Offset: 0xA000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M2_INTR_STA	RO	M2_INTR_STA Value After Reset: 0x0

10.5.2.114 M2_INTR_CLR

- Description: Clear interrupt register of ICU2
- Offset: 0xA004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M2_INTR_CLR	WO	M2_INTR_CLR Value After Reset: 0x0

10.5.2.115 M2_INTR_RAW

- Description: ICU2's raw interrupt status register
- Offset: 0xA008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M2_INTR_RAW	RO	M2_INTR_RAW Value After Reset: 0x0

10.5.2.116 M2_INTR_MASK

- Description: ICU2 interrupt mask register
- Offset: 0xA00C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M2_INTR_MASK	RW	M2_INTR_MASK Value After Reset: 0x0

10.5.2.117 M2_C3_INTR_STA

- Description: Channel3 interrupt status register of ICU2
- Offset: 0xB000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M2_C3_INTR_STA	RO	M2_C3_INTR_STA Value After Reset: 0x0

10.5.2.118 M2_C3_INTR_CLR

- Description: Channel3 clear interrupt register of ICU2

- Offset: 0xB004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M2_C3_INTR_CLR	WO	M2_C3_INTR_CLR Value After Reset: 0x0

10.5.2.119 M2_C3_INTR_RAW

- Description: Channel3 ICU2's raw interrupt status register
- Offset: 0xB008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M2_C3_INTR_RAW	RO	M2_C3_INTR_RAW Value After Reset: 0x0

10.5.2.120 M2_C3_INTR_MASK

- Description: Channel3 ICU2 interrupt mask register
- Offset: 0xB00C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M2_C3_INTR_MASK	RW	M2_C3_INTR_MASK Value After Reset: 0x0

10.5.2.121 M2_C3_GEN

- Description: Interrupt generation register of channel3 of ICU2
- Offset: 0xB010
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	M2_C3_GEN	RW	M2_C3_GEN Value After Reset: 0x0

10.5.2.122 M2_C3_INFO0

- Description: Information register 0 of channel 3 of ICU2
- Offset: 0xB014
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C3_INFO0	RW	M2_C3_INFO0 Value After Reset: 0x0

10.5.2.123 M2_C3_INFO1

- Description: Information register 1 of channel 3 of ICU2
- Offset: 0xB018
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C3_INFO1	RW	M2_C3_INFO1 Value After Reset: 0x0

10.5.2.124 M2_C3_INFO2

- Description: Information register 2 of channel 3 of ICU2
- Offset: 0xB01C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C3_INFO2	RW	M2_C3_INFO2 Value After Reset: 0x0

10.5.2.125 M2_C3_INFO3

- Description: Information register 3 of channel 3 of ICU2
- Offset: 0xB020
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C3_INFO3	RW	M2_C3_INFO3 Value After Reset: 0x0

10.5.2.126 M2_C3_INFO4

- Description: Information register 4 of channel 3 of ICU2

- Offset: 0xB024
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C3_INFO4	RW	M2_C3_INFO4 Value After Reset: 0x0

10.5.2.127 M2_C3_INFO5

- Description: Information register 5 of channel 3 of ICU2
- Offset: 0xB028
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C3_INFO5	RW	M2_C3_INFO5 Value After Reset: 0x0

10.5.2.128 M2_C3_INFO6

- Description: Information register 6 of channel 3 of ICU2
- Offset: 0xB02C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C3_INFO6	RW	M2_C3_INFO6 Value After Reset: 0x0

10.5.2.129 M2_C3_INFO7

- Description: Information register 7 of channel 3 of ICU2
- Offset: 0xB030
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M2_C3_INFO7	RW	M2_C3_INFO7 Value After Reset: 0x0

10.5.2.130 M3_C0_INTR_STA

- Description: Channel1 interrupt status register of ICU3
- Offset: 0xC000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M3_C0_INTR_STA	RO	M3_C0_INTR_STA Value After Reset: 0x0

10.5.2.131 M3_C0_INTR_CLR

- Description: Channel1 clear interrupt register of ICU3
- Offset: 0xC004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M3_C0_INTR_CLR	WO	M3_C0_INTR_CLR Value After Reset: 0x0

10.5.2.132 M3_C0_INTR_RAW

- Description: Channel1 ICU3's raw interrupt status register
- Offset: 0xC008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M3_C0_INTR_RAW	RO	M3_C0_INTR_RAW Value After Reset: 0x0

10.5.2.133 M3_C0_INTR_MASK

- Description: Channel1 ICU3 interrupt mask register
- Offset: 0xC00C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M3_C0_INTR_MASK	RW	M3_C0_INTR_MASK Value After Reset: 0x0

10.5.2.134 M3_C0_GEN

- Description: Interrupt generation register of channel 1 of ICU3

- Offset: 0xC010
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	M3_C0_GEN	RW	M3_C0_GEN Value After Reset: 0x0

10.5.2.135 M3_C0_INFO0

- Description: Information register 0 of channel 1 of ICU3
- Offset: 0xC014
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C0_INFO0	RW	M3_C0_INFO0 Value After Reset: 0x0

10.5.2.136 M3_C0_INFO1

- Description: Information register 1 of channel 1 of ICU3
- Offset: 0xC018
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C0_INFO1	RW	M3_C0_INFO1 Value After Reset: 0x0

10.5.2.137 M3_C0_INFO2

- Description: Information register 2 of channel 1 of ICU3
- Offset: 0xC01C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C0_INFO2	RW	M3_C0_INFO2 Value After Reset: 0x0

10.5.2.138 M3_C0_INFO3

- Description: Information register 3 of channel 1 of ICU3
- Offset: 0xC020

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C0_INFO3	RW	M3_C0_INFO3 Value After Reset: 0x0

10.5.2.139 M3_C0_INFO4

- Description: Information register 4 of channel 1 of ICU3
- Offset: 0xC024
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C0_INFO4	RW	M3_C0_INFO4 Value After Reset: 0x0

10.5.2.140 M3_C0_INFO5

- Description: Information register 5 of channel 1 of ICU3
- Offset: 0xC028
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C0_INFO5	RW	M3_C0_INFO5 Value After Reset: 0x0

10.5.2.141 M3_C0_INFO6

- Description: Information register 6 of channel 1 of ICU3
- Offset: 0xC02C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C0_INFO6	RW	M3_C0_INFO6 Value After Reset: 0x0

10.5.2.142 M3_C0_INFO7

- Description: Information register 7 of channel 1 of ICU3
- Offset: 0xC030
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C0_INFO7	RW	M3_C0_INFO7 Value After Reset: 0x0

10.5.2.143 M3_C1_INTR_STA

- Description: Channel2 interrupt status register of ICU3
- Offset: 0xD000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M3_C1_INTR_STA	RO	M3_C1_INTR_STA Value After Reset: 0x0

10.5.2.144 M3_C1_INTR_CLR

- Description: Channel2 clear interrupt register of ICU3
- Offset: 0xD004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M3_C1_INTR_CLR	WO	M3_C1_INTR_CLR Value After Reset: 0x0

10.5.2.145 M3_C1_INTR_RAW

- Description: Channel2 ICU3's raw interrupt status register
- Offset: 0xD008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M3_C1_INTR_RAW	RO	M3_C1_INTR_RAW Value After Reset: 0x0

10.5.2.146 M3_C1_INTR_MASK

- Description: Channel2 ICU3 interrupt mask register
- Offset: 0xD00C

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M3_C1_INTR_MASK	RW	M3_C1_INTR_MASK Value After Reset: 0x0

10.5.2.147 M3_C1_GEN

- Description: Interrupt generation register of channel 2 of ICU3
- Offset: 0xD010
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	M3_C1_GEN	RW	M3_C1_GEN Value After Reset: 0x0

10.5.2.148 M3_C1_INFO0

- Description: Information register 0 of channel 2 of ICU3
- Offset: 0xD014
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C1_INFO0	RW	M3_C1_INFO0 Value After Reset: 0x0

10.5.2.149 M3_C1_INFO1

- Description: Information register 1 of channel 2 of ICU3
- Offset: 0xD018
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C1_INFO1	RW	M3_C1_INFO1 Value After Reset: 0x0

10.5.2.150 M3_C1_INFO2

- Description: Information register 2 of channel 2 of ICU3
- Offset: 0xD01C

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C1_INFO2	RW	M3_C1_INFO2 Value After Reset: 0x0

10.5.2.151 M3_C1_INFO3

- Description: Information register 3 of channel 2 of ICU3
- Offset: 0xD020
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C1_INFO3	RW	M3_C1_INFO3 Value After Reset: 0x0

10.5.2.152 M3_C1_INFO4

- Description: Information register 4 of channel 2 of ICU3
- Offset: 0xD024
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C1_INFO4	RW	M3_C1_INFO4 Value After Reset: 0x0

10.5.2.153 M3_C1_INFO5

- Description: Information register 5 of channel 2 of ICU3
- Offset: 0xD028
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C1_INFO5	RW	M3_C1_INFO5 Value After Reset: 0x0

10.5.2.154 M3_C1_INFO6

- Description: Information register 6 of channel 2 of ICU3
- Offset: 0xD02C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C1_INFO6	RW	M3_C1_INFO6 Value After Reset: 0x0

10.5.2.155 M3_C1_INFO7

- Description: Information register 7 of channel 2 of ICU3
- Offset: 0xD030
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C1_INFO7	RW	M3_C1_INFO7 Value After Reset: 0x0

10.5.2.156 M3_C2_INTR_STA

- Description: Channel3 interrupt status register of ICU3
- Offset: 0xE000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M3_C2_INTR_STA	RO	M3_C2_INTR_STA Value After Reset: 0x0

10.5.2.157 M3_C2_INTR_CLR

- Description: Channel3 clear interrupt register of ICU3
- Offset: 0xE004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M3_C2_INTR_CLR	WO	M3_C2_INTR_CLR Value After Reset: 0x0

10.5.2.158 M3_C2_INTR_RAW

- Description: Channel3 ICU3's raw interrupt status register
- Offset: 0xE008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M3_C2_INTR_RAW	RO	M3_C2_INTR_RAW Value After Reset: 0x0

10.5.2.159 M3_C2_INTR_MASK

- Description: Channel3 ICU3 interrupt mask register
- Offset: 0xE00C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	M3_C2_INTR_MASK	RW	M3_C2_INTR_MASK Value After Reset: 0x0

10.5.2.160 M3_C2_GEN

- Description: Interrupt generation register of channel3 of ICU3
- Offset: 0xE010
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	M3_C2_GEN	RW	M3_C2_GEN Value After Reset: 0x0

10.5.2.161 M3_C2_INFO0

- Description: Information register 0 of channel 3 of ICU3
- Offset: 0xE014
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C2_INFO0	RW	M3_C2_INFO0 Value After Reset: 0x0

10.5.2.162 M3_C2_INFO1

- Description: Information register 1 of channel 3 of ICU3
- Offset: 0xE018

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C2_INFO1	RW	M3_C2_INFO1 Value After Reset: 0x0

10.5.2.163 M3_C2_INFO2

- Description: Information register 2 of channel 3 of ICU3
- Offset: 0xE01C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C2_INFO2	RW	M3_C2_INFO2 Value After Reset: 0x0

10.5.2.164 M3_C2_INFO3

- Description: Information register 3 of channel 3 of ICU3
- Offset: 0xE020
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C2_INFO3	RW	M3_C2_INFO3 Value After Reset: 0x0

10.5.2.165 M3_C2_INFO4

- Description: Information register 4 of channel 3 of ICU3
- Offset: 0xE024
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C2_INFO4	RW	M3_C2_INFO4 Value After Reset: 0x0

10.5.2.166 M3_C2_INFO5

- Description: Information register 5 of channel 3 of ICU3
- Offset: 0xE028
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C2_INFO5	RW	M3_C2_INFO5 Value After Reset: 0x0

10.5.2.167 M3_C2_INFO6

- Description: Information register 6 of channel 3 of ICU3
- Offset: 0xE02C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C2_INFO6	RW	M3_C2_INFO6 Value After Reset: 0x0

10.5.2.168 M3_C2_INFO7

- Description: Information register 7 of channel 3 of ICU3
- Offset: 0xE030
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	M3_C2_INFO7	RW	M3_C2_INFO7 Value After Reset: 0x0

10.5.2.169 M3_INTR_STA

- Description: Interrupt status register of ICU3
- Offset: 0xF000
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M3_INTR_STA	RO	M3_INTR_STA Value After Reset: 0x0

10.5.2.170 M3_INTR_CLR

- Description: Clear interrupt register of ICU3
- Offset: 0xF004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M3_INTR_CLR	WO	M3_INTR_CLR Value After Reset: 0x0

10.5.2.171 M3_INTR_RAW

- Description: ICU3's raw interrupt status register
- Offset: 0xF008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M3_INTR_RAW	RO	M3_INTR_RAW Value After Reset: 0x0

10.5.2.172 M3_INTR_MASK

- Description: ICU3 interrupt mask register
- Offset: 0xF00C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	M3_INTR_MASK	RW	M3_INTR_MASK Value After Reset: 0x0

10.5.2.173 IP_ID

- Description: IP_ID
- Offset: 0xFFFC
- Default Value: 0x80002

Bits	Field Name	Access	Description
[31:0]	IP_ID	RO	IP_ID Value After Reset: 0x80002

11 RTC

11.1 Overview

Real-Time Clock (RTC) module can realize real-time display time and timing alarm function.

11.2 Main Features

The RTC has the following features:

- 32bit RTC – Used with software for keeping track of time.
- Configurable option to include the prescalar counter.
- Long-term, exact chronometer – When clocked with a 1Hz clock, it can keep track of time from now up to 136 years in the future.
- Alarm function – Generates an interrupt after a programmed number of cycles.
- Long-time, base counter – Clocked with a very slow clock signal.

11.3 Interface

Figure & Table 11-1 Pin description table

Pin Name	Direction	Width	Description
RTC_CLK_IN	I	1	RTC dedicated clock signal
RTC_CLK_OUT	O	1	RTC dedicated clock signal

11.4 Function Description

The RTC has a programmable, 32bit, binary counter. The counter increments on successive positive edges of the input counter clock. When the Counter Load Register (RTC_CLR) is programmed, the counter is loaded with a start value that allows the counter to increment. When the counter reaches its maximum value (all bits are high), it wraps to 0 and then continues incrementing.
A match register, RTC_CMR, can be programmed and is compared to the internal counter. An interrupt is generated when the match register and the internal counter are equal.

11.5 Usage

The procedure of starting and using RTC is as follows:
1. Configure RTC initial value through the RTC_CLR register.
2. Configure the Counter Match register through the RTC_CMR register.
3. Configure RTC's control register RTC_CCR to begin counting.
4. Wait RTC's interrupt through reading the RTC_STAT register.
5. Clear RTC's interrupt by reading the RTC_EOI register.

11.6 Register Description

11.6.1 Register Memory Map

Register	Offset	Description	Section/Page
RTC_CCVR	0x0	Current Counter Value Register	10.6.2.1/704
RTC_CMR	0x4	Counter Match Register	10.6.2.2/704
RTC_CLR	0x8	Counter Load Register	10.6.2.3/705
RTC_CCR	0xc	Counter Control Register. Note: If the RTC_RSTAT register indicates that a pending interrupt exists...	10.6.2.4/705
RTC_STAT	0x10	Interrupt Status Register	10.6.2.5/706
RTC_RSTAT	0x14	Interrupt Raw Status Register	10.6.2.6/707
RTC_EOI	0x18	End of Interrupt Register	10.6.2.7/707
RTC_COMP_VERSION	0x1c	Component Version Register	10.6.2.8/707
RTC_CPSR	0x20	Counter PreScaler Register	10.6.2.9/708
RTC_CPCVR	0x24	Current Prescaler Counter Value Register	10.6.2.10/708

11.6.2 Register and Field Description

10.6.2.1 Current Counter Value Register

- Name: Current Counter Value Register
- Description: Current Counter Value Register
- Offset: 0x0

Bits	Field Name	Access	Description
31:0	Current_Counter_Value	R	When read, this register is the current value of the internal counter. This value is always read coherently. Value After Reset: 0x0

10.6.2.2 Counter Match Register

- Name: Counter Match Register
- Description: Counter Match Register
- Offset: 0x4

Bits	Field Name	Access	Description
31:0	Counter_Match	R/W	Interrupt Match Register. When the internal counter matches this register, an interrupt is generated, provided interrupt generation is enabled. When appropriate, this value is written coherently. Only when all the bytes are written is the register used by the interrupt detection logic. Value After Reset: 0x0

10.6.2.3 Counter Load Register

- Name: Counter Load Register
- Description: Counter Load Register
- Offset: 0x8

Bits	Field Name	Access	Description
31:0	Counter_Load	R/W	Loaded into the counter as the loaded value, which is written coherently. Value After Reset: 0x0

10.6.2.4 Counter Control Register

- Name: Counter Control Register
- Description: Counter Control Register
- Offset: 0xc

Bits	Field Name	Access	Description
31:8	RSVD_CCR	R	Reserved and read as 0. Value After Reset: 0x0
7:5	Reserved_5_7	RO	Reseved field
4	rtc_psclr_en	R/W	Allows the user to control the usage of RTC Prescaler feature. Values: 0x0 (DISABLED): Disable the Prescaler counter. 0x1 (ENABLED): Enable the Prescaler counter. Value After Reset: 0x0
3	rtc_wen	R/W	Allows the user to force the counter to wrap when a match occurs instead of waiting until the maximum count is reached. 0 = Wrap disabled, 1 = Wrap enabled, This bit is writable only when RTC_WRAP_MODE = 1.

Bits	Field Name	Access	Description
			Values: 0x0 (DISABLED): Disable the WRAP. 0x1 (ENABLED): Enable the WRAP. Value After Reset: 0x0
2	rtc_en	R/W	Allows the user to control counting in the counter. Internally, the counter is always enabled. Values: 0x0 (DISABLED): Disable the counter. 0x1 (ENABLED): Enable the counter. Value After Reset: 0x0
1	rtc_mask	R/W	Allows the user to mask interrupt generation. Values: 0x0 (UNMASKED): Interrupt unmasked. 0x1 (MASKED): Interrupt masked. Value After Reset: 0x0
0	rtc_ien	R/W	Allows the user to disable interrupt generation. Values: 0x0 (DISABLED): Disable the interrupt generation. 0x1 (ENABLED): Enable the interrupt generation. Value After Reset: 0x0

10.6.2.5 Interrupt Status Register

- Name: Interrupt Status Register
- Description: Interrupt Status Register
- Offset: 0x10

Bits	Field Name	Access	Description
31:1	RSVD_RTC_STAT	R	Reserved and read as 0. Value After Reset: 0x0 Exists: Always
0	rtc_stat	R	This register is the masked raw status. Values: 0x0 (INACTIVE): Interrupt is inactive. 0x1 (ACTIVE): Interrupt is active (regardless of polarity). Value After Reset: 0x0

10.6.2.6 Interrupt Raw Status Register

- Name: Interrupt Raw Status Register
- Description: Interrupt Raw Status Register
- Offset: 0x14

Bits	Field Name	Access	Description
31:1	RSVD_RTC_RSTAT	R	Reserved and read as 0. Value After Reset: 0x0
0	rtc_rstat	R	Raw Status Values: 0x0 (INACTIVE): Interrupt is inactive. 0x1 (ACTIVE): Interrupt is active (regardless of polarity). Value After Reset: 0x0

10.6.2.7 End of Interrupt Register

- Name: End of Interrupt Register
- Description: End of Interrupt Register
- Offset: 0x18

Bits	Field Name	Access	Description
31:1	RSVD_RTC_EOI	R	Reserved and read as 0. Value After Reset: 0x0
0	rtc_eoi	R	By reading this location, the match interrupt is cleared. Performing read-to-clear on interrupt, the interrupt is cleared at the end of the read. Value After Reset: 0x0

10.6.2.8 Component Version Register

- Name: Component Version Register
- Description: Component Version Register
- Offset: 0x1c

Bits	Field Name	Access	Description
31:0	rtc_comp_version	R	ASCII value for each number in the version, followed by *. For example, 32_30_31_2A represents the version 2.01*. Value After Reset: RTC_VERSION_ID

10.6.2.9 Counter PreScaler Register

- Name: Counter PreScaler Register
- Description: Counter PreScaler Register
- Offset: 0x20

Bits	Field Name	Access	Description
31:0	Counter_Prescaler_Value	R/W	Counter Prescaler Register. The RTC counter will be updating at the rate of rtc_clk, rtc_clk_en, or pclk based on the configuration. This register is used to prescale the rate at which the RTC counter updates. When appropriate, this register is written coherently. Only when all the bytes are written, the register used by the prescaler counter logic. Value After Reset: RTC_PRESCLR_VAL Exists: Always

10.6.2.10 Current Prescaler Counter Value Register

- Name: Current Prescaler Counter Value Register
- Description: Current Prescaler Counter Value Register
- Offset: 0x24

Bits	Field Name	Access	Description
31:0	Current_Prescaler_Counter_Value	R	When read, this register provides the current value of the internal prescaler counter. This value is always read coherently. Value After Reset: 0x0

12 WDT

12.1 Overview

The WDT can be used to prevent system lock-up that may be caused by conflicting parts or programs of RTOS. It ensures proper operation by requiring periodic attention to prevent a reset on time-out. The generated interrupt is passed to an interrupt controller. The generated reset is passed to a reset component, which generates a real system reset for all the components in the system, including WDT itself.

12.2 Main Features

The WDT supports the following features:

- Configurable watchdog counter width of 32 bits
- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
- Optional external clock enable signal to control the rate at which the counter counts
- If a timeout occurs, the WDT can perform one of the following operations:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset

12.3 Function Description

12.3.1 Block Diagram

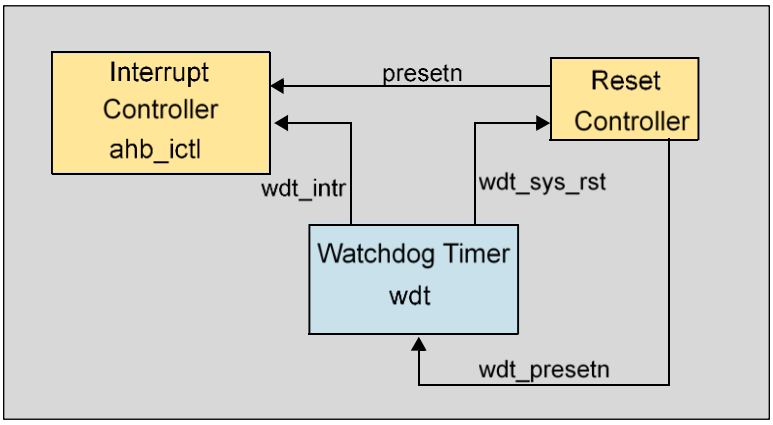


Figure & Table 12-1 WDT function block diagram

The generated interrupt is passed to an interrupt controller. The generated reset is passed to a reset controller, which in turn generates a reset for the components in the system. The WDT may be reset independently of the other components.

12.4 Usage

1. Select required timeout period.
2. Set reset pulse length, response mode, and enable WDT.
3. Write 0x76 to WDT_CRR.
4. Starts back to selected timeout period.
5. Can clear by reading WDT_EOI or restarting (kicking) the counter by writing 0x76 to WDT_CRR.

12.5 Register Description

12.5.1 Register Memory Map

Figure & Table 12-2 Memory map of WDT

Register	Offset	Description	Section/Page
WDT_CR	0x0	Control register	12.5.2.1/710
WDT_TORR	0x4	Timerout range register Reset value: 0x0	12.5.2.2/711
WDT_CCVR	0x8	Current counter value register Reset value: 32'hffff	12.5.2.3/713
WDT_CRR	0xc	Counter restart register Reset value: 0x0	12.5.2.4/713
WDT_STAT	0x10	Interrupt status register Reset value: 0x0	12.5.2.5/713
WDT_EOI	0x14	Interrupt clear register Reset value: 0x0	12.5.2.6/714
WDT_COMP_VERSION	0xf8	Component version register	12.5.2.7/714
WDT_COMP_TYPE	0xfc	Component type register	12.5.2.8/714

12.5.2 Register and Field Description

12.5.2.1 WDT_CR

- Name: Control Register
- Address Offset: 0x00

Bits	Field Name	Access	Description
31:5	Reserved and read as zero (0).		

Bits	Field Name	Access	Description
4:2	RPL	R/W	Reset pulse length This is used to select the number of pclk cycles for which the system reset stays asserted. The range of values available is 2 to 256 pclk cycles. 000: 2 pclk cycles 001: 4 pclk cycles 010: 8 pclk cycles 011: 16 pclk cycles 100: 32 pclk cycles 101: 64 pclk cycles 110: 128 pclk cycles 111: 256 pclk cycles Reset Value: 0
1	RMOD	R/W	Response mode Selects the output response generated to a timeout. 0: Generate a system reset; 1: First generate an interrupt and if it is not cleared by the time a second timeout occurs then generate a system reset. Reset Value: 1
0	WDT_EN	R/W	WDT enable This bit is used to enable and disable the DW_apb_wdt. When disabled, the counter does not decrement. Thus, no interrupts or system resets are generated. Once this bit has been enabled, it can be cleared only by a system reset. 0: WDT disabled. 1: WDT enabled. Reset Value: 0

12.5.2.2 WDT_TORR

- Name: Timeout Range Register
- Address Offset: 0x04

Bits	Field Name	Access	Description
31:8	Reserved and read as zero (0).		
7:4	TOP_INIT	R/W	Timeout period for initialization

Bits	Field Name	Access	Description
			Used to select the timeout period that the watchdog counter restarts from for the first counter restart (kick). This register should be written after reset and before the WDT is enabled. A change of the TOP_INIT is seen only once the WDT has been enabled, and any change after the first kick is not seen as subsequent kicks use the period specified by the TOP bits. The range of values is limited by the WDT_CNT_WIDTH(32). If TOP_INIT is programmed to select a range that is greater than the counter width, the timeout period is truncated to fit to the counter width. This affects only the non-user specified values as users are limited to these boundaries during configuration. The range of values available for a 32-bit watchdog counter are: Where i = TOP_INIT and t = timeout period For i = 0 to 15 if 0==1 t = 2(16 + i) else t = WDT_USER_TOP_INIT_(i) Reset Value: 0
3:0	TOP	R/W	Timeout period This field is used to select the timeout period from which the watchdog counter restarts. A change of the timeout period takes effect only after the next counter restart (kick). The range of values is limited by the WDT_CNT_WIDTH(32). If TOP is programmed to select a range that is greater than the counter width, the timeout period is truncated to fit to the counter width. This affects only the non-user specified values as users are limited to these boundaries during configuration. The range of values available for a 32-bit watchdog counter are: Where i = TOP and t = timeout period For i = 0 to 15

Bits	Field Name	Access	Description
			if 0==1 t = 2(16 + i) else t = WDT_USER_TOP_(i) Reset Value: 0

12.5.2.3 WDT_CCVR

- Name: Current Counter Value Register
- Address Offset: 0x08

Bits	Field Name	Access	Description
31:0	Current counter value register	R	This register, when read, is the current value of the internal counter. This value is read coherently when ever it is read, which is relevant when the APB_DATA_WIDTH(32) is less than the counter width. Reset Value: 0

12.5.2.4 WDT_CRR

- Name: Current Restart Register
- Address Offset: 0x0c

Bits	Field Name	Access	Description
31:8	Reserved and read as zero (0).		
7:0	Counter Restart Register	W	This register is used to restart the WDT counter. As a safety feature to prevent accidental restarts, the value 0x76 must be written. A restart also clears the WDT interrupt. Reading this register returns zero. Reset Value: 0

12.5.2.5 WDT_STAT

- Name: Interrupt Status Register
- Address Offset: 0x10

Bits	Field Name	Access	Description
31:1	Reserved and read as zero (0).		
0	Interrupt Status Register	R	This register shows the interrupt status of the WDT. 1: Interrupt is active regardless of polarity.

Bits	Field Name	Access	Description
			0: Interrupt is inactive. Reset Value: 0

12.5.2.6 WDT_EOI

- Name: Interrupt Clear Register
- Address Offset: 0x14

Bits	Field Name	Access	Description
31:1	Reserved and read as zero (0).		
0	Interrupt Clear Register	R	Clears the watchdog interrupt. This can be used to clear the interrupt without restarting the watchdog counter. Reset Value: 0

12.5.2.7 WDT_COMP_VERSION

- Name: Component Version Register
- Address Offset: 0xf8

Bits	Field Name	Access	Description
31:0	WDT Component Version	R	ASCII value for each number in the version, followed by *. For example, 32_30_31_2A represents the version 2.01*.

12.5.2.8 WDT_COMP_TYPE

- Name: Component Type Register
- Address Offset: 0xfc

Bits	Field Name	Access	Description
31:0	Component Type Register	R	Designware Component Type number = 0x44_57_01_20. This assigned unique hex value is constant, and is derived from the two ASCII letters "DW" followed by a 16-bit unsigned number.

13 Timer

13.1 Overview

Timers count down from a programmed value and generate an interrupt when the count reaches zero. The initial value for each timer (the value it counts down from) is loaded into the counter by writing the desired value into the timer Local Count Register.

13.2 Main Features

Timer has the following features:

- Up to four timer units
- The four counters can be cascaded in pairs by configuring related sysreg registers
- Each timer configurable timer width: 32 bits
- Configurable counter cascade, the maximum counting bit width is up to 128 bits
- Support for two operation modes: free-running and user-defined count

13.3 Function Description

Timers count down from a programmed value and generate an interrupt when the count reaches zero. The initial value for each timer (the value it counts down from) is loaded into the counter by writing the desired value into the timer Local Count Register.
The four counters can be cascaded in pairs by configuring related sysreg registers.

13.4 Usage

13.4.1 Base Usage

The procedure is illustrated below:

1. Initialize the timer through the TimerNControlReg register (where N is in the range 1 to 4).
   a) Disable the timer by writing a “0” to the timer enable bit (bit0); accordingly, the timer_en output signal is de-asserted.
   b) Program the timer mode–user-defined or free-running–by writing a “0” or “1,” respectively, to the timer mode bit (bit1).
   c) Set the interrupt mask as either masked or not masked by writing a “0” or “1,” respectively, to the timer interrupt mask bit (bit2).
2. Load the timer counter value into the TimerNLoadCount register (where N is in the range 1 to 4).
3. Enable the timer by writing a “1” to bit0 of TimerNControlReg.

13.4.2 Timer Cascade Function

Users can configure the subsystem sysreg registers field timer_1_2_link, timer_2_3_link and timer_3_4_link to control the cascade connection between timer1 and timer2, timer2 and timer3, and timer3 and timer4 respectively.

13.5 Register Description

13.5.1 Register Memory Map

Register	Offset	Description	Section/Page
TIMERNLOADCOUNT (for N = 1, N <= 4)	0x00 + N*0x14	Value to be loaded into Timer N	13.5.2.1/717
TIMERNCURRENTVALUE	0x04 + N*0x14	Current value of Timer N	13.5.2.2/717
TIMERNCONTROLREG	0x08 + N*0x14	Control register for Timer N. This register controls enabling, operating mode (free-running or defined-count).	13.5.2.3/717
TIMERNEOI (for N = 1, N <= 4)	0x0c + N*0x14	Clears the interrupt from Timer N	13.5.2.4/718
TIMERNINTSTATUS (for N = 1, N <= 4)	0x10 + N*0x14	Contains the interrupt status for Timer N	13.5.2.5/719
TIMERSINTSTATUS	0xa0	Contains the interrupt status of all timers in the component.	13.5.2.6/719
TIMERSEOI	0xa4	Returns all zeroes (0) and clears all active interrupts.	13.5.2.7/720
TIMERSRAWINTSTATUS	0xa8	Contains the unmasked interrupt status of all timers in the component.	13.5.2.8/720
TIMERS_COMP_VERSION	0xac	Current revision number of the timer's component.	13.5.2.9/720
TIMERSNLOADCONUT2	0xb0 + N*0x04	Value to be loaded into Timer N when toggle output changes from 0 to 1.	13.5.2.10/721
TIMERS_N_PROT_LEVEL (for N = 1, N <= 4)	0xd0 + N*0x04	Timer N protection level register Read/Write access: R/W	13.5.2.11/721

13.5.2 Register and Field Description

13.5.2.1 TIMERNLOADCOUNT

- Name: Timer N Load Count Register
- Address Offset: 0x00 + N*0x14 (for N = 1, N <= 4)

Bits	Field Name	Access	Description
31:0	TimerNLoadCount	R/W	Value to be loaded into Timer N. This is the value from which counting commences. Any value written to this register is loaded into the associated timer. Value After Reset: 0x0 Exists: Always

13.5.2.2 TIMERNCURRENTVALUE

- Name: Current Value of Timer N
- Address Offset: 0x04 + N*0x14 (for N = 1, N <= 4)

Bits	Field Name	Access	Description
31:0	TimerNCurrentValue	R	Current Value of Timer N. When TIM_NEWMODE = 0, This register is supported only when timer_N_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value. When TIM_NEWMODE = 1, no restrictions apply. Value After Reset: 32'h80000000 Exists: Always Volatile: True

13.5.2.3 TIMERNCONTROLREG

- Name: Timer N Control Register
- Address Offset: 0x08 + N*0x14 (for N = 1, N <= 4)

Bits	Field Name	Access	Description
31:5	RSVD_TimerNControlReg	R	Reserved field Value After Reset: 0x0
4	TIMER_0N100PWM_EN	R	Optional. Allows the user to enable or disable the usage of Timer 0% and 100% mode feature. Reserved. Values: 0x1 (ENABLED): Timer 0% and 100% PWM duty cycle mode is enabled.

Bits	Field Name	Access	Description
			0x0 (DISABLE): Timer 0% and 100% PWM duty cycle mode is disabled. Value After Reset: 0x0
3	TIMER_PWM	R/W	Pulse Width Modulation of timer_N_toggle output. This field is only present when TIM_NEWMODE is enabled. Values: 0x1 (ENABLED): PWM for timer_N_toggle o/p is enabled. 0x0 (DISABLE): PWM for timer_N_toggle o/p is disabled. Value After Reset: 0x0
2	TIMER_INTERRUPT_MASK	R/W	Timer interrupt mask for Timer N Values: 0x1 (MASKED): Timer N interrupt is masked. 0x0 (UNMASKED): Timer N interrupt is unmasked. Value After Reset: 0x0
1	TIMER_MODE	R/W	Timer mode for Timer N NOTE: You must set the Timer1LoadCount registers to all 1s before enabling the timer in free-running mode. Values: 0x1 (USER_DEFINED): User-defined mode of operation 0x0 (FREE_RUNNING): Free running mode of operation Value After Reset: 0x0
0	TIMER_ENABLE	R/W	Timer enable bit for Timer N Values: 0x1 (ENABLED): Timer N is enabled. 0x0 (DISABLE): Timer N is disabled. Value After Reset: 0x0

13.5.2.4 TIMERNEOI

- Name: Timer N End-of-Interrupt Register
- Address Offset: 0x0c + N*0x14 (for N = 1, N <= 4)

Bits	Field Name	Access	Description
31:1	RSVD_TimerNEOI	R	Reserved field Value After Reset: 0x0

Bits	Field Name	Access	Description
0	TimerNEOI	R	Reading from this register returns all zeros (0) and clears the interrupt from Timer N. Value After Reset: 0x0

13.5.2.5 TIMERNINTSTATUS

- Name: Timer N Interrupt Status Register
- Address Offset: 0x10 + N*0x14 (for N = 1, N <= 4)

Bits	Field Name	Access	Description
31:1	RSVD_TimerNIntStatus	R	Reserved field Value After Reset: 0x0
0	TimerNIntStatus	R	Contains the interrupt status for Timer N. Values: 0x1 (ACTIVE): Timer N interrupt is active. 0x0 (INACTIVE): Timer N interrupt is inactive. Value After Reset: 0x0

13.5.2.6 TIMERSINTSTATUS

- Name: Timer Interrupt Status Register
- Address Offset: 0xa0

Bits	Field Name	Access	Description
31:4	RSVD_TimerIntStatus	R	Reserved field Value After Reset: 0x0
3:0	TimerIntStatus	R	Contains the interrupt status of all timers in the component. If a bit of this register is 0, then the corresponding timer interrupt is not active and the corresponding interrupt could be on either the timer_intr bus or the timer_intr_n bus, depending on the interrupt polarity you have chosen. Similarly, if a bit of this register is 1, then the corresponding interrupt bit has been set in the relevant interrupt bus. In both cases, the status reported is the status after the interrupt mask has been applied. Reading from this register does not clear any active interrupts. Values: 0x1 (ACTIVE): Timer_intr(_n) is active. 0x0 (INACTIVE): Timer_intr(_n) is inactive.

Bits	Field Name	Access	Description
			Value After Reset: 0x0

13.5.2.7 TIMERSEOI

- Name: Timer End-of-Interrupt Register
- Address Offset: 0xa4

Bits	Field Name	Access	Description
31:4	RSVD_TIMERSEOI	R	Reserved field Value After Reset: 0x0 Exists: Always
3:0	TIMERSEOI	R	Reading this register returns all zeroes (0) and clears all active interrupts. Value After Reset: 0x0

13.5.2.8 TIMERSRAWINTSTATUS

- Name: Timer Raw Interrupt Status Register
- Address Offset: 0xa8

Bits	Field Name	Access	Description
31:4	RSVD_TIMERSRAWINTSTAT	R	Reserved field Value After Reset: 0x0
3:0	TIMERSRAWINTSTAT	R	The register contains the unmasked interrupt status of all timers in the component. Values: 0x1 (ACTIVE): Raw Timer_intr(_n) is active. 0x0 (INACTIVE): Raw Timer_intr(_n) is inactive. Value After Reset: 0x0

13.5.2.9 TIMERS_COMP_VERSION

- Name: Timer Component Version
- Address Offset: 0xac

Bits	Field Name	Access	Description
31:0	TIMERSCOMPVERSION	R	Current revision number of the timer's component Value After Reset: 0x0 Value After Reset: 3231322a

13.5.2.10 TIMERSNLOADCOUNT2

- Name: Timer N Load Count2 Register
- Address Offset: 0xb0 + N*0x04 (for N = 1, N <= 4)

Bits	Field Name	Access	Description
31:0	TIMERNLOADCOUNT2	R/W	Value to be loaded into Timer N when timer_N_toggle output changes from 0 to 1. This value determines the width of the HIGH period of the timer_N_toggle output. Value After Reset: 0x0

13.5.2.11 TIMERS_N_PROT_LEVEL

- Name: Timer_N_Protection level
- Address Offset: 0xd0 + N*0x04 (for N = 1, N <= 4)

Bits	Field Name	Access	Description
31:3	RsvdTimer_N_ProtLevel	R	Reserved field-read-only Value After Reset: 0x0 Exists: Always
2:0	Timer_N_ProtLevelField	R/W	This field holds protection value of TIMER_N_PROT_LEVEL register. Value After Reset: 3'h2 Exists: Always

14 DMAC

14.1 Overview

In Direct Memory Access (DMA) mode, I/O exchange is completely performed by hardware. In this mode, the Direct Memory Access Controller (DMAC) directly transmits data between a memory and a peripheral, or between peripherals, or between memories, avoiding interference with the CPU and reducing interrupt processing overhead of the CPU. A DMA is generally used to transmit a group of data at a high speed. After receiving a DMA transmission request, the DMAC starts the main bus controller based on the channel configuration of the CPU, then sends address and control signals to the memory or peripheral, and counts the amount of transmitted data, and reports an end or error of transmission to the CPU through an interrupt.

14.2 Main Features

The DW_axi_dmac supports the following features:

- Independent core, slave interface and master interface clocks
- Up to 4 channels, one per source and destination pair
- Data transfers in one direction only (each channel is unidirectional)
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral DMA transfers
- AMBA 4 AXI-compliant master interface
- AHB slave interface for programming the DMA controller
- Multiple levels of DMA transfer hierarchy
  - DMA transfer split into transaction, block, and complete DMA transfer levels
- Support for AXI unaligned transfers
- Single FIFO per channel
- Automatic packing/unpacking of data to fit FIFO width
- Single or multiple DMA transactions
- Programmable multiple transaction size for each channel
- Channel disabling without data loss
- Channel suspend and resume
- Programmable channel priority
- Programmable multiblock transfer using linked list, contiguous address, auto reload, and shadow register methods
- Dynamic extension of linked list
- Independent configuration of SRC/DST multiblock transfer type
- Multiple state machines, one for each channel SRC and DST
- Separate state machines for data and LLI access
- Programmable transfer length (block length)

- Error status register to ease debugging during error events
- Programmable flow control at DMA transfer level
  - If the size of the block transfer is known prior to DMA initialization, the DMA controller is a flow controller at the DMA block transfer level.
  - If the size of the DMA block transfer is unknown prior to the DMA initialization Peripheral, either source or destination is the flow controller for undefined length (demand mode) DMA block transfers.
- Programmable software and hardware handshaking interfaces for non-memory peripherals
- Up to 64 hardware handshaking interfaces (only in REE)
- Enabling/disabling of individual handshake interfaces
- Combined interrupt outputs
- Interrupt generation on:
  - DMA transfer completion
  - Block transfer completion
  - Single or multiple transaction completion
  - Error condition
  - Channel suspend or disable
- Interrupt enabling and masking
- Outstanding transactions on master interface
- Setting outstanding transaction limit per channel on the master interface
- Out-of-order transaction support for different channels connected on same master interface. Transactions of a particular channel are always initiated in order.
- Increment and fixed address transfers on master interface
- Source and destination data transfer addresses must be aligned to respective transfer widths
- Transfer size (width) used for slave interface; must be same as data bus width

14.3 Function Description

14.3.1 Data Flow

Figure & Table 14-1 shows the flow of data in the DW_axi_dmac in a scenario when the source and destination peripherals are on the same AXI layer. In this scenario, the source peripheral uses a hardware handshaking interface and the destination peripheral uses a software handshaking interface. If these peripherals are memory, handshaking interfaces are not used.

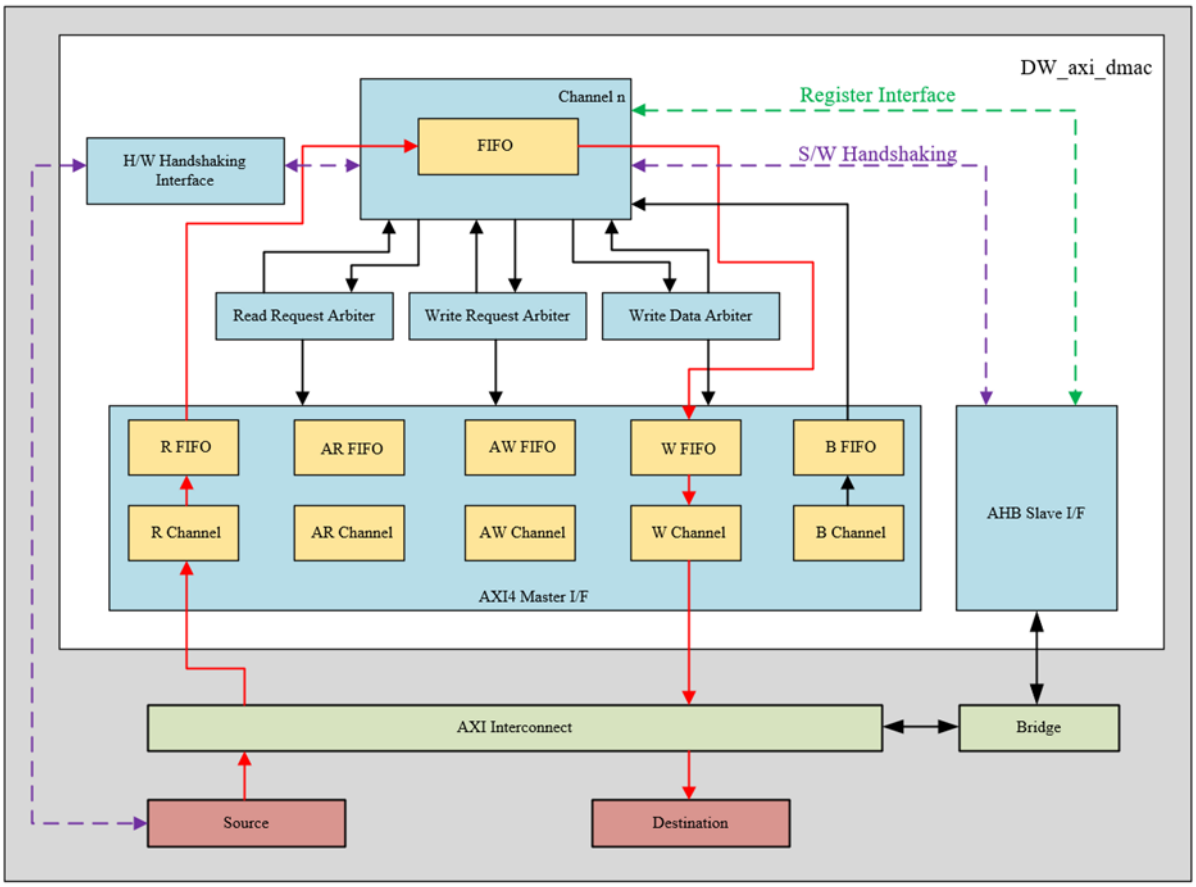


Figure & Table 14-1 DW_axi_dmac flow diagram when source and destination peripherals on same AXI layer

14.3.2 Clock and Reset

There are 2 clocks in DW_axi_dmac:

- aclk: DW_axi_dmac core clock and AXI4 master interface clock
- hclk: AHB slave interface clock

There are 2 resets in DW_axi_dmac:

- aresetn: DW_axi_dmac core reset and AXI4 master interface reset. Active low.
- hresetn: AHB slave interface reset. Active low.

DW_axi_dmac supports a soft reset, which is set using the DMAC_RST field in the DMAC_ResetReg register. The soft reset procedure is as follows:

1. Software writes 1 to the DMAC_ResetReg. DMAC_RST bit to reset the DW_axi_dmac. Software polls the DMAC_ResetReg. DMAC_RST bit until it is seen as 0, which confirms the reset.
2. DW_axi_dmac resets all the modules in different clock domains except for the slave bus interface module. The slave bus interface module is not reset because software is polling the DMAC_ResetReg. DMAC_RST field.
3. DW_axi_dmac clears the DMAC_ResetReg.DMAC_RST bit to 0.

14.3.3 Slave Bus Interface

The slave bus interface module implements the logic to access the internal registers of DW_axi_dmac by an external AHB master. This module supports only the little-endian scheme for data transfer. The slave bus interface module supports a 32-bit data bus width.

14.3.4 Master Interface

The master interface implements all five channels specified in the AXI protocol:

- Write address
- Write data
- Write response
- Read address
- Read data

The master interface implements different FIFOs for temporary storage of data transferred between external memories or peripherals through different channels in DW_axi_dmac core. DW_axi_dmac supports 4 channels, which can be assigned to either of the master interfaces, based on a well-defined, programmable arbitration scheme for accessing the master interface.

14.3.5 Arbitration Scheme

DW_axi_dmac implements a dynamic priority and fair-among-equals arbitration scheme, with options for channel locking at different DMA transfer hierarchy levels. The number of priority levels available is the same as the number of enabled channels and the priority value is programmable for each channel in the channel configuration register, CHx_CFG. Multiple channels can be given the same priority level, however, some priority levels remain unused. A priority of 3 is the highest priority, and 0 is the lowest.

Dynamic priority and fair-among-equals arbitration is a two-tier arbitration scheme which works as follows:

- The first-tier arbitration uses the priority inputs of the requests and decides which one of the requesting clients is issued the grant signal. The request with the highest priority is granted access to the AXI channel on the master interface.
- If two or more requests to the arbiter have the same programmed priority value, the second-tier arbitration, based on the fair-among-equals scheme, is used. In this scheme, the grant is issued fairly among actively requesting clients with the same priority level.

14.3.6 Interrupt

DW_axi_dmac supports combined interrupt outputs.

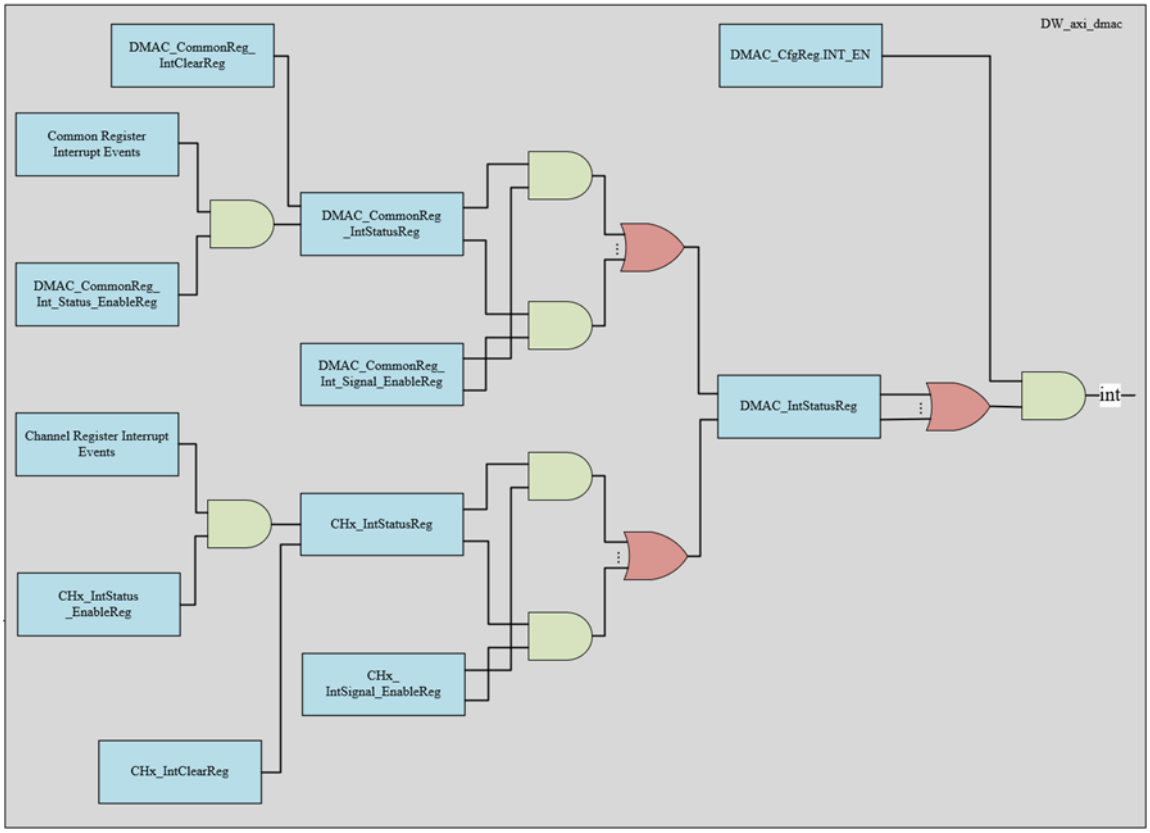


Figure & Table 14-2 DW_axi_dmac interrupt generation

14.3.7 Single Transaction Region

In certain cases, a DMA block transfer cannot complete using only burst transactions. Typically this occurs when the block size is not a multiple of the burst transaction length. In these cases, the block transfer uses burst transactions up to the point where the amount of data left to complete the block is less than the amount of data in a burst transaction. At this point, the DW_axi_dmac samples the dma_single status flag and completes the block transfer using single transactions. The peripheral asserts a single status flag to indicate to the DW_axi_dmac that there is enough data or space to complete a single transaction from or to the source or destination peripheral.

For hardware handshaking, the single status flag is a signal on the hardware handshaking interface. For software handshaking, the single status flag is one bit in the software handshaking interface register.

14.3.8 Handshaking Interface

Handshaking interfaces are used at the transaction level to control the flow of single or burst transactions. The operation of the handshaking interface depends on whether the peripheral or the DW_axi_dmac is the flow controller. The peripheral uses the handshaking interface to indicate to the DW_axi_dmac that it is ready to transfer or accept data over the AXI bus.

DW_axi_dmac supports a maximum of 64 hardware handshaking interfaces. The type of handshaking interface used (software or hardware) is independently programmable for each

channel source and destination in the channel configuration register, CHx_CFG. Software handshaking is accomplished through memory-mapped registers, while hardware handshaking is accomplished using a dedicated handshaking interface.

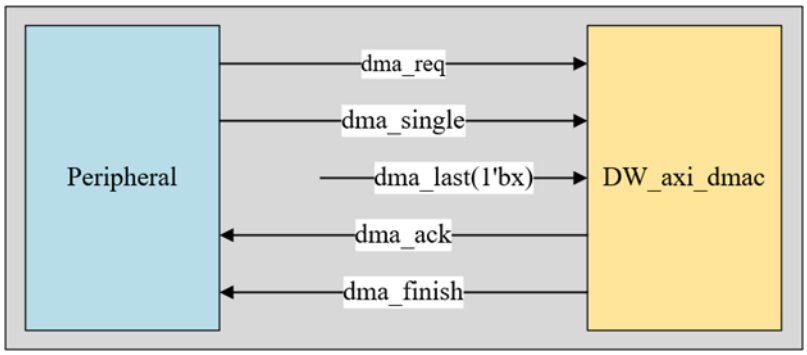


Figure & Table 14-3 Hardware handshaking interface (peripheral not flow controller)

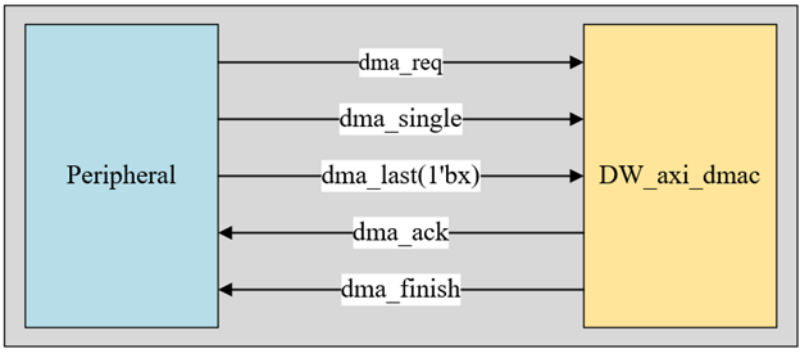


Figure & Table 14-4 Hardware handshaking interface (peripheral is flow controller)

14.3.9 Early Terminated Burst Transaction

When a source or destination peripheral is in the single transaction region, a burst transaction can still be requested. However, in this case, src_burst_size_bytes or dst_burst_size_bytes is greater than the number of bytes left to complete the source or destination block transfer at the time the burst transaction is triggered. In this case, the burst transaction is started and 'early-terminated' at block completion without transferring the programmed amount of data. Only the amount of data required to complete the block transfer is transferred.

14.3.10 Transfer Control

Transfer control logic facilitates the data transfer from a source peripheral of the channel to the destination peripheral. It interacts with multiple other modules, such as the channel source and destination state machine, linked list control logic, channel registers, channel FIFO control logic and so on. Data from the source peripheral is temporarily stored in the channel FIFO before being sent to the destination peripheral. DW_axi_dmac implements the logic needed to pack and unpack data to fit the FIFO configuration, if source and destination peripherals use different transfer size (arsize, awsize) for data transfer.

If a DMA transfer consists of a single block, the software sets the multi-block type bits of both source and destination peripherals in the CHx_CFG register to 2'b00. In this case, the DW_axi_dmac disables the channel once the block transfer corresponding to the block length programmed in CHx_BLOCK_TS register is completed. The CHx_IntStatusReg register is updated with the status corresponding to the completed block transfer. The CHx_IntStatusReg register is updated based on the settings of the CHx_IntMaskReg register and interrupts are generated based on the settings of the CHx_IntMaskReg, DMAC_IntMaskReg, and DMAC_CfgReg registers.

If DW_axi_dmac is programmed for multiblock transfers, the CHx_SAR and CHx_DAR registers are reprogrammed using either of the following methods on successive blocks of a multiblock transfer:

- Contiguous Address
- Auto Reloading
- Shadow Register
- Linked List

The CHx_CTL and CHx_BLOCK_TS registers are reprogrammed using either of the following methods on successive blocks of a multiblock transfer:

- Auto Reloading
- Shadow Register
- Linked List

Contiguous Address: In this case, the address between successive blocks is selected as a continuation from the end of the previous block. Enabling the source or destination address to be contiguous between blocks is a function of CHx_CTL.SRC_MLTBLK_TYPE and CHx_CTL.DST_MLTBLK_TYPE register fields. CHx_SAR and CHx_DAR updates cannot be selected to be contiguous at the same time. If required, this functionality can be achieved indirectly, by using linked lists. To do this, set up the LLI.CHx_SAR address of the next block descriptor to be one greater than the end address of the previous block. Similarly, set up the LLI.CHx_DAR address of the next block descriptor to be one greater than the end address of the previous block.

Auto Reloading: In this case, the channel transfer control registers are reloaded with their initial values at the completion of each block and these values are used for the new block. Some or all of the CHx_SAR, CHx_DAR, CHx_BLOCK_TS, and CHx_CTL channel registers are reloaded from their initial value at the start of a new block transfer, depending on the multi-block transfer type selected for source and destination peripherals. The DW_axi_dmac does not proceed to the next block transfer until software clears the corresponding channel's block transfer complete interrupt by writing 1 to the corresponding bit in the DMAC_IntClear_Reg register if this interrupt is not masked off.

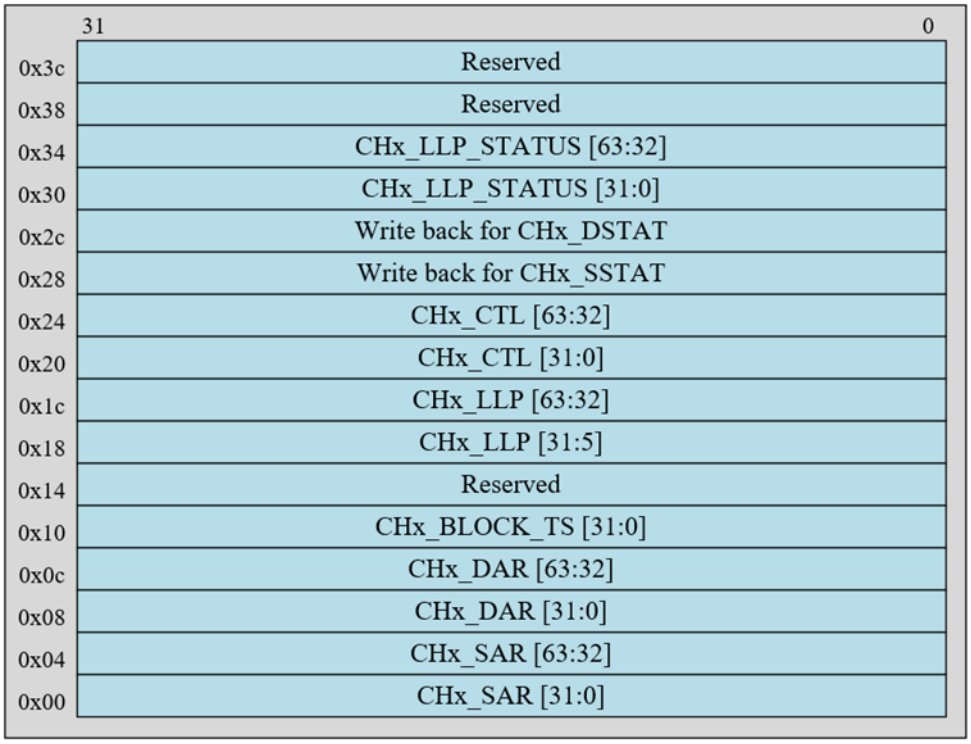
Shadow Register: In this case, the channel transfer control registers are loaded from their corresponding shadow registers at the completion of each block and these values are used for the new block. Some or all of the CHx_SAR, CHx_DAR, CHx_BLOCK_TS, and CHx_CTL channel registers are loaded from their corresponding shadow registers at the start of a new block transfer, depending on the multiblock transfer type selected for source and destination peripherals. A separate memory map is not defined for the shadow register access. Software always writes to the CHx_SAR, CHx_DAR, CHx_BLOCK_TS, and CHx_CTL registers irrespective of the type of multiblock

transfer used. If a shadow-register-based multiblock transfer is used for a source or destination transfer, DW_axi_dmac internally routes the data to the corresponding shadow registers. DW_axi_dmac copies the shadow register contents to CHx_SAR, CHx_DAR, CHx_BLOCK_TS, and CHx_CTL registers before starting a new block transfer. Read operations to the CHx_SAR, CHx_DAR, CHx_BLOCK_TS, and CHx_CTL registers always return the data corresponding to the current block transfer and not the shadow register contents (which corresponds to the next block). For shadow-register-based multiblock transfer, the ShadowReg_Or_LLI_Valid bit in the CHx_CTL register indicates whether the shadow register contents are valid or not. Zero indicates that the shadow register contents are invalid, while 1 indicates that the shadow register contents are valid. If this bit is read as zero during a shadow register fetch phase, DW_axi_dmac discards the shadow register contents and generates a ShadowReg_Or_LLI_Invalid_ERR interrupt. DW_axi_dmac waits until the software writes any value to the CHx_BLK_TFR_ResumeReqReg register to indicate valid shadow register availability, before attempting another shadow register fetch operation to continue the next block transfer.

Linked List: In this case, the DW_axi_dmac reprograms the channel transfer control registers prior to the start of each block, by fetching the block descriptor for that block from system memory. This is known as an LLI update. DW_axi_dmac block chaining uses a linked list pointer register (CHx_LLP) to store the address in memory of the next linked list item. Each LLI contains the following block descriptors:

- CHx_SAR
- CHx_DAR
- CHx_BLOCK_TS
- CHx_CTL
- CHx_LLP

To set up block chaining, a sequence of linked lists should be programmed in memory. DW_axi_dmac allows dynamic extension of linked lists, which eliminates the need for creating the entire linked list in the system memory in advance. The CHx_CTL.ShadowReg_Or_LLI_Valid and CHx_CTL.LLI_Last fields of the LLI are used to achieve this functionality. For linked-list-based multi-block transfers, the ShadowReg_Or_LLI_Valid bit of the LLI.CHx_CTL register indicates whether the linked list item fetched from the memory is valid or not. If this bit is set to 0, it indicates the LLI is invalid, while 1 indicates the LLI is valid. If the LLI is invalid, DW_axi_dmac discards the LLI and generates an LLI Error interrupt (if the corresponding channel error interrupt mask bit is set to 0). This error condition causes the DW_axi_dmac to halt the corresponding channel gracefully. DW_axi_dmac waits till software writes any value to the CHx_BLK_TFR_ResumeReqReg register to indicate the availability of a valid LLI, before attempting another LLI read operation. LLI access always uses a burst size (arsize or awsize) that is the same as the data bus width and cannot be changed or programmed to anything other than this. Burst length (awlen or arlen) is chosen based on the data bus width so that the access does not cross one complete LLI structure of 64 bytes. DW_axi_dmac fetches the entire LLI (40 bytes) in one AXI burst, if the burst length is not limited by other settings.



	31 ... 0
0x3c	Reserved
0x38	Reserved
0x34	CHx_LLP_STATUS [63:32]
0x30	CHx_LLP_STATUS [31:0]
0x2c	Write back for CHx_DSTAT
0x28	Write back for CHx_SSTAT
0x24	CHx_CTL [63:32]
0x20	CHx_CTL [31:0]
0x1c	CHx_LLP [63:32]
0x18	CHx_LLP [31:5]
0x14	Reserved
0x10	CHx_BLOCK_TS [31:0]
0x0c	CHx_DAR [63:32]
0x08	CHx_DAR [31:0]
0x04	CHx_SAR [63:32]
0x00	CHx_SAR [31:0]

Figure & Table 14-5 DW_axi_dmac linked list item (descriptor)

14.3.11 AXI Unaligned Transfer Support

The DW_axi_dmac supports the generation of unaligned DMA transfers on the AXI master interfaces.

14.3.12 Channel Suspend and Disable

Under normal operation, software enables a channel by writing a 1 to the channel enable register, DMAC_ChEnReg.CH_EN, and hardware disables a channel on transfer completion by clearing the DMAC_ChEnReg.CH_EN register. Software can suspend and disable a channel before a transfer completes. The suspend and disable procedures are explained in the following sections.

14.4 Usage

14.4.1 Programming Flow for Shadow-Register-Based Multi-Block Transfer

1. Software reads the DMAC channel enable register (DMAC_ChEnReg) to select an available (unused) channel.
2. Software programs the CHx_CFG register with appropriate values for the DMA transfer. The SRC_MLTBLK_TYPE and/or DST_MLTBLK_TYPE bits must be set to 2'b10.
3. Software programs the CHx_SAR and/or CHx_DAR, CHx_BLOCK_TS, and CHx_CTL registers with appropriate values for the first block. DW_axi_dmac loads the corresponding shadow registers with these values. The CHx_CTL register must be the last register to be programmed with the

ShadowReg_Or_LLI_Valid bit set to 1 to indicate that the shadow register contents are valid. If the slave interface data bus width or transfer size is less than 64 bits, CHx_CTL[63:56] must be updated last.

4. Software enables the channel by writing 1 to the appropriate bit location in the DMAC_ChEnReg register.
5. DW_axi_dmac initiates the DMA block transfer operation based on the settings for the block transfer.
   a) The block transfer might start immediately or after the hardware or software handshaking request, depending on the value of the TT_FC field in the CHx_CFG register.
   b) DW_axi_dmac checks CHx_CTL_ShadowReg.ShadowReg_Or_LLI_Valid bit and if it is seen as '0', DW_axi_dmac waits till software writes (any value) to CHx_BLK_TFR_ResumeReqReg to indicate valid LLI availability, before attempting another Shadow Register fetch operation. DW_axi_dmac might generate 'ShadowReg_Or_LLI_Invalid_ERR' Interrupt in this case.
   c) DW_axi_dmac checks CHx_CTL_ShadowReg.ShadowReg_Or_LLI_Valid bit and if it is seen as '1,' DW_axi_dmac copies the shadow register contents to the registers used for executing the DMA block transfer (CHx_SAR and/or CHx_DAR, CHx_BLOCK_TS and CHx_CTL registers) and clears the ShadowReg_Or_LLI_Valid bit in CHx_CTL and CHx_CTL_ShadowReg registers to 0.
      i. If DW_axi_dmac sees CHx_CTL.ShadowReg_Or_LLI_Last bit of the copied Shadow Register as 1, it understands that the current block is the final block in the transfer and completes the DMA transfer operation at the end of current block transfer.
      ii. If DW_axi_dmac sees CHx_CTL.ShadowReg_Or_LLI_Last bit of the copied Shadow Register as 0, it understands that there are one or more blocks to be transferred and checks CHx_CTL_ShadowReg.ShadowReg_Or_LLI_Valid bit again at the end of current block transfer.
6. Software polls the ShadowReg_Or_LLI_Valid bit in the CHx_CTL register till it is 0.
   a) DW_axi_dmac clears this bit to 0 only after copying the shadow register contents to the registers used for executing the DMA block transfer (that is, the CHx_SAR and/or CHx_DAR, CHx_BLOCK_TS, and CHx_CTL registers).
   b) Software must program the shadow registers with a new set of values only after the ShadowReg_Or_LLI_Valid bit is set to 0.
   c) If software tries to program the shadow registers when the ShadowReg_Or_LLI_Valid bit is set to 1, DW_axi_dmac ignores this write operation, sets the SLVIF_ShadowReg_WrOnValid_ERR bit of the CHx_IntStatusReg register to 1, and generates an interrupt (if the corresponding interrupt generation is not masked off).
7. Software programs the CHx_SAR and/or CHx_DAR, CHx_BLOCK_TS, and CHx_CTL registers with appropriate values for the next block.
   a) The CHx_CTL register must be the last register to be programmed with the ShadowReg_Or_LLI_Valid bit set to 1 to indicate that the shadow register contents are valid.
   b) If current block is the final block in the transfer, software must set CHx_CTL.ShadowReg_Or_LLI_Last bit to 1.

c) The DMA block transfer corresponding to the previous shadow register contents may be in progress during this time.
d) DW_axi_dmac loads the corresponding shadow registers with these new values.

8. DW_axi_dmac initiates the DMA block transfer operation based on the settings for the block transfer.
   a) Based on the settings of TT_FC field in CHx_CFG register, the block transfer might start immediately or after the hardware/software handshaking request.
   b) DW_axi_dmac checks CHx_CTL_ShadowReg.ShadowReg_Or_LLI_Valid bit and if it is seen as 0, DW_axi_dmac waits until software writes (any value) to CHx_BLK_TFR_ResumeReqReg to indicate valid LLI availability, before attempting another Shadow Register fetch operation. DW_axi_dmac might generate ShadowReg_Or_LLI_Invalid_ERR interrupt in this case.
   c) DW_axi_dmac checks CHx_CTL_ShadowReg.ShadowReg_Or_LLI_Valid bit and if it is seen as 1, DW_axi_dmac copies the shadow register contents to the registers used for executing the DMA block transfer (CHx_SAR and/or CHx_DAR, CHx_BLOCK_TS and CHx_CTL registers) and clears the ShadowReg_Or_LLI_Valid bit in CHx_CTL and CHx_CTL_ShadowReg registers to 0.
   d) If DW_axi_dmac sees CHx_CTL.ShadowReg_Or_LLI_Last bit of the copied Shadow Register as 1, it understands that the current block is the final block in the transfer and completes the DMA transfer operation at the end of current block transfer.
   e) If DW_axi_dmac sees CHx_CTL.ShadowReg_Or_LLI_Last bit of the copied Shadow Register as 0, it understands that there are one or more blocks to be transferred and checks CHx_CTL_ShadowReg.ShadowReg_Or_LLI_Valid bit again at the end of current block transfer.
9. Software waits for the block transfer completion interrupt or polls the block transfer completion indication bit (BLOCK_TFR_DONE) of the CHx_IntStatusReg register until it is set to 1.
10. On block transfer completion:
   a) DW_axi_dmac checks CHx_CTL_ShadowReg.ShadowReg_Or_LLI_Valid bit and if it is seen as 0, DW_axi_dmac waits until software writes (any value) to CHx_BLK_TFR_ResumeReqReg to indicate valid LLI availability, before attempting another Shadow Register fetch operation. DW_axi_dmac might generate a ShadowReg_Or_LLI_Invalid_ERR interrupt in this case.
   b) DW_axi_dmac checks CHx_CTL_ShadowReg.ShadowReg_Or_LLI_Valid bit and if it is seen as 1, DW_axi_dmac copies the shadow register contents to the registers used for executing the DMA block transfer (CHx_SAR and/or CHx_DAR, CHx_BLOCK_TS and CHx_CTL registers) and clears ShadowReg_Or_LLI_Valid bit in CHx_CTL and CHx_CTL_ShadowReg registers to 0.
      i. If CHx_CTL.ShadowReg_Or_LLI_Last bit of the copied Shadow Register is 1, it understands that the current block is the final block in the transfer and completes the DMA transfer operation.
      ii. If CHx_CTL.ShadowReg_Or_LLI_Last bit of the copied Shadow Register is 0, it understands that there are one or more blocks to be transferred and checks CHx_CTL_ShadowReg.ShadowReg_Or_LLI_Valid bit again at the end of current block transfer.
   c) If there are one or more blocks to be transferred, software polls CHx_CTL.ShadowReg_Or_LLI_Valid bit until it is seen as 0 and goes to step 7. One read

operation is enough as DW_axi_dmac should have already copied the shadow register contents and cleared this bit to 0.

14.4.2 Programming Flow for Linked-List-Based Multi-Bock Transfer

1. Software reads the DMAC channel enable register (DMAC_ChEnReg) to select an available (unused) channel.
2. Software programs the CHx_CFG register with appropriate values for the DMA transfer. The SRC_MLTBLK_TYPE and/or DST_MLTBLK_TYPE bits must be set to 2'b11.
3. Software programs the base address of the first linked list item and the master interface on which the linked list item is available in the CHx_LLP register.
4. Software creates one or more linked list items in system memory. Software can create the entire linked list item in advance or dynamically extend the linked list using the CHx_CTL.ShadowReg_Or_LLI_Valid and CHx_CTL.LLI_Last fields of the LLI.
5. Software enables the channel by writing 1 to the appropriate bit location in DMAC_ChEnReg register.
6. DW_axi_dmac initiates the DMA block transfer operation based on the settings for the block transfer. The block transfer might start immediately or after the hardware or software handshaking request, depending on the settings of the TT_FC field in the CHx_CFG register. DW_axi_dmac copies the linked list contents to the registers used for executing the DMA block transfer (that is, the CHx_SAR and/or CHx_DAR, CHx_BLOCK_TS, and CHx_CTL registers) and initiates the DMA block transfer.
7. During the linked list fetch phase:
   a) If DW_axi_dmac sees CHx_CTL.ShadowReg_Or_LLI_Last bit of the fetched LLI as 1, it understands that the current block is the final block in the transfer and completes the DMA transfer operation at the end of current block transfer.
   b) If DW_axi_dmac sees CHx_CTL.ShadowReg_Or_LLI_Last bit of the fetched LLI as 0, it understands that there are one or more blocks to be transferred and goes to step 6.
   c) If DW_axi_dmac sees CHx_CTL.ShadowReg_Or_LLI_Valid bit of the fetched LLI as 0, DW_axi_dmac might generate ShadowReg_Or_LLI_Invalid_ERR Interrupt. DW_axi_dmac waits till software writes (any value) to CHx_BLK_TFR_ResumeReqReg to indicate valid LLI availability, before attempting another LLI read operation.

14.4.3 Programming Flow for Single Block Transfer

1. Software reads the DMAC Channel Enable Register (DMAC_ChEnReg) to choose a free (unused) channel.
2. Software programs CHx_CFG register with multi-block type value of both source and destination peripheral to be 2'b00.
3. Software programs CHx_SAR and/or CHx_DAR, CHx_BLOCK_TS and CHx_CTL registers with appropriate values for the block.

4. Software enables the channel by writing 1 to the appropriate bit location in DMAC_ChEnReg register.
5. Source and destination request single or burst DMA transactions to transfer the block of data (assuming non-memory peripherals). The DW_axi_dmac acknowledges at the completion of every transaction (burst and single) in the block and carries out the block transfer.
6. Software waits for the block transfer completion interrupt/polls the block transfer completion indication bit (BLOCK_TFR_DONE) in CHx_IntStatusReg register till the bit is 1.

14.4.4 Channel Suspend

To suspend a channel during DMA transfer:

1. Software writes a 1 to the channel suspend bit CH_SUSP in the channel enable register, DMAC_ChEnReg.
2. DW_axi_dmac gracefully halts all transfers from the source peripheral, after completing all AXI transfers initiated on the source peripheral.
3. DW_axi_dmac sets CHx_IntStatusReg.CH_SRC_SUSPENDED bit to 1 to indicate that source data transfer is suspended and generates the interrupt if it is not masked off.
4. DW_axi_dmac transfers all the data in channel FIFO to destination peripheral. When CHx_CTL.SRC_TR_WIDTH < CHx_CTL.DST_TR_WIDTH and the DMAC_ChEnReg.CH_SUSP bit is high, there may still be data in the channel FIFO, but not enough to form a single transfer of CHx_CTL.DST_TR_WIDTH. The data remaining in the channel FIFO will be transferred to destination if channel is resumed later which results in filling of more data in channel FIFO.
5. DW_axi_dmac clears channel locking and resets the channel locking settings in the CHx_CFG register.
6. DW_axi_dmac sets the CHx_IntStatusReg.ChLock_Cleared bit to 1 to indicate that channel locking is cleared.
7. DW_axi_dmac sets the CHx_IntStatusReg.CH_SUSPENDED bit to 1 to indicate that the channel is suspended.
8. DW_axi_dmac generates a CH_SUSPENDED interrupt (if it is not masked off).

After a channel suspend, software may either resume the channel after some time, or disable the channel.

14.4.5 Channel Suspend and Resume

To suspend and resume a channel:

1. Follow steps 1 to 4 in Channel Suspend.
2. Software writes a 0 to the channel suspend bit CH_SUSP in the channel enable register, DMAC_ChEnReg.
3. DW_axi_dmac resumes the DMA transfer from the point where it got suspended.

14.4.6 Channel Suspend and Disable Prior to Transfer Completion

To suspend and disable a channel:

1. Follow steps 1 to 4 in Channel Suspend.
2. To disable the suspended channel using software, write a 0 to the channel enable bit (CH_EN) in the channel enable register (DMAC_ChEnReg) after DW_axi_dmac asserts the CHx_IntStatusReg.CH_SUSPENDED bit to 1 to indicate that channel is suspended. When CHx_CTL.SRC_TR_WIDTH < CHx_CTL.DST_TR_WIDTH and the DMAC_ChEnReg.CH_SUSP bit is high, there may still be data in the channel FIFO, but not enough to form a single transfer of CHx_CTL.DST_TR_WIDTH. In this scenario, once the channel is disabled, the remaining data in the channel FIFO is not transferred to the destination peripheral and is lost.
3. DW_axi_dmac sets the CHx_IntStatusReg.CH_DISABLED bit to 1 to indicate that the channel is disabled.
4. DW_axi_dmac generates a CH_DISABLED interrupt (if it is not masked off).
5. DW_axi_dmac clears the DMAC_ChEnReg.CH_EN bit to 0.

14.4.7 Channel Disable Prior to Transfer Completion without Suspend

To disable a channel without suspending:

1. Software writes a 0 to the channel enable bit CH_EN in the channel enable register, DMAC_ChEnReg.
2. DW_axi_dmac gracefully halts all transfers from the source peripheral, after completing all AXI transfers initiated on the source peripheral.
3. DW_axi_dmac transfers all the data in the channel FIFO to the destination peripheral. If CHx_CTL.SRC_TR_WIDTH is less than CHx_CTL.DST_TR_WIDTH and the DMAC_ChEnReg.CH_EN bit is low, there may still be data in the channel FIFO, but not enough to form a single transfer of CHx_CTL.DST_TR_WIDTH. In this scenario, once the channel is disabled, the remaining data in the channel FIFO is not transferred to the destination peripheral and is lost.
4. DW_axi_dmac clears channel locking and resets the channel locking settings in the CHx_CFG register.
5. DW_axi_dmac sets the CHx_IntStatusReg.ChLock_Cleared bit to 1 to indicate that channel locking is cleared.
6. DW_axi_dmac sets the CHx_IntStatusReg.CH_DISABLED bit to 1 to indicate that the channel is disabled.
7. DW_axi_dmac generates a CH_DISABLED interrupt (if it is not masked off).
8. DW_axi_dmac clears the DMAC_ChEnReg.CH_EN bit to 0.

14.5 Registers

Figure & Table 14-6 Possible read and write behaviors

Read (or Write) Behavior	Description
RC	A read clears this register field.

Read (or Write) Behavior	Description
RS	A read sets this register field.
RM	A read modifies the contents of this register field.
Wo	You can only write to this register field once.
W1C	A write of 1 clears this register field.
W1S	A write of 1 sets this register field.
W1T	A write of 1 toggles this register field.
W0C	A write of 0 clears this register field.
W0S	A write of 0 sets this register field.
W0T	A write of 0 toggles this register field.
WC	Any write clears this register field.
WS	Any write sets this register field.
WM	Any write toggles this register field.
No Read Behavior attribute	You cannot read this register. It is Write-Only.
No Write Behavior attribute	You cannot write to this register. It is Read-Only.

Figure & Table 14-7 Memory access examples

Memory Access	Description
R	Read-only register field.
W	Write-only register field.
R/W	Read/write register field.
R/W1C	You can read this register field. Writing 1 clears it.
RC/W1C	Reading this register field clears it. Writing 1 clears it.
R/Wo	You can read this register field. You can only write to it once.

14.5.1 DW_axi_dmac_mem_map/Common_Registers_Address_Block Registers

14.5.1.1 DMAC_IDREG

- Description: DMAC ID Register contains a 64-bit value that is hardwired and read back by a read to the DW_axi_dmac ID Register.
- Size: 64 bits

- Offset: 0x0
- Exists: Always

Figure & Table 14-8 Fields for register: DMAC_IDREG

Bits	Name	Access	Description
63:0	DMAC_ID	R	DMAC ID Number. Value After Reset: DMAX_ID_NUM Exists: Always

14.5.1.2 DMAC_COMPVERREG

- Description: This register contains a 64-bit value that is hardwired and read back by a read to the DW_axi_dmac Component Version Register.
- Size: 64 bits
- Offset: 0x8
- Exists: Always

Figure & Table 14-9 Fields for register: DMAC_COMPVERREG

Bits	Name	Access	Description
63:32	RSVD_DMAC_COMPVERREG	R	DMAC_COMPVERREG Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
31:0	DMAC_COMPVER	R	DMAC Component Version Number Value After Reset: DMAX_COMP_VER Exists: Always

14.5.1.3 DMAC_CFGREG

- Description: This register is used to enable the DW_axi_dmac, which must be done before any channel activity can begin. This register also contains global interrupt enable bit.
- Size: 64 bits
- Offset: 0x10
- Exists: Always

Figure & Table 14-10 Fields for register: DMAC_CFGREG

Bits	Name	Access	Description
63:2	RSVD_DMAC_CFGREG	R	DMAC_CFGREG Reserved bits - Read Only Value After Reset: 0x0 Exists: Always

Bits	Name	Access	Description
1	INT_EN	R/W	This bit is used to globally enable the interrupt generation. ■ 0: DW_axi_dmac Interrupts are disabled. ■ 1: DW_axi_dmac Interrupt logic is enabled. Values: ■ 0x1 (ENABLED): DW_axi_dmac Interrupts are enabled. ■ 0x0 (DISABLED): DW_axi_dmac Interrupts are disabled. Value After Reset: 0x0 Exists: Always
0	DMAC_EN	R/W	This bit is used to enable the DW_axi_dmac. ■ 0: DW_axi_dmac disabled. ■ 1: DW_axi_dmac enabled. NOTE: If this bit DMAC_EN bit is cleared while any channel is still active, then this bit still returns 1 to indicate that there are channels still active until DW_axi_dmac hardware has terminated all activities on all channels, at which point this bit returns zero (0). Values: ■ 0x1 (ENABLED): DW_axi_dmac is enabled. ■ 0x0 (DISABLED): DW_axi_dmac is disabled. Value After Reset: 0x0 Exists: Always

14.5.1.4 DMAC_CHENREG

- Description: This is DW_axi_dmac Channel Enable Register. If software wants to set up a new channel, it can read this register to find out which channels are currently inactive and then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the DW_axi_dmac Global Enable bit (DMAC_CfgReg.DMAC_EN) is 0. When DMAC_CfgReg.DMAC_EN is 0, a write to the DMAC_ChEnReg register is ignored and a read always reads back 0. The channel enable bit, DMAC_ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, DMAC_ChEnReg.CH_EN_WE, is asserted on the same slave interface write transfer. For example, writing hex XXXX01X1 writes a 1 into DMAC_ChEnReg [0], while DMAC_ChEnReg [7:1] remains unchanged. Writing hex XXXX00XX leaves DMAC_ChEnReg [7:0] unchanged. The channel suspend bit, DMAC_ChEnReg.CH_SUSP, is written only if the corresponding channel write enable bit, DMAC_ChEnReg.CH_SUSP_WE, is asserted on the same slave interface write transfer. For example, writing hex 32'h01X1XXXX

writes a 1 into DMAC_ChEnReg [16], while DMAC_ChEnReg [23:17] remains unchanged. Writing hex 32'h00XXXXXX leaves DMAC_ChEnReg [23:16] unchanged. The channel abort bit, DMAC_ChEnReg.CH_ABORT, is written only if the corresponding channel write enable bit, C_ChEnReg.CH_ABORT_WE, is asserted on the same slave interface write transfer.

- Size: 64 bits
- Offset: 0x18
- Exists: Yes

Figure & Table 14-11 Fields for register: DMAC_CHENREG

Bits	Name	Access	Description
63:48	RSVD_DMAC_CHENREG	R	DMAC_CHENREG reserved bits - read only Value After Reset: 0x0 Exists: Always Volatile: True
47	CH8_ABORT_WE	-	This bit is used to write enable the Channel-8 Abort bit. The read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH8_ABORT): Enable Write to CH8_ABORT bit. ■ 0x0 (DISABLE_WR_CH8_ABORT): Disable Write to CH8_ABORT bit. Value After Reset: 0x0 Exists: No
46	CH7_ABORT_WE	-	This bit is used to write enable the Channel-7 Abort bit. The read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH7_ABORT): Enable Write to CH7_ABORT bit. ■ 0x0 (DISABLE_WR_CH7_ABORT): Disable Write to CH7_ABORT bit. Value After Reset: 0x0 Exists: No
45	CH6_ABORT_WE	-	This bit is used to write enable the Channel-6 Abort bit. The read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH6_ABORT): Enable Write to CH6_ABORT bit; ■ 0x0 (DISABLE_WR_CH6_ABORT): Disable Write to CH6_ABORT bit.

Bits	Name	Access	Description
			Value After Reset: 0x0 Exists: No
44	CH5_ABORT_WE	-	This bit is used to write enable the Channel-5 Abort bit. The read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH5_ABORT): Enable Write to CH5_ABORT bit; ■ 0x0 (DISABLE_WR_CH5_ABORT): Disable Write to CH5_ABORT bit. Value After Reset: 0x0 Exists: No
43	CH4_ABORT_WE	R	This bit is used to write enable the Channel-4 Abort bit. The read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH4_ABORT): Enable Write to CH4_ABORT bit. ■ 0x0 (DISABLE_WR_CH4_ABORT): Disable Write to CH4_ABORT bit. Value After Reset: 0x0 Exists: Yes Volatile:True Memory Access: Read-only
42	CH3_ABORT_WE	R	This bit is used to write enable the Channel-3 Abort bit. The read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH3_ABORT): Enable Write to CH3_ABORT bit. ■ 0x0 (DISABLE_WR_CH3_ABORT): Disable Write to CH3_ABORT bit. Value After Reset: 0x0 Exists: Yes Volatile: True Memory Access: Read-only
41	CH2_ABORT_WE	R	This bit is used to write enable the Channel-2 Abort bit. The read back value of this register bit is always 0. Values:

Bits	Name	Access	Description
			■ 0x1 (ENABLE_WR_CH2_ABORT): Enable Write to CH2_ABORT bit. ■ 0x0 (DISABLE_WR_CH2_ABORT): Disable Write to CH2_ABORT bit. Value After Reset: 0x0 Exists: Yes Volatile: True Memory Access: Read-only
40	CH1_ABORT_WE	R	This bit is used to write enable the Channel-1 Abort bit. The read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH1_ABORT): Enable Write to CH1_ABORT bit. ■ 0x0 (DISABLE_WR_CH1_ABORT): Disable Write to CH1_ABORT bit. Value After Reset: 0x0 Exists: Yes Volatile: True Memory Access: Read-only
39	CH8_ABORT	-	Channel-8 Abort Request Software sets this bit to 1 to request channel abort. If this bit is set to 1, DW_axi_dmac disables the channel immediately. Aborting the channel might result in AXI Protocol violation as DW_axi_dmac does not make sure that all AXI transfers initiated on the master interface are completed. Aborting the channel is not recommended and should be used only in situations where a particular channel hangs due to no response from the corresponding AXI slave interface and software wants to disable the channel without resetting the entire DW_axi_dmac. It is recommended to try channel disabling first and then only opt for channel aborting. ■ 0: No Channel Abort Request. ■ 1: Request for Channel Abort. DW_axi_dmac clears this bit to 0 once the channel is aborted (when it sets CH8_Status.CH_ABORTED bit to 1). Values: ■ 0x1 (ENABLE_CH8_ABORT): Request for Channel-8

Bits	Name	Access	Description
			Abort. ■ 0x0 (DISABLE_CH8_ABORT): No Request for Channel-8 Abort. Value After Reset: 0x0 Exists: No
38	CH7_ABORT	-	Channel-7 Abort Request Software sets this bit to 1 to request channel abort. If this bit is set to 1, DW_axi_dmac disables the channel immediately. Aborting the channel might result in AXI Protocol violation as DW_axi_dmac does not make sure that all AXI transfers initiated on the master interface are completed. Aborting the channel is not recommended and should be used only in situations where a particular channel hangs due to no response from the corresponding AXI slave interface and software wants to disable the channel without resetting the entire DW_axi_dmac. It is recommended to try channel disabling first and then only opt for channel aborting. ■ 0: No Channel Abort Request. ■ 1: Request for Channel Abort. DW_axi_dmac clears this bit to 0 once the channel is aborted (when it sets CH7_Status.CH_ABORTED bit to 1). Values: ■ 0x1 (ENABLE_CH7_ABORT): Request for Channel-7 Abort. ■ 0x0 (DISABLE_CH7_ABORT): No Request for Channel-7 Abort. Value After Reset: 0x0 Exists: No
37	CH6_ABORT	-	Channel-6 Abort Request Software sets this bit to 1 to request channel abort. If this bit is set to 1, DW_axi_dmac disables the channel immediately. Aborting the channel might result in AXI Protocol violation as DW_axi_dmac does not make sure that all AXI transfers initiated on the master interface are completed. Aborting the channel is not recommended and should be used only in situations where a particular channel hangs due to no response from the corresponding AXI slave interface and software wants to disable the channel without

Bits	Name	Access	Description
			resetting the entire DW_axi_dmac. It is recommended to try channel disabling first and then only opt for channel aborting. ■ 0: No Channel Abort Request. ■ 1: Request for Channel Abort. DW_axi_dmac clears this bit to 0 once the channel is aborted (when it sets CH6_Status.CH_ABORTED bit to 1). Values: ■ 0x1 (ENABLE_CH6_ABORT): Request for Channel-6 Abort. ■ 0x0 (DISABLE_CH6_ABORT): No Request for Channel-6 Abort. Value After Reset: 0x0 Exists: No
36	CH5_ABORT	-	Channel-5 Abort Request Software sets this bit to 1 to request channel abort. If this bit is set to 1, DW_axi_dmac disables the channel immediately. Aborting the channel might result in AXI Protocol violation as DW_axi_dmac does not make sure that all AXI transfers initiated on the master interface are completed. Aborting the channel is not recommended and should be used only in situations where a particular channel hangs due to no response from the corresponding AXI slave interface and software wants to disable the channel without resetting the entire DW_axi_dmac. It is recommended to try channel disabling first and then only opt for channel aborting. ■ 0: No Channel Abort Request. ■ 1: Request for Channel Abort. DW_axi_dmac clears this bit to 0 once the channel is aborted (when it sets CH5_Status.CH_ABORTED bit to 1). Values: ■ 0x1 (ENABLE_CH5_ABORT): Request for Channel-5 Abort. ■ 0x0 (DISABLE_CH5_ABORT): No Request for Channel-5 Abort. Value After Reset: 0x0 Exists: No
35	CH4_ABORT	R	Channel-4 Abort Request

Bits	Name	Access	Description
			Software sets this bit to 1 to request channel abort. If this bit is set to 1, DW_axi_dmac disables the channel immediately. Aborting the channel might result in AXI Protocol violation as DW_axi_dmac does not make sure that all AXI transfers initiated on the master interface are completed. Aborting the channel is not recommended and should be used only in situations where a particular channel hangs due to no response from the corresponding AXI slave interface and software wants to disable the channel without resetting the entire DW_axi_dmac. It is recommended to try channel disabling first and then only opt for channel aborting. ■ 0: No Channel Abort Request. ■ 1: Request for Channel Abort. DW_axi_dmac clears this bit to 0 once the channel is aborted (when it sets CH4_Status.CH_ABORTED bit to 1). Values: ■ 0x1 (ENABLE_CH4_ABORT): Request for Channel-4 Abort. ■ 0x0 (DISABLE_CH4_ABORT): No Request for Channel-4 Abort. Value After Reset: 0x0 Exists: Yes Volatile: True Memory Access: Read-only
34	CH3_ABORT	R	Channel-3 Abort Request Software sets this bit to 1 to request channel abort. If this bit is set to 1, DW_axi_dmac disables the channel immediately. Aborting the channel might result in AXI Protocol violation as DW_axi_dmac does not make sure that all AXI transfers initiated on the master interface are completed. Aborting the channel is not recommended and should be used only in situations where a particular channel hangs due to no response from the corresponding AXI slave interface and software wants to disable the channel without resetting the entire DW_axi_dmac. It is recommended to try channel disabling first and then only opt for channel aborting. ■ 0: No Channel Abort Request. ■ 1: Request for Channel Abort.

Bits	Name	Access	Description
			DW_axi_dmac clears this bit to 0 once the channel is aborted (when it sets CH3_Status.CH_ABORTED bit to 1). Values: ■ 0x1 (ENABLE_CH3_ABORT): Request for Channel-3 Abort. ■ 0x0 (DISABLE_CH3_ABORT): No Request for Channel-3 Abort. Value After Reset: 0x0 Exists: Yes Volatile: True Memory Access: Read-only
33	CH2_ABORT	R	Channel-2 Abort Request Software sets this bit to 1 to request channel abort. If this bit is set to 1, DW_axi_dmac disables the channel immediately. Aborting the channel might result in AXI Protocol violation as DW_axi_dmac does not make sure that all AXI transfers initiated on the master interface are completed. Aborting the channel is not recommended and should be used only in situations where a particular channel hangs due to no response from the corresponding AXI slave interface and software wants to disable the channel without resetting the entire DW_axi_dmac. It is recommended to try channel disabling first and then only opt for channel aborting. ■ 0: No Channel Abort Request. ■ 1: Request for Channel Abort. DW_axi_dmac clears this bit to 0 once the channel is aborted (when it sets CH2_Status.CH_ABORTED bit to 1). Values: ■ 0x1 (ENABLE_CH2_ABORT): Request for Channel-2 Abort; ■ 0x0 (DISABLE_CH2_ABORT): No Request for Channel-2 Abort. Value After Reset: 0x0 Exists: Yes Volatile: True Memory Access: Read-only
32	CH1_ABORT	R	Channel-1 Abort Request

Bits	Name	Access	Description
			Software sets this bit to 1 to request channel abort. If this bit is set to 1, DW_axi_dmac disables the channel immediately. Aborting the channel might result in AXI Protocol violation as DW_axi_dmac does not make sure that all AXI transfers initiated on the master interface are completed. Aborting the channel is not recommended and should be used only in situations where a particular channel hangs due to no response from the corresponding AXI slave interface and software wants to disable the channel without resetting the entire DW_axi_dmac. It is recommended to try channel disabling first and then only opt for channel aborting. ■ 0: No Channel Abort Request. ■ 1: Request for Channel Abort. DW_axi_dmac clears this bit to 0 once the channel is aborted (when it sets CH1_Status.CH_ABORTED bit to 1). Values: ■ 0x1 (ENABLE_CH1_ABORT): Request for Channel-1 Abort. ■ 0x0 (DISABLE_CH1_ABORT): No Request for Channel-1 Abort. Value After Reset: 0x0 Exists: Yes Volatile: True Memory Access: Read-only
31	CH8_SUSP_WE	-	This bit is used as a write enable to the Channel-8 Suspend bit. The read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH8_SUSP): Enable Write to respective CH8_SUSP bit. ■ 0x0 (DISABLE_WR_CH8_SUSP): Disable Write to CH8_SUSP bit. Value After Reset: 0x0 Exists: No
30	CH7_SUSP_WE	-	This bit is used as a write enable to the Channel-7 Suspend bit. The read back value of this register bit is always 0. Values:

Bits	Name	Access	Description
			■ 0x1 (ENABLE_WR_CH7_SUSP): Enable Write to respective CH7_SUSP bit. ■ 0x0 (DISABLE_WR_CH7_SUSP): Disable Write to CH7_SUSP bit. Value After Reset: 0x0 Exists: No
29	CH6_SUSP_WE	-	This bit is used as a write enable to the Channel-6 Suspend bit. The read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH6_SUSP): Enable Write to respective CH6_SUSP bit. ■ 0x0 (DISABLE_WR_CH6_SUSP): Disable Write to CH6_SUSP bit. Value After Reset: 0x0 Exists: No
28	CH5_SUSP_WE	-	This bit is used as a write enable to the Channel-5 Suspend bit. The read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH5_SUSP): Enable Write to respective CH5_SUSP bit. ■ 0x0 (DISABLE_WR_CH5_SUSP): Disable Write to CH5_SUSP bit. Value After Reset: 0x0 Exists: No
27	CH4_SUSP_WE	W	This bit is used as a write enable to the Channel-4 Suspend bit. The read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH4_SUSP): Enable Write to respective CH4_SUSP bit. ■ 0x0 (DISABLE_WR_CH4_SUSP): Disable Write to CH4_SUSP bit. Value After Reset: 0x0 Exists: Yes Volatile: True
26	CH3_SUSP_WE	W	This bit is used as a write enable to the Channel-3

Bits	Name	Access	Description
			Suspend bit. The read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH3_SUSP): Enable Write to respective CH3_SUSP bit. ■ 0x0 (DISABLE_WR_CH3_SUSP): Disable Write to CH3_SUSP bit. Value After Reset: 0x0 Exists: Yes Volatile: True
25	CH2_SUSP_WE	W	This bit is used as a write enable to the Channel-2 Suspend bit. The read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH2_SUSP): Enable Write to respective CH2_SUSP bit. ■ 0x0 (DISABLE_WR_CH2_SUSP): Disable Write to CH2_SUSP bit. Value After Reset: 0x0 Exists: Yes Volatile: True
24	CH1_SUSP_WE	W	This bit is used as a write enable to the Channel-1 Suspend bit. The read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH1_SUSP): Enable Write to respective CH1_SUSP bit. ■ 0x0 (DISABLE_WR_CH1_SUSP): Disable Write to CH1_SUSP bit. Value After Reset: 0x0 Exists: Yes Volatile: True
23	CH8_SUSP	-	Channel-8 Suspend Request Software sets this bit to 1 to request channel suspend. If this bit is set to 1, DW_axi_dmac suspends all DMA data transfers from the source gracefully until this bit is cleared. There is no guarantee that the current dma transaction will complete. This bit can also be used in conjunction with CH8_Status.CH_SUSPENDED to cleanly

Bits	Name	Access	Description
			disable the channel without losing any data. In this case, software first sets CH8_SUSP bit to 1 and polls CH8_Status.CH_SUSPENDED till it is set to 1. Software can then clear CH8_EN bit to 0 to disable the channel. ■ 0: No Channel Suspend Request. ■ 1: Request for Channel Suspend. Software can clear CH8_SUSP bit to 0, after DW_axi_dmac sets CH8_Status.CH_SUSPENDED bit to 1, to exit the channel suspend mode. Note: CH_SUSP is cleared when channel is disabled. Values: ■ 0x1 (ENABLE_CH8_SUSP): Request to Suspended Channel-8. ■ 0x0 (DISABLE_CH8_SUSP): No Channel Suspend Request. Value After Reset: 0x0 Exists: No
22	CH7_SUSP	-	Channel-7 Suspend Request Software sets this bit to 1 to request channel suspend. If this bit is set to 1, DW_axi_dmac suspends all DMA data transfers from the source gracefully until this bit is cleared. There is no guarantee that the current dma transaction will complete. This bit can also be used in conjunction with CH7_Status.CH_SUSPENDED to cleanly disable the channel without losing any data. In this case, software first sets CH7_SUSP bit to 1 and polls CH7_Status.CH_SUSPENDED till it is set to 1. Software can then clear CH7_EN bit to 0 to disable the channel. ■ 0: No Channel Suspend Request. ■ 1: Request for Channel Suspend. Software can clear CH7_SUSP bit to 0, after DW_axi_dmac sets CH7_Status.CH_SUSPENDED bit to 1, to exit the channel suspend mode. Note: CH_SUSP is cleared when channel is disabled. Values: ■ 0x1 (ENABLE_CH7_SUSP): Request to Suspended Channel-7. ■ 0x0 (DISABLE_CH7_SUSP): No Channel Suspend Request. Value After Reset: 0x0

Bits	Name	Access	Description
			Exists: No
21	CH6_SUSP	-	Channel-6 Suspend Request Software sets this bit to 1 to request channel suspend. If this bit is set to 1, DW_axi_dmac suspends all DMA data transfers from the source gracefully until this bit is cleared. There is no guarantee that the current dma transaction will complete. This bit can also be used in conjunction with CH6_Status.CH_SUSPENDED to cleanly disable the channel without losing any data. In this case, software first sets CH6_SUSP bit to 1 and polls CH6_Status.CH_SUSPENDED till it is set to 1. Software can then clear CH6_EN bit to 0 to disable the channel. ■ 0: No Channel Suspend Request. ■ 1: Request for Channel Suspend. Software can clear CH6_SUSP bit to 0, after DW_axi_dmac sets CH6_Status.CH_SUSPENDED bit to 1, to exit the channel suspend mode. Note: CH_SUSP is cleared when channel is disabled. Values: ■ 0x1 (ENABLE_CH6_SUSP): Request to Suspended Channel-6. ■ 0x0 (DISABLE_CH6_SUSP): No Channel Suspend Request. Value After Reset: 0x0 Exists: No
20	CH5_SUSP	-	Channel-5 Suspend Request Software sets this bit to 1 to request channel suspend. If this bit is set to 1, DW_axi_dmac suspends all DMA data transfers from the source gracefully until this bit is cleared. There is no guarantee that the current dma transaction will complete. This bit can also be used in conjunction with CH5_Status.CH_SUSPENDED to cleanly disable the channel without losing any data. In this case, software first sets CH5_SUSP bit to 1 and polls CH5_Status.CH_SUSPENDED till it is set to 1. Software can then clear CH5_EN bit to 0 to disable the channel. ■ 0: No Channel Suspend Request. ■ 1: Request for Channel Suspend. Software can clear CH5_SUSP bit to 0, after DW_axi_dmac sets CH5_Status.CH_SUSPENDED bit to 1,

Bits	Name	Access	Description
			to exit the channel suspend mode. Note: CH_SUSP is cleared when channel is disabled. Values: ■ 0x1 (ENABLE_CH5_SUSP): Request to Suspended Channel-5. ■ 0x0 (DISABLE_CH5_SUSP): No Channel Suspend Request. Value After Reset: 0x0 Exists: No
19	CH4_SUSP	R/W	Channel-4 Suspend Request Software sets this bit to 1 to request channel suspend. If this bit is set to 1, DW_axi_dmac suspends all DMA data transfers from the source gracefully until this bit is cleared. There is no guarantee that the current dma transaction will complete. This bit can also be used in conjunction with CH4_Status.CH_SUSPENDED to cleanly disable the channel without losing any data. In this case, software first sets CH4_SUSP bit to 1 and polls CH4_Status.CH_SUSPENDED till it is set to 1. Software can then clear CH4_EN bit to 0 to disable the channel. ■ 0: No Channel Suspend Request. ■ 1: Request for Channel Suspend. Software can clear CH4_SUSP bit to 0, after DW_axi_dmac sets CH4_Status.CH_SUSPENDED bit to 1, to exit the channel suspend mode. Note: CH_SUSP is cleared when channel is disabled. Values: ■ 0x1 (ENABLE_CH4_SUSP): Request to Suspended Channel-4. ■ 0x0 (DISABLE_CH4_SUSP): No Channel Suspend Request. Value After Reset: 0x0 Exists: Yes Volatile: True
18	CH3_SUSP	R/W	Channel-3 Suspend Request Software sets this bit to 1 to request channel suspend. If this bit is set to 1, DW_axi_dmac suspends all DMA data transfers from the source gracefully until this bit is cleared. There is no guarantee that the current DMA

Bits	Name	Access	Description
			transaction will complete. This bit can also be used in conjunction with CH3_Status.CH_SUSPENDED to cleanly disable the channel without losing any data. In this case, software first sets CH3_SUSP bit to 1 and polls CH3_Status.CH_SUSPENDED till it is set to 1. Software can then clear CH3_EN bit to 0 to disable the channel. ■ 0: No Channel Suspend Request. ■ 1: Request for Channel Suspend. Software can clear CH3_SUSP bit to 0, after DW_axi_dmac sets CH3_Status.CH_SUSPENDED bit to 1, to exit the channel suspend mode. Note: CH_SUSP is cleared when channel is disabled. Values: ■ 0x1 (ENABLE_CH3_SUSP): Request to Suspended Channel-3. ■ 0x0 (DISABLE_CH3_SUSP): No Channel Suspend Request. Value After Reset: 0x0 Exists: Yes Volatile: True
17	CH2_SUSP	R/W	Channel-2 Suspend Request Software sets this bit to 1 to request channel suspend. If this bit is set to 1, DW_axi_dmac suspends all DMA data transfers from the source gracefully until this bit is cleared. There is no guarantee that the current dma transaction will complete. This bit can also be used in conjunction with CH2_Status.CH_SUSPENDED to cleanly disable the channel without losing any data. In this case, software first sets CH2_SUSP bit to 1 and polls CH2_Status.CH_SUSPENDED till it is set to 1. Software can then clear CH2_EN bit to 0 to disable the channel. ■ 0: No Channel Suspend Request. ■ 1: Request for Channel Suspend. Software can clear CH2_SUSP bit to 0, after DW_axi_dmac sets CH2_Status.CH_SUSPENDED bit to 1, to exit the channel suspend mode. Note: CH_SUSP is cleared when channel is disabled. Values: ■ 0x1 (ENABLE_CH2_SUSP): Request to Suspended Channel-2.

Bits	Name	Access	Description
			■ 0x0 (DISABLE_CH2_SUSP): No Channel Suspend Request. Value After Reset: 0x0 Exists: Yes Volatile: True
16	CH1_SUSP	R/W	Channel-1 Suspend Request Software sets this bit to 1 to request channel suspend. If this bit is set to 1, DW_axi_dmac suspends all DMA data transfers from the source gracefully until this bit is cleared. There is no guarantee that the current dma transaction will complete. This bit can also be used in conjunction with CH1_Status.CH_SUSPENDED to cleanly disable the channel without losing any data. In this case, software first sets CH1_SUSP bit to 1 and polls CH1_Status.CH_SUSPENDED till it is set to 1. Software can then clear CH1_EN bit to 0 to disable the channel. ■ 0: No Channel Suspend Request. ■ 1: Request for Channel Suspend. Software can clear CH1_SUSP bit to 0, after DW_axi_dmac sets CH1_Status.CH_SUSPENDED bit to 1, to exit the channel suspend mode. Note: CH_SUSP is cleared when channel is disabled. Values: ■ 0x1 (ENABLE_CH1_SUSP): Request to Suspended Channel-1. ■ 0x0 (DISABLE_CH1_SUSP): No Channel Suspend Request. Value After Reset: 0x0 Exists: Yes Volatile: True
15	CH8_EN_WE	-	DW_axi_dmac Channel-8 Enable Write Enable bit. Read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH8_EN): Enable Write to CH8_EN bit. ■ 0x0 (DISABLE_WR_CH8_EN): Disable Write to respective CH8_EN bit. Value After Reset: 0x0 Exists: No

Bits	Name	Access	Description
14	CH7_EN_WE	-	DW_axi_dmac Channel-7 Enable Write Enable bit. Read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH7_EN): Enable Write to CH7_EN bit. ■ 0x0 (DISABLE_WR_CH7_EN): Disable Write to respective CH7_EN bit. Value After Reset: 0x0 Exists: No
13	CH6_EN_WE	-	DW_axi_dmac Channel-6 Enable Write Enable bit. Read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH6_EN): Enable Write to CH6_EN bit. ■ 0x0 (DISABLE_WR_CH6_EN): Disable Write to respective CH6_EN bit. Value After Reset: 0x0 Exists: No
12	CH5_EN_WE	-	DW_axi_dmac Channel-5 Enable Write Enable bit. Read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH5_EN): Enable Write to CH5_EN Bit. ■ 0x0 (DISABLE_WR_CH5_EN): Disable Write to respective CH5_EN bit. Value After Reset: 0x0 Exists: No
11	CH4_EN_WE	W	DW_axi_dmac Channel-4 Enable Write Enable bit. Read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH4_EN): Enable Write to CH4_EN bit; ■ 0x0 (DISABLE_WR_CH4_EN): Disable Write to respective CH4_EN bit. Value After Reset: 0x0 Exists: Yes Volatile: True

Bits	Name	Access	Description
10	CH3_EN_WE	W	DW_axi_dmac Channel-3 Enable Write Enable bit. Read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH3_EN): Enable Write to CH3_EN bit. ■ 0x0 (DISABLE_WR_CH3_EN): Disable Write to respective CH3_EN bit. Value After Reset: 0x0 Exists: Yes Volatile: True
9	CH2_EN_WE	W	DW_axi_dmac Channel-2 Enable Write Enable bit. Read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH2_EN): Enable Write to CH2_EN Bit. ■ 0x0 (DISABLE_WR_CH2_EN): Disable Write to respective CH2_EN bit. Value After Reset: 0x0 Exists: Yes Volatile: True
8	CH1_EN_WE	W	DW_axi_dmac Channel-1 Enable Write Enable bit. Read back value of this register bit is always 0. Values: ■ 0x1 (ENABLE_WR_CH1_EN): Enable Write to CH1_EN bit. ■ 0x0 (DISABLE_WR_CH1_EN): Disable Write to respective CH1_EN bit. Value After Reset: 0x0 Exists: Yes Volatile: True
7	CH8_EN	-	This bit is used to enable the DW_axi_dmac Channel-8. ■ 0: DW_axi_dmac Channel-8 is disabled. ■ 1: DW_axi_dmac Channel-8 is enabled. The bit 'DMAC_ChEnReg.CH8_EN' is automatically cleared by hardware to disable the channel after the last AMBA transfer of the DMA transfer to the destination has completed. Software can therefore poll

Bits	Name	Access	Description
			this bit to determine when this channel is free for a new DMA transfer. Values: ■ 0x1 (ENABLE_CH8): DW_axi_dmac: Channel-8 is enabled. ■ 0x0 (DISABLE_CH8): DW_axi_dmac: Channel-8 is disabled. Value After Reset: 0x0 Exists: No
6	CH7_EN	-	This bit is used to enable the DW_axi_dmac Channel-7. ■ 0: DW_axi_dmac Channel-7 is disabled. ■ 1: DW_axi_dmac Channel-7 is enabled. The bit 'DMAC_ChEnReg.CH7_EN' is automatically cleared by hardware to disable the channel after the last AMBA transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer. Values: ■ 0x1 (ENABLE_CH7): DW_axi_dmac: Channel-7 is enabled. ■ 0x0 (DISABLE_CH7): DW_axi_dmac: Channel-7 is disabled. Value After Reset: 0x0 Exists: No
5	CH6_EN	-	This bit is used to enable the DW_axi_dmac Channel-6. ■ 0: DW_axi_dmac Channel-6 is disabled. ■ 1: DW_axi_dmac Channel-6 is enabled. The bit 'DMAC_ChEnReg.CH6_EN' is automatically cleared by hardware to disable the channel after the last AMBA transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer. Values: ■ 0x1 (ENABLE_CH6): DW_axi_dmac: Channel-6 is enabled; ■ 0x0 (DISABLE_CH6): DW_axi_dmac: Channel-6 is disabled.

Bits	Name	Access	Description
			Value After Reset: 0x0 Exists: No
4	CH5_EN	-	This bit is used to enable the DW_axi_dmac Channel-5. ■ 0: DW_axi_dmac Channel-5 is disabled. ■ 1: DW_axi_dmac Channel-5 is enabled. The bit 'DMAC_ChEnReg.CH5_EN' is automatically cleared by hardware to disable the channel after the last AMBA transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer. Values: ■ 0x1 (ENABLE_CH5): DW_axi_dmac: Channel-5 is enabled. ■ 0x0 (DISABLE_CH5): DW_axi_dmac: Channel-5 is disabled. Value After Reset: 0x0 Exists: No
3	CH4_EN	R/W	This bit is used to enable the DW_axi_dmac Channel-4. ■ 0: DW_axi_dmac Channel-4 is disabled. ■ 1: DW_axi_dmac Channel-4 is enabled. The bit 'DMAC_ChEnReg.CH4_EN' is automatically cleared by hardware to disable the channel after the last AMBA transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer. Values: ■ 0x1 (ENABLE_CH4): DW_axi_dmac: Channel-4 is enabled. ■ 0x0 (DISABLE_CH4): DW_axi_dmac: Channel-4 is disabled. Value After Reset: 0x0 Exists: Yes Volatile: True
2	CH3_EN	R/W	This bit is used to enable the DW_axi_dmac Channel-3. ■ 0: DW_axi_dmac Channel-3 is disabled. ■ 1: DW_axi_dmac Channel-3 is enabled.

Bits	Name	Access	Description
			The bit 'DMAC_ChEnReg.CH3_EN' is automatically cleared by hardware to disable the channel after the last AMBA transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer. Values: ■ 0x1 (ENABLE_CH3): DW_axi_dmac: Channel-3 is enabled. ■ 0x0 (DISABLE_CH3): DW_axi_dmac: Channel-3 is disabled. Value After Reset: 0x0 Exists: Yes Volatile: True
1	CH2_EN	R/W	This bit is used to enable the DW_axi_dmac Channel-2. ■ 0: DW_axi_dmac Channel-2 is disabled. ■ 1: DW_axi_dmac Channel-2 is enabled. The bit 'DMAC_ChEnReg.CH2_EN' is automatically cleared by hardware to disable the channel after the last AMBA transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer. Values: ■ 0x1 (ENABLE_CH2): DW_axi_dmac: Channel-2 is enabled. ■ 0x0 (DISABLE_CH2): DW_axi_dmac: Channel-2 is disabled. Value After Reset: 0x0 Exists: Yes Volatile: True
0	CH1_EN	R/W	This bit is used to enable the DW_axi_dmac Channel-1. ■ 0: DW_axi_dmac Channel-1 is disabled. ■ 1: DW_axi_dmac Channel-1 is enabled. The bit 'DMAC_ChEnReg.CH1_EN' is automatically cleared by hardware to disable the channel after the last AMBA transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new

Bits	Name	Access	Description
			DMA transfer. Values: ■ 0x1 (ENABLE_CH1): DW_axi_dmac: Channel-1 is enabled. ■ 0x0 (DISABLE_CH1): DW_axi_dmac: Channel-1 is disabled. Value After Reset: 0x0 Exists: Yes Volatile: True

14.5.1.5 DMAC_INTSTATUSREG

- Description: DMAC Interrupt Status Register captures the combined channel interrupt for each channel and combined common register block interrupt. This register is present provided number of DMA channels are greater than 8.
- Size: 64 bits
- Offset: 0x30
- Exists: Yes

Figure & Table 14-12 Fields for register: DMAC_INTSTATUSREG

Bits	Name	Access	Description
63:17	RSVD_DMAC_INTSTATUSREG_ 63to17	R	DMAC Interrupt Status Register (bits 63 to 17) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always Volatile: True
16	CommonReg_IntStat	R	Common Register Interrupt Status bit Values: ■ 0x1 (ACTIVE): Common Register Interrupt is Active. ■ 0x0 (INACTIVE): Common Register Interrupt is Inactive. Value After Reset: 0x0 Exists: Always Volatile: True
15:8	RSVD_DMAC_INTSTATUSREG	R	DMAC Interrupt Status Register (bits 15 to 8) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always

Bits	Name	Access	Description
			Volatile: True
7	CH8_IntStat	-	Channel 8 Interrupt Status bit Values: ■ 0x1 (ACTIVE): Channel ${ch_num} Interrupt is Active. ■ 0x0 (INACTIVE): Channel ${ch_num} Interrupt is Inactive. Value After Reset: 0x0 Exists: No
6	CH7_IntStat	-	Channel 7 Interrupt Status bit Values: ■ 0x1 (ACTIVE): Channel ${ch_num} Interrupt is Active. ■ 0x0 (INACTIVE): Channel ${ch_num} Interrupt is Inactive. Value After Reset: 0x0 Exists: No
5	CH6_IntStat	-	Channel 6 Interrupt Status Bit. Values: ■ 0x1 (ACTIVE): Channel ${ch_num} Interrupt is Active. ■ 0x0 (INACTIVE): Channel ${ch_num} Interrupt is Inactive. Value After Reset: 0x0 Exists: No
4	CH5_IntStat	-	Channel 5 Interrupt Status Bit. Values: ■ 0x1 (ACTIVE): Channel ${ch_num} Interrupt is Active. ■ 0x0 (INACTIVE): Channel ${ch_num} Interrupt is Inactive. Value After Reset: 0x0 Exists: No
3	CH4_IntStat	R	Channel 4 Interrupt Status Bit. Values: ■ 0x1 (ACTIVE): Channel ${ch_num} Interrupt is Active.

Bits	Name	Access	Description
			■ 0x0 (INACTIVE): Channel ${ch_num} Interrupt is Inactive. Value After Reset: 0x0 Exists: Yes Volatile: True
2	CH3_IntStat	R	Channel 3 Interrupt Status Bit. Values: ■ 0x1 (ACTIVE): Channel ${ch_num} Interrupt is Active. ■ 0x0 (INACTIVE): Channel ${ch_num} Interrupt is Inactive. Value After Reset: 0x0 Exists: Yes Volatile: true
1	CH2_IntStat	R	Channel 2 Interrupt Status Bit. Values: ■ 0x1 (ACTIVE): Channel ${ch_num} Interrupt is Active. ■ 0x0 (INACTIVE): Channel ${ch_num} Interrupt is Inactive. Value After Reset: 0x0 Exists: Yes Volatile: True
0	CH1_IntStat	R	Channel 1 Interrupt Status Bit. Values: ■ 0x1 (ACTIVE): Channel ${ch_num} Interrupt is Active. ■ 0x0 (INACTIVE): Channel ${ch_num} Interrupt is Inactive. Value After Reset: 0x0 Exists: Yes Volatile: True

14.5.1.6 DMAC_COMMONREG_INTCLEARREG

- Description: Writing 1 to specific field clears the corresponding field in DMAC Common register Interrupt Status Register (DMAC_CommonReg_IntStatusReg).
- Size: 64 bits

- Offset: 0x38
- Exists: Always

Figure & Table 14-13 Fields for register: DMAC_COMMONREG_INTCLEARREG

Bits	Name	Access	Description
63:9	RSVD_DMAC_COMMONREG_INTCLEARREG_63to9	W	DMAC Common Register Interrupt Clear Register (bits 63 to 9) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
8	Clear_SLVIF_UndefinedReg_DEC_ERR_IntStat	W	Slave Interface Undefined register Decode Error Interrupt clear Bit. This bit is used to clear the corresponding channel interrupt status bit SLVIF_UndefinedReg_DEC_ERR_IntStat in DMAC_CommonReg_IntStatusReg. Values: ■ 0x1 (CLEAR_SLVIF_UndefinedReg_DEC_ERR): Clear the SLVIF_UndefinedReg_DEC_ERR interrupt in the interrupt register DMAC_CommonReg_IntStatusReg. ■ 0x0 (No_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
7:4	RSVD_DMAC_COMMONREG_INTCLEARREG_7to4	W	DMAC Common Register Interrupt Clear Register (bits 7 to 4) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
3	Clear_SLVIF_CommonReg_WrOnHold_ERR_IntStat	W	Slave Interface Common Register Write On Hold Error Interrupt clear Bit. This bit is used to clear the corresponding channelinterrupt status bit SLVIF_CommonReg_WrOnHold_ERR_IntStat in DMAC_CommonReg_IntStatusReg. Values: ■ 0x1 (CLEAR_SLVIF_CommonReg_WrOnHold_ERR): Clear the SLVIF_CommonReg_WrOnHold_ERR interrupt in the interrupt register DMAC_CommonReg_IntStatusReg. ■ 0x0 (No_ACTION): Inactive signal. No action taken. Value After Reset: 0x0

Bits	Name	Access	Description
			Exists: Always
2	Clear_SLVIF_CommonReg_RD2WO_ERR_IntStat	W	Slave Interface Common Register Read to Write only Error Interrupt clear Bit. This bit is used to clear the corresponding channelinterrupt status bit SLVIF_CommonReg_RD2WO_ERR_IntStat in DMAC_CommonReg_IntStatusReg. Values: ■ 0x1 (CLEAR_SLVIF_CommonReg_RD2WO_ERR): Clear the SLVIF_CommonReg_RD2WO_ERR interrupt in the interrupt register DMAC_CommonReg_IntStatusReg. ■ 0x0 (No_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
1	Clear_SLVIF_CommonReg_WR2RO_ERR_IntStat	W	Slave Interface Common Register Write to Read only Error Interrupt clear Bit. This bit is used to clear the corresponding channelinterrupt status bit SLVIF_CommonReg_WR2RO_ERR_IntStat in DMAC_CommonReg_IntStatusReg. Values: ■ 0x1 (CLEAR_SLVIF_CommonReg_WR2RO_ERR): Clear the SLVIF_CommonReg_WR2RO_ERR interrupt in the interrupt register DMAC_CommonReg_IntStatusReg. ■ 0x0 (No_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
0	Clear_SLVIF_CommonReg_DEC_ERR_IntStat	W	Slave Interface Common Register Decode Error Interrupt clear Bit. This bit is used to clear the corresponding channel interrupt status bit SLVIF_CommonReg_DEC_ERR_IntStat in DMAC_CommonReg_IntStatusReg. Values: ■ 0x1 (CLEAR_SLVIF_CommonReg_DEC_ERR): Clear the SLVIF_CommonReg_DEC_ERR interrupt in the interrupt register DMAC_CommonReg_IntStatusReg.

Bits	Name	Access	Description
			■ 0x0 (No_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always

14.5.1.7 DMAC_COMMONREG_INTSTATUS_ENABLEREG

- Description: Writing 1 to specific field enables the corresponding interrupt status generation in DMAC Common register Interrupt Status Register (DMAC_CommonReg_IntStatusReg).
- Size: 64 bits
- Offset: 0x40
- Exists: Always

Figure & Table 14-14 Fields for register: DMAC_COMMONREG_INTSTATUS_ENABLEREG

Bits	Name	Access	Description
63:9	RSVD_DMAC_COMMONREG_ INTSTATUS_ENABLEREG_63to9	R	DMAC Common Register Interrupt Status Enable Register (bits 63 to 9) Reserved bits - Read Only Value After Reset: 0x7fffffffffffff Exists: Always
8	Enable_SLVIF_UndefinedReg_ DEC_ERR_IntStat	R/W	Slave Interface Undefined register Decode Error Interrupt Status enable Bit. This bit is used to enable the corresponding channel interrupt status bit (SLVIF_UndefinedReg_DEC_ERR_IntStat in DMAC_CommonReg_IntStatusReg. Values: ■ 0x1 (ENABLE_SLVIF_UndefinedReg_DEC_ERR): SLVIF_UndefinedReg_DEC_ERR_IntStat bit in DMAC_CommonReg_IntStatusReg is enabled. ■ 0x0 (DISABLE_SLVIF_UndefinedReg_DEC_ERR): SLVIF_UndefinedReg_DEC_ERR_IntStat bit in DMAC_CommonReg_IntStatusReg is disabled. Value After Reset: 0x1 Exists: Always
7:4	RSVD_DMAC_COMMONREG_ INTSTATUS_ENABLEREG_7to4	R	DMAC Common Register Interrupt Status Enable Register (bits 7 to 4) Reserved bits - Read Only Value After Reset: 0xf Exists: Always
3	Enable_SLVIF_CommonReg_Wr OnHold_ERR_IntStat	R/W	Slave Interface Common Register Write On Hold Error Interrupt Status Enable Bit.

Bits	Name	Access	Description
			This bit is used to enable the corresponding channel interrupt status bit (SLVIF_CommonReg_WrOnHold_ERR_IntStat in DMAC_CommonReg_IntStatusReg. Values: ■ 0x1 (ENABLE_SLVIF_CommonReg_WrOnHold_ERR): SLVIF_CommonReg_WrOnHold_ERR_IntStat bit in DMAC_CommonReg_IntStatusReg is enabled. ■ 0x0 (DISABLE_SLVIF_CommonReg_WrOnHold_ERR): SLVIF_CommonReg_WrOnHold_ERR_IntStat bit in DMAC_CommonReg_IntStatusReg is disabled. Value After Reset: 0x1 Exists: Always
2	Enable_SLVIF_CommonReg_RD2WO_ERR_IntStat	R/W	Slave Interface Common Register Read to Write only Error Interrupt Status Enable Bit. This bit is used to enable the corresponding channel interrupt status bit (SLVIF_CommonReg_RD2WO_ERR_IntStat in DMAC_CommonReg_IntStatusReg. Values: ■ 0x1 (ENABLE_SLVIF_CommonReg_RD2WO_ERR): SLVIF_CommonReg_RD2WO_ERR_IntStat bit in DMAC_CommonReg_IntStatusReg is enabled. ■ 0x0 (DISABLE_SLVIF_CommonReg_RD2WO_ERR): SLVIF_CommonReg_RD2WO_ERR_IntStat bit in DMAC_CommonReg_IntStatusReg is disabled. Value After Reset: 0x1 Exists: Always
1	Enable_SLVIF_CommonReg_WR2RO_ERR_IntStat	R/W	Slave Interface Common Register Write to Read only Error Interrupt Status Enable Bit. This bit is used to enable the corresponding channel interrupt status bit (SLVIF_CommonReg_WR2RO_ERR_IntStat in DMAC_CommonReg_IntStatusReg. Values: ■ 0x1 (ENABLE_SLVIF_CommonReg_WR2RO_ERR): SLVIF_CommonReg_WR2RO_ERR_IntStat bit in DMAC_CommonReg_IntStatusReg is enabled. ■ 0x0 (DISABLE_SLVIF_CommonReg_WR2RO_ERR): SLVIF_CommonReg_WR2RO_ERR_IntStat bit in

Bits	Name	Access	Description
			DMAC_CommonReg_IntStatusReg is disabled. Value After Reset: 0x1 Exists: Always
0	Enable_SLVIF_CommonReg_DEC_ERR_IntStat	R/W	Slave Interface Common Register Decode Error Interrupt Status Enable Bit. This bit is used to enable the corresponding channel interrupt status bit (SLVIF_CommonReg_DEC_ERR_IntStat in DMAC_CommonReg_IntStatusReg. Values: ■ 0x1 (ENABLE_SLVIF_CommonReg_DEC_ERR): SLVIF_CommonReg_DEC_ERR_IntStat bit in DMAC_CommonReg_IntStatusReg is Enabled. ■ 0x0 (DISABLE_SLVIF_CommonReg_DEC_ERR): SLVIF_CommonReg_DEC_ERR_IntStat bit in DMAC_CommonReg_IntStatusReg is disabled. Value After Reset: 0x1 Exists: Always

14.5.1.8 DMAC_COMMONREG_INTSIGNAL_ENABLEREG

- Description: Writing 1 to specific field will propagate the corresponding interrupt status in DMAC Common register Interrupt Status Register (DMAC_CommonReg_IntStatusReg) to generate a port level interrupt.
- Size: 64 bits
- Offset: 0x48
- Exists: Always

Figure & Table 14-15 Fields for register: DMAC_COMMONREG_INTSIGNAL_ENABLEREG

Bits	Name	Access	Description
63:9	RSVD_DMAC_COMMONREG_INTSIGNAL_ENABLEREG_63to9	R	DMAC Common Register Interrupt Signal Enable Register (bits 63 to 9) Reserved bits - Read Only Value After Reset: 0x7fffffffffffff Exists: Always
8	Enable_SLVIF_UndefinedReg_DEC_ERR_IntSignal	R/W	Slave Interface Undefined register Decode Error Interrupt Signal Enable Bit. This bit is used to enable the propagation of corresponding channel interrupt status bit (SLVIF_UndefinedReg_DEC_ERR_IntStat in DMAC_CommonReg_IntStatusReg) to generate a port

Bits	Name	Access	Description
			level interrupt. Values: ■ 0x1(ENABLE_SLVIF_UndefinedReg_DEC_ERR_IntSignal): SLVIF_UndefinedReg_DEC_ERR_IntStat signal in DMAC_CommonReg_IntStatusReg is enabled at port level. ■ 0x0(DISABLE_SLVIF_UndefinedReg_DEC_ERR_IntSignal): SLVIF_UndefinedReg_DEC_ERR_IntStat signal in DMAC_CommonReg_IntStatusReg is disabled at portlevel. Value After Reset: 0x1 Exists: Always
7:4	RSVD_DMAC_COMMONREG_INTSIGNAL_ENABLEREG_7to4	R	DMAC Common Register Interrupt Signal Enable Register (bits 7 to 4) Reserved bits - Read Only Value After Reset: 0xf Exists: Always
3	Enable_SLVIF_CommonReg_WrOnHold_ERR_IntSignal	R/W	Slave Interface Common Register Write On Hold Error Interrupt Signal Enable Bit. This bit is used to enable the propagation of corresponding channel interrupt status bit (SLVIF_CommonReg_WrOnHold_ERR_IntStat in DMAC_CommonReg_IntStatusReg) to generate a port level interrupt. Values: ■ 0x1 (ENABLE_SLVIF_CommonReg_WrOnHold_ERR_IntSignal): SLVIF_CommonReg_WrOnHold_ERR_IntStat signal in DMAC_CommonReg_IntStatusReg is enabled at port level. ■ 0x0 (DISABLE_SLVIF_CommonReg_WrOnHold_ERR_IntSignal): SLVIF_CommonReg_WrOnHold_ERR_IntStat signal in DMAC_CommonReg_IntStatusReg is disabled at port level. Value After Reset: 0x1 Exists: Always
2	Enable_SLVIF_CommonReg_RD2WO_ERR_IntSignal	R/W	Slave Interface Common Register Read to Write only Error Interrupt Signal Enable Bit. This bit is used to enable the propagation of corresponding channel interrupt status bit (SLVIF_CommonReg_RD2WO_ERR_IntStat in DMAC_CommonReg_IntStatusReg) to generate a port

Bits	Name	Access	Description
			level interrupt. Values: ■ 0x1(ENABLE_SLVIF_CommonReg_RD2WO_ERR_IntSignal): SLVIF_CommonReg_RD2WO_ERR_IntStat signal in DMAC_CommonReg_IntStatusReg is enabled at port level. ■ 0x0(DISABLE_SLVIF_CommonReg_RD2WO_ERR_IntSignal):SLVIF_CommonReg_RD2WO_ERR_IntStat signal in DMAC_CommonReg_IntStatusReg is disabled at port level. Value After Reset: 0x1 Exists: Always
1	Enable_SLVIF_CommonReg_WR2RO_ERR_IntSignal	R/W	Slave Interface Common Register Write to Read only Error Interrupt Signal Enable Bit. This bit is used to enable the propagation of corresponding channel interrupt status bit (SLVIF_CommonReg_WR2RO_ERR_IntStat in DMAC_CommonReg_IntStatusReg) to generate a port level interrupt. Values: ■ 0x1(ENABLE_SLVIF_CommonReg_WR2RO_ERR_IntSignal): SLVIF_CommonReg_WR2RO_ERR_IntStat signal in DMAC_CommonReg_IntStatusReg is enabled at port level. ■ 0x0(DISABLE_SLVIF_CommonReg_WR2RO_ERR_IntSignal): SLVIF_CommonReg_WR2RO_ERR_IntStat signal in DMAC_CommonReg_IntStatusReg is disabled at port level. Value After Reset: 0x1 Exists: Always
0	Enable_SLVIF_CommonReg_DEC_ERR_IntSignal	R/W	Slave Interface Common Register Decode Error Interrupt Signal Enable Bit. This bit is used to enable the propagation of corresponding channel interrupt status bit (SLVIF_CommonReg_DEC_ERR_IntStat in DMAC_CommonReg_IntStatusReg) to generate a port level interrupt. Values: ■ 0x1 (ENABLE_SLVIF_CommonReg_DEC_ERR_IntSignal): SLVIF_CommonReg_DEC_ERR_IntStat signal in

Bits	Name	Access	Description
			DMAC_CommonReg_IntStatusReg is enabled at port level. ■ 0x0 (DISABLE_SLVIF_CommonReg_DEC_ERR_IntSignal): SLVIF_CommonReg_DEC_ERR_IntStat signal in DMAC_CommonReg_IntStatusReg is disabled at port level. Value After Reset: 0x1 Exists: Always

14.5.1.9 DMAC_COMMONREG_INTSTATUSREG

- Description: This Register captures Slave interface access errors.
  - Decode Error
  - Write to read only register
  - Read to write only register
  - Write on hold
  - Undefined address
- Size: 64 bits
- Offset: 0x50
- Exists: Always

Figure & Table 14-16 Fields for register: DMAC_COMMONREG_INTSTATUSREG

Bits	Name	Access	Description
63:9	RSVD_DMAC_COMMONREG_INTSTATUSREG_63to9	R	DMAC Common Register Interrupt Signal Enable Register (bits 63 to 9) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always Volatile: true
8	SLVIF_UndefinedReg_DEC_ERR_IntStat	R	Slave Interface Undefined register Decode Error Interrupt Signal Enable Bit. Decode Error generated by DW_axi_dmac during register access. This error occurs if the register access is to undefined address range (>0x8FF if 8 channels are configured, >0x4FF if 4 channels are configured etc.) resulting in error response by DW_axi_dmac slave interface. ■ 0: No Slave Interface Decode Errors. ■ 1: Slave Interface Decode Error detected. Error Interrupt Status is generated if the corresponding

Bits	Name	Access	Description
			Status Enable bit in DMAC_CommonReg_IntStatus_Enable register bit is set to 1. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in DMAC_COMMONREG_INTCLEARREG on enabling the channel (required when the interrupt is not enabled). Values: ■ 0x1 (Active_UndefinedReg_DEC_ERR): Slave Interface Decode Error detected. ■ 0x0 (Inactive_UndefinedReg_DEC_ERR): No Slave Interface Decode Errors. Value After Reset: 0x0 Exists: Always Volatile: True
7:4	RSVD_DMAC_COMMONREG_INTSTATUSREG_7to4	R	DMAC Common Register Interrupt Status Register (bits 7 to 4) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always Volatile: True
3	SLVIF_CommonReg_WrOnHold_ERR_IntStat	R	Slave Interface Common Register Write On Hold Error Interrupt Status Bit. This error occurs if an illegal write operation is performed on a common register; this happens if a write operation is performed on a common register except DMAC_RESETREG with DMAC_RST field set to 1 when DW_axi_dmac is in Hold mode. ■ 0: No Slave Interface Common Register Write On Hold Errors; ■ 1: Slave Interface Common Register Write On Hold Error detected. Error Interrupt Status is generated if the corresponding Status Enable bit in DMAC_CommonReg_IntStatus_Enable register bit is set to 1. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in DMAC_COMMONREG_INTCLEARREG on enabling the channel (required when the interrupt is not enabled). Values: ■ 0x1 (Active_CommonReg_WrOnHold_ERR): Slave Interface Common Register Write On Hold Error

Bits	Name	Access	Description
			detected. ■ 0x0 (Inactive_CommonReg_WrOnHold_ERR): No Slave Interface Common Register Write On Hold Errors. Value After Reset: 0x0 Exists: Always Volatile: True
2	SLVIF_CommonReg_RD2WO_ERR_IntStat	R	Slave Interface Common Register Read to Write only Error Interrupt Status bit. This error occurs if Read operation is performed to a Write Only register in the common register space (0x000 to 0x0FF). ■ 0: No Slave Interface Read to Write Only Errors. ■ 1: Slave Interface Read to Write Only Error detected. Error Interrupt status is generated if the corresponding Status Enable bit in DMAC_CommonReg_IntStatus_Enable register bit is set to 1. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in DMAC_COMMONREG_INTCLEARREG on enabling the channel (required when the interrupt is not enabled). Values: ■ 0x1 (Active_CommonReg_RD2WO_ERR): Slave Interface Read to Write Only Error detected. ■ 0x0 (Inactive_CommonReg_RD2WO_ERR): No Slave Interface Read to Write Only Errors. Value After Reset: 0x0 Exists: Always Volatile: True
1	SLVIF_CommonReg_WR2RO_ERR_IntStat	R	Slave Interface Common Register Write to Read Only Error Interrupt Status bit. This error occurs if write operation is performed to a Read Only register in the common register space (0x000 to 0x0FF). ■ 0: No Slave Interface Write to Read Only Errors. ■ 1: Slave Interface Write to Read Only Error detected. Error Interrupt status is generated if the corresponding Status Enable bit in

Bits	Name	Access	Description
			DMAC_CommonReg_IntStatus_Enable register bit is set to 1. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in DMAC_COMMONREG_INTCLEARREG on enabling the channel (required when the interrupt is not enabled). Values: ■ 0x1 (Active_CommonReg_WR2RO_ERR): No Slave Interface Write to Read Only Errors. ■ 0x0 (Inactive_CommonReg_WR2RO_ERR): Slave Interface Write to Read Only Error detected. Value After Reset: 0x0 Exists: Always Volatile: True
0	SLVIF_CommonReg_DEC_ERR_IntStat	R	Slave Interface Common Register Decode Error Interrupt Status Bit. Decode Error generated by DW_axi_dmac during register access. This error occurs if the register access is to an invalid address in the common register space (0x000 to 0x0FF) resulting in error response by DW_axi_dmac slave interface. ■ 0: No Slave Interface Decode Errors. ■ 1: Slave Interface Decode Error detected. The Error Interrupt status is generated if the corresponding Status Enable bit in DMAC_CommonReg_IntStatus_Enable register bit is set to 1. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in DMAC_COMMONREG_INTCLEARREG on enabling the channel (required when the interrupt is not enabled). Values: ■ 0x1 (Active_CommonReg_DEC_ERR): Slave Interface Decode Error detected. ■ 0x0 (Inactive_CommonReg_DEC_ERR): No Slave Interface Decode Errors. Value After Reset: 0x0 Exists: Always Volatile: True

14.5.1.10 DMAC_RESETREG

- Description: This register is used to initiate the Software Reset to DW_axi_dmac.

- Size: 64 bits
- Offset: 0x58
- Exists: Always

Figure & Table 14-17 Fields for register: DMAC_RESETREG

Bits	Name	Access	Description
63:1	RSVD_DMAC_ResetReg_1to63	R	DMAC_ResetReg (bits 1 to 63) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always Volatile: True
0	DMAC_RST	R/W	DMAC Reset Request bit. Software writes 1 to this bit to reset the DW_axi_dmac and polls this bit to see it as 0. DW_axi_dmac resets all the modules except the slave bus interface module and clears this bit to 0. NOTE: Software is not allowed to write 0 to this bit. Value After Reset: 0x0 Exists: Always Volatile: True

14.5.1.11 DMAC_LOWPOWER_CFGREG

- Description: This register contains the fields that configures the Context Sensitive Low Power feature. This register should be programmed prior to enabling the channel.
- Size: 64 bits
- Offset: 0x60
- Exists: Always

Figure & Table 14-18 Fields for register: DMAC_LOWPOWER_CFGREG

Bits	Name	Access	Description
63:56	RSVD_DMAC_LOWPOWER_CFGREG_63to56	R	DMAC_LOWPOWER_CFGREG (bits 56 to 63) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always Volatile: True
55:48	MXIF_LPDLY	R/W	Defines the load value to be programmed into the AXI Master Interface low power delay counter. The programmed value must be greater than or equal to 0x4. If value programmed is less than 0x4, then the register value is reset to DMAX_MXIF_LPDLY. The maximum value programmed into this register field is

Bits	Name	Access	Description
			limited to (2**DMAX_MXIF_LPDLY_WIDTH)-1, otherwise the upper bits (8-DMAX_MXIF_LPDLY_WIDTH) of this field is reset to 0x0. Value After Reset: 0x0 Exists: Always Volatile: True
47:40	SBIU_LPDLY	R/W	Defines the load value to be programmed into the SBIU low power delay counter. The programmed value must be greater than or equal to 0x4. If value programmed is less than 0x4, then the register value is reset to DMAX_SBIU_LPDLY. The maximum value programmed into this register field is limited to (2**DMAX_SBIU_LPDLY_WIDTH)-1, otherwise the upper bits (8-DMAX_SBIU_LPDLY_WIDTH) of this field is reset to 0x0. Value After Reset: 0x0 Exists: Always Volatile: True
39:32	GLCH_LPDLY	R/W	Defines the load value to be programmed into the Global and DMA Channel low power delay counter. The programmed value must be greater than or equal to 0x4. If value programmed is less than 0x4, then the register value is reset to DMAX_GLCH_LPDLY. The maximum value programmed into this register field is limited to (2**DMAX_GLCH_LPDLY_WIDTH)-1, otherwise the upper bits (8-DMAX_GLCH_LPDLY_WIDTH) of this field is reset to 0x0. Value After Reset: 0x0 Exists: Always Volatile: True
31:4	RSVD_DMAC_LOWPOWER_CFGREG_31to4	R	DMAC_LOWPOWER_CFGREG (bits 4to31) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always Volatile: True
3	MXIF_CSLP_EN	R/W	AXI Master Interface Context Sensitive Low Power feature enable. Values: ■ 0x0 (MXIF_CSLP_DISABLE): AXI Master Interface

Bits	Name	Access	Description
			Context Sensitive Low Power feature is disabled. ■ 0x1 (MXIF_CSLP_ENABLE): AXI Master Interface Context Sensitive Low Power feature is enabled. Value After Reset: 0x0 Exists: Always Volatile: True
2	SBIU_CSLP_EN	R/W	SBIU Context Sensitive Low Power feature enable. Values: ■ 0x0 (SBIU_CSLP_DISABLE): SBIU Context Sensitive Low Power feature is disabled. ■ 0x1 (SBIU_CSLP_ENABLE): SBIU Context Sensitive Low Power feature is enabled. Value After Reset: 0x0 Exists: Always Volatile: True
1	CHNL_CSLP_EN	R/W	DMA Channel Context Sensitive Low Power feature enable. Values: ■ 0x0 (CHNL_CSLP_DISABLE): DMA Channel Context Sensitive Low Power feature is disabled. ■ 0x1 (CHNL_CSLP_ENABLE): DMA Channel Context Sensitive Low Power feature is enabled. Value After Reset: 0x0 Exists: Always Volatile: True
0	GBL_CSLP_EN	R/W	Global Context Sensitive Low Power feature enable. Values: ■ 0x0 (GBL_CSLP_DISABLE): Global Context Sensitive Low Power feature is disabled. ■ 0x1 (GBL_CSLP_ENABLE): Global Context Sensitive Low Power feature is enabled. Value After Reset: 0x0 Exists: Always Volatile: True

14.5.2 DW_axi_dmac_mem_map/Channelx_Registers_Address_Block Registers

14.5.2.1 CHx_SAR (for x = 1; x <= 4)

- Description: The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current AXI transfer.
- Size: 64 bits
- Offset: 0x100 + (x-1)*0x100
- Exists: Yes

Figure & Table 14-19 Fields for register: CHx_SAR (for x = 1; x <= 4)

Bits	Name	Access	Description
63:0	SAR	R/W	Current Source Address of DMA transfer. Updated after each source transfer. The SINC fields in the CHx_CTL register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. Value After Reset: 0x0 Exists: Always Volatile: True

14.5.2.2 CHx_DAR (for x = 1; x <= 4)

- Description: The starting destination address is programmed by the software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current AXI transfer.
- Size: 64 bits
- Offset: 0x108 + (x-1)*0x100
- Exists: Yes

Figure & Table 14-20 Fields for register: CHx_DAR (for x = 1; x <= 4)

Bits	Name	Access	Description
63:0	DAR	R/W	Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC fields in the CHx_CTL register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. Value After Reset: 0x0 Exists: Always

Bits	Name	Access	Description
			Volatile: True

14.5.2.3 CHx_BLOCK_TS (for x = 1; x <= 4)

- Description: When DW_axi_dmac is the flow controller, the DMAC uses this register before the channel is enabled for block-size.
- Size: 64 bits
- Offset: 0x110 + (x-1)*0x100
- Exists: Yes

Figure & Table 14-21 Fields for register: CHx_BLOCK_TS (for x = 1; x <= 4)

Bits	Name	Access	Description
63:22	RSVD_DMAC_CHx_BLOCK_TS REG_63to22	R	DMAC Channelx Block Transfer Size Register (bits 63 to 22) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always Volatile: True
21:0	BLOCK_TS	R/W	Block Transfer Size. The number programmed into BLOCK_TS field indicates the total number of data of width CHx_CTL.SRC_TR_WIDTH to be transferred in a DMA block transfer. Block Transfer Size = BLOCK_TS+1 When the transfer starts, the read-back value is the total number of data items already read from the source peripheral, regardless of who is the flow controller. When the source or destination peripheral is assigned as the flow controller, the value before the transfer starts saturates at DMAX_CHx_MAX_BLK_SIZE, but the actual block size can be greater. Value After Reset: 0x0 Exists: Always Volatile: True

14.5.2.4 CHx_CTL (for x = 1; x <= 4)

- Description: This register contains fields that control the DMA transfer. This register should be programmed prior to enabling the channel except for LLI-based multi-block transfer. When LLIbased multi-block transfer is enabled, the CHx_CTL register is loaded from the corresponding location of the LLI and it can be varied on a block-by-block basis within a DMA

transfer. The software is not allowed to directly update this register through DW_axi_dmac slave interface. Any write to this register during LLI based multi-block transfer is ignored.

- Size: 64 bits
- Offset: 0x118 + (x-1)*0x100
- Exists: Yes

Figure & Table 14-22 Fields for register: CHx_CTL (for x = 1; x <= 4)

Bits	Name	Access	Description
63	SHADOWREG_OR_LLI_VALID	R/W	Shadow Register content/Linked List Item valid. Indicates whether the content of shadow register or the linked list item fetched from the memory is valid. ■ 0: Shadow Register content/LLI is invalid. ■ 1: Last Shadow Register/LLI is valid. LLI based multi-block transfer: The CHx_CTL register is loaded from the LLI. Hence, the software is not allowed to directly update this register through the DW_axi_dmac slave interface. This field can be used to dynamically extend the LLI by the software. On noticing this bit as 0, DW_axi_dmac discards the LLI and generates the ShadowReg_Or_LII_Invalid_ERR Interrupt if the corresponding channel error interrupt mask bit is set to 0. In the case of LLI pre-fetching, the ShadowReg_Or_LLI_Invalid_ERR interrupt is not generated even if the ShadowReg_Or_LLI_Valid bit is seen to be 0 for the pre-fetched LLI. In this case, DW_axi_dmac attempts the LLI fetch operation again after completing the current block transfer and generates the ShadowReg_Or_LII_Invalid_ERR interrupt only if ShadowReg_Or_LII_Valid bit is still seen to be 0. This error condition causes the DW_axi_dmac to halt the corresponding channel gracefully. DW_axi_dmac waits until software writes (any value) to CHx_BLK_TFR_ResumeReqReg to indicate valid LLI availability before attempting another LLI read operation. This bit is cleared to 0 and written back to the corresponding LLI location after block transfer completion when LLI writeback option is enabled. Hence, for LLI-based multi-block transfers, the software might manipulate/redefine any descriptor with the ShadowReg_Or_LII_Valid bit set to 0 if LLI write-back option is enabled.

Bits	Name	Access	Description
			Shadow Reg based multi-block transfer: On noticing this bit as 0 during shadow register fetch phase, DW_axi_dmac discards the Shadow Register contents and generates ShadowReg_Or_LLI_Invlid_ERR Interrupt. In this case, the software has to write (any value) to CHx_BLK_TFR_ResumeReqReg after updating the shadow registers and after setting ShadowReg_Or_LLI_Valid bit to 1 to indicate to DW_axi_dmac that shadow register contents are valid and the next block transfer can be resumed. DW_axi_dmac clears this bit to 0 after copying the shadow register contents. Software can reprogram the shadow registers only if ShadowReg_Or_LLI_Valid bit is 0. Software needs to read this register in block completion interrupt service routine (if interrupt is enabled)/continuously poll this register (if interrupt is not enabled) to make sure that this bit is 0 before updating the shadow registers. If shadow-register-based multi-block transfer is enabled and software attempts to write to the shadow register when ShadowReg_Or_LLI_Valid bit is 1, DW_axi_dmac generates SLVIF_ShadowReg_WrOnValid_ERR interrupt. Values: ■ 0x1 (VALID): Indicates shadowreg/LLI content is Valid. ■ 0x0 (INVALID): Indicates shadowreg/LLI content is Invalid. Value After Reset: 0x0 Exists: Always Volatile: True
62	SHADOWREG_OR_LLI_LAST	R/W	Last Shadow Register/Linked List Item. Indicates whether shadow register content or the linked list item fetched from the memory is the last one or not. ■ 0: Not last Shadow Register/LLI. ■ 1: Last Shadow Register/LLI. LLI based multi-block transfer: DW_axi_dmac uses this bit to decide if another LLI fetch is needed in the current DMA transfer. If this bit is 0, DW_axi_dmac fetches the next LLI from the address pointed out by LLP field in the current LLI.

Bits	Name	Access	Description
			If this bit is 1, DW_axi_dmac understands that current block is the final block in the dma transfer and ends the dma transfer once the AMBA transfer corresponding to the current block completes. Shadow Reg based multi-block transfer: DW_axi_dmac uses this bit to decide if another Shadow Register fetch is needed in the current DMA transfer. If this bit is 0, DW_axi_dmac understands that there are one or more blocks to be transferred in the current block and hence one or more shadow register set contents will be valid and needs to be fetched. If this bit is 1, DW_axi_dmac understands that current block is the final block in the dma transfer and ends the dma transfer once the AMBA transfer corresponding to the current block completes. Values: ■ 0x1 (LAST_ITEM): Indicates shadowreg/LLI content is the last one. ■ 0x0 (NOT_LAST_ITEM): Indicates shadowreg/LLI content is not the last one. Value After Reset: 0x0 Exists: Always Volatile: True
61:59	RSVD_DMAC_CHx_CTL_59to61	R	DMAC Channelx Control Transfer Register (bits 59 to 61) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
58	IOC_BlkTfr	R/W	Interrupt On completion of Block Transfer. This bit is used to control the block transfer completion interrupt generation on a block by block basis for shadow register or linked list based multi-block transfers. Writing 1 to this register field enables CHx_IntStatusReg.BLOCK_TFR_DONE_IntStat field if this interrupt generation is enabled in CHx_IntStatus_EnableReg register and the external interrupt output is is asserted if this interrupt generation is enabled in CHx_IntSignal_EnableReg register. Note: If a linked-list or shadow-register-based multi-block transfer is not used for both source and destination (for instance if source and destination use

Bits	Name	Access	Description
			contiguous address or auto-reload-based multi-block transfer), the value of this field cannot be modified per block. Additionally, the value programmed before the channel is enabled is used for all the blocks in the DMA transfer. Values: ■ 0x1 (Enable_BLKTFR_INTR): Enables CHx_IntStatusReg.BLOCK_TFR_DONE_IntStat field. ■ 0x0 (DISABLE_BLKTFR_INTR): Disables CHx_IntStatusReg.BLOCK_TFR_DONE_IntStat field. Value After Reset: 0x0 Exists: Always
57	DST_STAT_EN	R	Destination Status Enable. Enable the logic to fetch status from destination peripheral of channel x pointed to by the content of CHx_DSTATAR register and stores it in CHx_DSTAT register. This value is written back to the CHx_DSTAT location of linked list at end of each block transfer if DMAX_CHx_LLI_WB_EN is set to 1 and if linked list based multi-block transfer is used by either source or destination peripheral. Values: ■ 0x1 (Enable_STAT_FETCH): Enables status fetch for Destination and store the value in CH1_DSTAT register. ■ 0x0 (NO_STAT_FETCH): No status fetch for Destination device. Value After Reset: 0x0 Exists: Always
56	SRC_STAT_EN	R	Source Status Enable. Enable the logic to fetch status from source peripheral of channel x pointed to by the content of CHx_SSTATAR register and stores it in CHx_SSTAT register. This value is written back to the CHx_SSTAT location of linked list at end of each block transfer if DMAX_CHx_LLI_WB_EN is set to 1 and if linked list based multi-block transfer is used by either source or destination peripheral. Values: ■ 0x1 (Enable_STAT_FETCH): Enables status fetch for Source and store the value in CH1_SSTAT register. ■ 0x0 (NO_STAT_FETCH): No status fetch for Source

Bits	Name	Access	Description
			device. Value After Reset: 0x0 Exists: Always
55:48	AWLEN	R/W	Destination Burst Length. AXI Burst length used for destination data transfer. The specified burst length is used for destination data transfer till the extent possible; remaining transfers use maximum possible value that is less than or equal to DMAX_CHx_MAX_AMBA_BURST_LENGTH. The maximum value of AWLEN is limited by DMAX_CHx_MAX_AMBA_BURST_LENGTH. Note: The AWLEN setting may not be honored towards endto-block transfers, the end of a transaction (only applicable to non-memory peripherals), and during 4K boundary crossings. Value After Reset: 0x0 Exists: Always
47	AWLEN_EN	R/W	Destination Burst Length Enable. If this bit is set to 1, DW_axi_dmac uses the value of CHx_CTL.AWLEN as AXI Burst length for destination data transfer till the extent possible; remaining transfers use maximum possible burst length. If this bit is set to 0, DW_axi_dmac uses any possible value which is less than or equal to DMAX_CHx_MAX_AMBA_BURST_LENGTH as AXI Burst length for destination data transfer. Values: ■ 0x1 (Enable): AXI Burst Length is CH1_CTL.AWLEN (till the extent possible) for Destination data transfers. ■ 0x0 (Disable): AXI Burst Length is any possible value <= DMAX_CH1_MAX_AMBA_BURST_LENGTH for Destination data transfers. Value After Reset: 0x0 Exists: Always
46:39	ARLEN	R/W	Source Burst Length. AXI Burst length used for source data transfer. The specified burst length is used for source data transfer till the extent possible; remaining transfers use maximum possible value that is less than or equal to

Bits	Name	Access	Description
			DMAX_CHx_MAX_AMBA_BURST_LENGTH. The maximum value of ARLEN is limited by DMAX_CHx_MAX_AMBA_BURST_LENGTH. Value After Reset: 0x0 Exists: Always
38	ARLEN_EN	R/W	Source Burst Length Enable. If this bit is set to 1, DW_axi_dmac uses the value of CHx_CTL.ARLEN as AXI Burst length for source data transfer till the extent possible; remaining transfers use maximum possible burst length. If this bit is set to 0, DW_axi_dmac uses any possible value that is less than or equal to DMAX_CHx_MAX_AMBA_BURST_LENGTH as AXI Burst length for source data transfer. Values: ■ 0x1 (Enable): AXI Burst Length is CH1_CTL.ARLEN (till the extent possible) for Source data transfers. ■ 0x0 (Disable): AXI Burst Length is any possible value <= DMAX_CH1_MAX_AMBA_BURST_LENGTH for Source data transfers. Value After Reset: 0x0 Exists: Always
37:35	AW_PROT	R/W	AXI 'aw_prot' signal Value After Reset: 0x0 Exists: Always
34:32	AR_PROT	R/W	AXI 'ar_prot' signal Value After Reset: 0x0 Exists: Always
31	RSVD_DMAC_CHx_CTL_31	R	DMAC Channelx Control Transfer Register bit31 Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
30	NonPosted_LastWrite_En	R/W	Non Posted Last Write Enable. This bit decides whether posted writes can be used throughout the block transfer. ■ 0: Posted writes may be used throughout the block transfer. ■ 1: Posted writes may be used till the end of the

Bits	Name	Access	Description
			block (inside a block) and the last write in the block must be non-posted. This is to synchronize block completion interrupt generation to the last write data reaching the end memory/peripheral. Values: ■ 0x1 (Enable): Last write in the block must be non-posted. ■ 0x0 (Disable): Posted writes may be used throughout the block transfer. Value After Reset: 0x0 Exists: Always
29:26	AW_CACHE	R/W	AXI 'aw_cache' signal Value After Reset: 0x0 Exists: Always
25:22	AR_CACHE	R/W	AXI 'ar_cache' signal Value After Reset: 0x0 Exists: Always
21:18	DST_MSIZE	R/W	Destination Burst Transaction Length. Number of data items, each of width CHx_CTL.DST_TR_WIDTH, to be written to the destination every time a destination burst transaction request is made from the corresponding hardware or software handshaking interface. Note: This Value is not related to the AXI awlen signal. Values: ■ 0x0 (DATA_ITEM_1): 1 Data Item read from Destination in the burst transaction. ■ 0x1 (DATA_ITEMS_4): 4 Data Item read from Destination in the burst transaction. ■ 0x2 (DATA_ITEMS_8): 8 Data Item read from Destination in the burst transaction. ■ 0x3 (DATA_ITEMS_16): 16 Data Item read from Destination in the burst transaction. ■ 0x4 (DATA_ITEMS_32): 32 Data Item read from Destination in the burst transaction. ■ 0x5 (DATA_ITEMS_64): 64 Data Item read from Destination in the burst transaction. ■ 0x6 (DATA_ITEMS_128): 128 Data Item read from Destination in the burst transaction.

Bits	Name	Access	Description
			■ 0x7 (DATA_ITEMS_256): 256 Data Item read from Destination in the burst transaction. ■ 0x8 (DATA_ITEMS_512): 512 Data Item read from Destination in the burst transaction. ■ 0x9 (DATA_ITEMS_1024): 1024 Data Item read from Destination in the burst transaction. Value After Reset: 0x0 Exists: Always
17:14	SRC_MSIZE	R/W	Source Burst Transaction Length. Number of data items, each of width CHx_CTL.SRC_TR_WIDTH, to be read from the source every time a source burst transaction request is made from the corresponding hardware or software handshaking interface. The maximum value of DST_MSIZE is limited by DMAX_CHx_MAX_MSIZE. Note: This Value is not related to the AXI arlen signal. Values: ■ 0x0 (DATA_ITEM_1): 1 Data Item read from Source in the burst transaction. ■ 0x1 (DATA_ITEMS_4): 4 Data Item read from Source in the burst transaction. ■ 0x2 (DATA_ITEMS_8): 8 Data Item read from Source in the burst transaction. ■ 0x3 (DATA_ITEMS_16): 16 Data Item read from Source in the burst transaction. ■ 0x4 (DATA_ITEMS_32): 32 Data Item read from Source in the burst transaction. ■ 0x5 (DATA_ITEMS_64): 64 Data Item read from Source in the burst transaction. ■ 0x6 (DATA_ITEMS_128): 128 Data Item read from Source in the burst transaction. ■ 0x7 (DATA_ITEMS_256): 256 Data Item read from Source in the burst transaction. ■ 0x8 (DATA_ITEMS_512): 512 Data Item read from Source in the burst transaction. ■ 0x9 (DATA_ITEMS_1024): 1024 Data Item read from Source in the burst transaction. Value After Reset: 0x0 Exists: Always

Bits	Name	Access	Description
13:11	DST_TR_WIDTH	R/W	Destination Transfer Width. Mapped to AXI bus awsize, this value must be less than or equal to DMAX_M_DATA_WIDTH. Values: ■ 0x0 (BITS_8): Destination Transfer Width is 8 bits. ■ 0x1 (BITS_16): Destination Transfer Width is 16 bits. ■ 0x2 (BITS_32): Destination Transfer Width is 32 bits. ■ 0x3 (BITS_64): Destination Transfer Width is 64 bits. ■ 0x4 (BITS_128): Destination Transfer Width is 128 bits. ■ 0x5 (BITS_256): Destination Transfer Width is 256 bits. ■ 0x6 (BITS_512): Destination Transfer Width is 512 bits. Value After Reset: 2 Exists: Always
10:8	SRC_TR_WIDTH	R/W	Source Transfer Width. Mapped to AXI bus arsize, this value must be less than or equal to DMAX_M_DATA_WIDTH. Values: ■ 0x0 (BITS_8): Source Transfer Width is 8 bits. ■ 0x1 (BITS_16): Source Transfer Width is 16 bits. ■ 0x2 (BITS_32): Source Transfer Width is 32 bits. ■ 0x3 (BITS_64): Source Transfer Width is 64 bits. ■ 0x4 (BITS_128): Source Transfer Width is 128 bits. ■ 0x5 (BITS_256): Source Transfer Width is 256 bits. ■ 0x6 (BITS_512): Source Transfer Width is 512 bits. Value After Reset: 2 Exists: Always
7	RSVD_DMAC_CHx_CTL_7	R	DMAC Channelx Control Transfer Register bit7 Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
6	DINC	R/W	Destination Address Increment.

Bits	Name	Access	Description
			Indicates whether to increment the destination address on every destination transfer. If the device is writing data from a source peripheral FIFO with a fixed address, then set this field to 'No change'. ■ 0: Increment ■ 1: No Change NOTE: Increment aligns the address to the next CHx_CTL.DST_TR_WIDTH boundary. Values: ■ 0x0 (INCREMENTAL): Destination address incremented on every source transfer. ■ 0x1 (FIXED): Destination address is fixed. Value After Reset: 0x0 Exists: Always
5	RSVD_DMAC_CHx_CTL_5	R	DMAC Channelx Control Transfer Register bit5 Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
4	SINC	R/W	Source Address Increment. Indicates whether to increment the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to 'No change'. ■ 0: Increment; ■ 1: No Change. NOTE: Increment aligns the address to the next CHx_CTL.SRC_TR_WIDTH boundary. Values: ■ 0x0 (INCREMENTAL): Source address incremented on every source transfer. ■ 0x1 (FIXED): Source address is fixed. Value After Reset: 0x0 Exists: Always
3	RSVD_DMAC_CHx_CTL_3	R	DMAC Channelx Control Transfer Register bit3 Reserved bits - Read Only Value After Reset: 0x0 Exists: Always

Bits	Name	Access	Description
2	DMS	R	Destination Master Select. Identifies the Master Interface layer from which the destination device (peripheral or memory) is accessed. ■ 0: AXI master 1 ■ 1: AXI Master 2 Values: ■ 0x1 (MASTER2_INTF): Destination device on Master-2 interface layer. ■ 0x0 (MASTER1_INTF): Destination device on Master-1 interface layer. Value After Reset: 0 Exists: Always
1	RSVD_DMAC_CHx_CTL_1	R	DMAC Channelx Control Transfer Register bit1 Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
0	SMS	R	Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed. ■ 0: AXI master 1 ■ 1: AXI Master 2 Values: ■ 0x1 (MASTER2_INTF): Source device on Master-2 interface layer. ■ 0x0 (MASTER1_INTF): Source device on Master-1 interface layer. Value After Reset: 0 Exists: Always

14.5.2.5 CHx_CFG (for x = 1; x <= 4)

- Description: This register contains fields that configure the DMA transfer. This register should be programmed prior to enabling the channel. Bits [63:32] of the channel configuration register remains fixed for all blocks of a multi-block transfer and can be programmed only when channel is disabled. Bits [3:0] of the channel configuration register can be programmed even when channel is enabled. Software clears these bits to end the multi-block transfers. For Contiguous-Address and Auto- Reloading-based multi-block transfers (if neither source nor destination peripheral uses Shadow-Register or Linked-List-based multi-block transfers), if the

corresponding multi-block type selection bits namely CHx_CFG.SRC_MLTBLK_TYPE and/or CHx_CFG.DST_MLTBLK_TYPE bits are seen to be 2'b00 at the end of a block transfer, the DW_axi_dmac understands that the previous block was the final block in the transfer and completes the DMA transfer operation.

- Size: 64 bits
- Offset: 0x120 + (x-1)*0x100
- Exists: TEE DMA Only

Figure & Table 14-23 Fields for register: CHx_CFG (for x = 1; x <= 4)

Bits	Name	Access	Description
63	RSVD_DMAC_CHx_CFG_63	R	DMAC Channelx Transfer Configuration Register (63bit) Reserved bit - Read Only Value After Reset: 0x0 Exists: Always
62:59	DST_OSR_LMT	R/W	Destination Outstanding Request Limit. Maximum outstanding request supported is 16. Source Outstanding Request Limit = DST_OSR_LMT + 1 Value After Reset: 0x0 Exists: Always
58:55	SRC_OSR_LMT	R/W	Source Outstanding Request Limit. Maximum outstanding request supported is 16. Source Outstanding Request Limit = SRC_OSR_LMT + 1 Value After Reset: 0x0 Exists: Always
54:53	LOCK_CH_L	R	Channel Lock Level. This bit indicates the duration over which CHx_CFG.LOCK_CH bit applies. ■ 00: Over complete DMA transfer ■ 01: Over DMA block transfe ■ 1x: Reserved This field does not exist if the configuration parameter DMAX_CHx_LOCK_EN is set to False; in that case, the read-back value is always 0. Values: ■ 0x0 (DMA_transfer_CH_LOCK): Duration of the Channel locking is for the entire DMA transfer. ■ 0x1 (BLOCK_TRANFER_CH_LOCK): Duration of the Channel locking is for the current block transfer. Value After Reset: 0x0

Bits	Name	Access	Description
			Exists: Always
52	LOCK_CH	R	Channel Lock bit. When the channel is granted control of the master bus interface and if the CHx_CFG.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CHx_CFG.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CHx_CFG.LOCK_CH_L. This field does not exist if the configuration parameter DMAX_CHx_LOCK_EN is set to False; in this case, the read-back value is always 0. Locking the channel locks AXI Read Address, Write Address and Write Data channels on the corresponding master interface. Note: Channel locking feature is supported only for memory-to-memory transfer at Block Transfer and DMA Transfer levels. Hardware does not check for the validity of channel locking setting, hence the software must take care of enabling the channel locking only for memory-to-memory transfers at Block Transfer or DMA Transfer levels. Illegal programming of channel locking might result in unpredictable behavior. Values: ■ 0x0 (NO_CHANNEL_LOCK): Channel is not locked during the transfers. ■ 0x1 (CHANNEL_LOCK): Channel is locked and granted exclusive access to the Master Bus Interface. Value After Reset: 0x0 Exists: Always
51:49	CH_PRIOR	R/W	Channel Priority. A priority of DMAX_NUM_CHANNELS-1 is the highest priority, and 0 is the lowest. This field must be programmed within the following range: 0: 3 A programmed value outside this range will cause erroneous behavior. Value After Reset: 4 – x Exists: Always

Bits	Name	Access	Description
48	RSVD_DMAC_CHx_CFG_48	R	DMAC Channelx Transfer Configuration Register (48bit) Reserved bit - Read Only Value After Reset: 0x0 Exists: Always
47:44	RSVD_DMAC_CHx_CFG_47_44	R	DMAC Channelx Transfer Configuration Register (bits 44 to 47) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
43	RSVD_DMAC_CHx_CFG_43	R	DMAC Channelx Transfer Configuration Register (43bit) Reserved bit - Read Only Value After Reset: 0x0 Exists: Always
42:39	RSVD_DMAC_CHx_CFG_42_39	R	DMAC Channelx Transfer Configuration Register (bits 39 to 42) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
38	DST_HWHS_POL	R	Destination Hardware Handshaking Interface Polarity. 0: ACTIVE HIGH. 1: ACTIVE LOW. Values: ■ 0x0 (ACTIVE_HIGH): Polarity of the Handshaking Interface used for the Destination peripheral is Active High. ■ 0x1 (ACTIVE_LOW): Polarity of the Handshaking Interface used for the Destination peripheral is Active Low. Value After Reset: 0x0 Exists: Always
37	SRC_HWHS_POL	R	Source Hardware Handshaking Interface Polarity. 0: ACTIVE HIGH. 1: ACTIVE LOW. Values: ■ 0x0 (ACTIVE_HIGH): Polarity of the Handshaking Interface used for the Source peripheral is Active High. ■ 0x1 (ACTIVE_LOW): Polarity of the Handshaking

Bits	Name	Access	Description
			Interface used for the Source peripheral is Active Low. Value After Reset: 0x0 Exists: Always
36	HS_SEL_DST	R/W	Destination Software or Hardware Handshaking Select. This register selects which of the handshaking interfaces (hardware or software) is active for destination requests on this channel. ■ 0: Hardware handshaking interface. Software-initiated transaction requests are ignored. ■ 1: Software handshaking interface. Hardware-initiated transaction requests are ignored. If the destination peripheral is memory, then this bit is ignored. Values: ■ 0x0 (HARDWARE_HS): Hardware Handshaking Interface is used for the Destination peripheral. ■ 0x1 (SOFTWARE_HS): Software Handshaking Interface is used for the Destination peripheral. Value After Reset: 0x1 Exists: Always
35	HS_SEL_SRC	R/W	Source Software or Hardware Handshaking Select. This register selects which of the handshaking interfaces (hardware or software) is active for source requests on this channel. ■ 0: Hardware handshaking interface. Software-initiated transaction requests are ignored. ■ 1: Software handshaking interface. Hardware-initiated transaction requests are ignored. If the source peripheral is memory, then this bit is ignored. Values: ■ 0x0 (HARDWARE_HS): Hardware Handshaking Interface is used for the Source peripheral. ■ 0x1 (SOFTWARE_HS): Software Handshaking Interface is used for the Source peripheral. Value After Reset: 0x1 Exists: Always

Bits	Name	Access	Description
34:32	TT_FC	R/W	Transfer Type and Flow Control. The following transfer types are supported. ■ Memory to Memory ■ Memory to Peripheral ■ Peripheral to Memory ■ Peripheral to Peripheral Flow Control can be assigned to the DW_axi_dmac, the source peripheral, or hte destination peripheral. Values: ■ 0x0 (MEM_TO_MEM_DMAC): Transfer Type is memory to memory and Flow Controller is DW_axi_dmac. ■ 0x1 (MEM_TO_PER_DMAC): Transfer Type is memory to peripheral and Flow Controller is DW_axi_dmac. ■ 0x2 (PER_TO_MEM_DMAC): Transfer Type is peripheral to memory and Flow Controller is DW_axi_dmac. ■ 0x3 (PER_TO_PER_DMAC): Transfer Type is peripheral to peripheral and Flow Controller is DW_axi_dmac. ■ 0x4 (PER_TO_MEM_SRC): Transfer Type is peripheral to Memory and Flow Controller is Source peripheral. ■ 0x5 (PER_TO_PER_SRC): Transfer Type is peripheral to peripheral and Flow Controller is Source peripheral. ■ 0x6 (MEM_TO_PER_DST): Transfer Type is memory to peripheral and Flow Controller is Destination peripheral. ■ 0x7 (PER_TO_PER_DST): Transfer Type is peripheral to peripheral and Flow Controller is Destination peripheral. Value After Reset: 3 Exists: Always
31:4	RSVD_DMAC_CHx_CFG_4to31	R	DMAC Channelx Transfer Configuration Register (bits 4 to 31) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always

Bits	Name	Access	Description
3:2	DST_MULTBLK_TYPE	R/W	Destination Multi Block Transfer Type. These bits define the type of multi-block transfer used for destination peripheral. ■ 00: Contiguous ■ 01: Reload ■ 10: Shadow Register ■ 11: Linked List If the type selected is Contiguous, the CHx_DAR register is loaded with the value of the end source address of previous block + 1 at the end of every block for multi-block transfers. A new block transfer is then initiated. If the type selected is Reload, the CHx_DAR register is reloaded from the initial value of DAR at the end of every block for multi-block transfers. A new block transfer is then initiated. If the type selected is Shadow Register, the CHx_DAR register is loaded from the content of its shadow register if CHx_CTL.ShadowReg_Or_LLI_Valid bit is set to 1 at the end of every block for multi-block transfers. A new block transfer is then initiated. If the type selected is Linked List, the CHx_DAR register is loaded from the Linked List if CTL.ShadowReg_Or_LLI_Valid bit is set to 1 at the end of every block for multi-block transfers. A new block transfer is then initiated. CHx_CTL and CHx_BLOCK_TS registers are loaded from their initial values or from the contents of their shadow registers (if CHx_CTL.ShadowReg_Or_LLI_Valid bit is set to 1) or from the linked list (if CTL.ShadowReg_Or_LLI_Valid bit is set to 1) at the end of every block for multi-block transfers based on the multi-block transfer type programmed for source and destination peripherals. Contiguous transfer on both source and destination peripheral is not a valid multi-block transfer configuration. This field does not exist if the configuration parameter DMAX_CHx_MULTI_BLK_EN is not selected; in that case, the read-back value is always 0. Values: ■ 0x0 (CONTINGUOUS): Contiguous Multiblock Type

Bits	Name	Access	Description
			used for Destination Transfer. ■ 0x1 (RELOAD): Reload Multiblock Type used for Destination Transfer. ■ 0x2 (SHADOW_REGISTER): Shadow Register based Multiblock Type used for Destination Transfer. ■ 0x3 (LINKED_LIST): Linked List based Multiblock Type used for Destination Transfer. Value After Reset: 0 Exists: Always
1:0	SRC_MULTBLK_TYPE	R/W	Source Multi Block Transfer Type. These bits define the type of multi-block transfer used for source peripheral. ■ 00: Contiguous ■ 01: Reload ■ 10: Shadow Register ■ 11: Linked List If the type selected is Contiguous, the CHx_SAR register is loaded with the value of the end source address of previous block + 1 at the end of every block for multi-block transfers. A new block transfer is then initiated. If the type selected is Reload, the CHx_SAR register is reloaded from the initial value of SAR at the end of every block for multi-block transfers. A new block transfer is then initiated. If the type selected is Shadow Register, the CHx_SAR register is loaded from the content of its shadow register if CHx_CTL.ShadowReg_Or_LLI_Valid bit is set to 1 at the end of every block for multi-block transfers. A new block transfer is then initiated. If the type selected is Linked List, the CHx_SAR register is loaded from the Linked List if CTL.ShadowReg_Or_LLI_Valid bit is set to 1 at the end of every block for multi-block transfers. A new block transfer is then initiated. CHx_CTL and CHx_BLOCK_TS registers are loaded from their initial values or from the contents of their shadow registers (if CHx_CTL.ShadowReg_Or_LLI_Valid bit is set to 1) or from the linked list (if CTL.ShadowReg_Or_LLI_Valid bit is set to 1) at the end of every block for multi-block transfers based on the multi-block transfer type programmed for source and

Bits	Name	Access	Description
			destination peripherals. Contiguous transfer on both source and destination peripheral is not a valid multi-block transfer configuration. This field does not exist if the configuration parameter DMAX_CHx_MULTI_BLK_EN is not selected; in that case, the read-back value is always 0. Values: ■ 0x0 (CONTINGUOUS): Contiguous Multiblock Type used for Source Transfer. ■ 0x1 (RELOAD): Reload Multiblock Type used for Source Transfer. ■ 0x2 (SHADOW_REGISTER): Shadow Register based Multiblock Type used for Source Transfer. ■ 0x3 (LINKED_LIST): Linked List based Multiblock Type used for Source Transfer. Value After Reset: 0 Exists: Always

14.5.2.6 CHx_CFG2 (for x = 1; x <= 4)

- Description: This register contains fields that configure the DMA transfer. This register should be programmed prior to enabling the channel. Bits [63:32] of the channel configuration register remains fixed for all blocks of a multi-block transfer and can be programmed only when channel is disabled. Bits [3:0] of the channel configuration register can be programmed even when channel is enabled. Software clears these bits to end the multi-block transfers. For Contiguous-Address and Auto-Reloading-based multi-block transfers (if neither source nor destination peripheral uses Shadow-Register or Linked-List-based multi-block transfers), if the corresponding multi-block type selection bits namely CHx_CFG.SRC_MLTBLK_TYPE and/or CHx_CFG.DST_MLTBLK_TYPE bits are seen to be 2'b00 at the end of a block transfer, the DW_axi_dmac understands that the previous block was the final block in the transfer and completes the DMA transfer operation.
- Size: 64 bits
- Offset: 0x120 + (x-1) * 0x100
- Exists: REE DMA Only

Figure & Table 14-24 Fields for register: CHx_CFG2 (for x = 1; x <= 4)

Bits	Name	Access	Description
63	RSVD_DMAC_CHx_CFG_63	R	DMAC Channelx Transfer Configuration Register (63bit) Reserved bit - Read Only

Bits	Name	Access	Description
			Value After Reset: 0x0 Exists: Always
62:59	DST_OSR_LMT	R/W	Destination Outstanding Request Limit. Maximum outstanding request supported is 16. Source Outstanding Request Limit = DST_OSR_LMT + 1 Value After Reset: 0x0 Exists: Always
58:55	SRC_OSR_LMT	R/W	Source Outstanding Request Limit. Maximum outstanding request supported is 16. Source Outstanding Request Limit = SRC_OSR_LMT + 1 Value After Reset: 0x0 Exists: Always
54:53	LOCK_CH_L	R	Channel Lock Level. This bit indicates the duration over which CHx_CFG.LOCK_CH bit applies. ■ 00: Over complete DMA transfer ■ 01: Over DMA block transfer ■ 1x: Reserved This field does not exist if the configuration parameter DMAX_CHx_LOCK_EN is set to False; in that case, the read-back value is always 0. Values: ■ 0x0 (DMA_transfer_CH_LOCK): Duration of the Channel locking is for the entire DMA transfer. ■ 0x1 (BLOCK_TRANFER_CH_LOCK): Duration of the Channel locking is for the current block transfer. Value After Reset: 0x0 Exists: Always
52	LOCK_CH	R	Channel Lock bit. When the channel is granted control of the master bus interface and if the CHx_CFG.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CHx_CFG.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CHx_CFG.LOCK_CH_L. This field does not exist if the configuration parameter

Bits	Name	Access	Description
			DMAX_CHx_LOCK_EN is set to False; in this case, the read-back value is always 0. Locking the channel locks AXI Read Address, Write Address and Write Data channels on the corresponding master interface. Note: Channel locking feature is supported only for memoryto-memory transfer at Block Transfer and DMA Transfer levels. Hardware does not check for the validity of channel locking setting, hence the software must take care of enabling the channel locking only for memory-to-memory transfers at Block Transfer or DMA Transfer levels. Illegal programming of channel locking might result in unpredictable behavior. Values: ■ 0x0 (NO_CHANNEL_LOCK): Channel is not locked during the transfers. ■ 0x1 (CHANNEL_LOCK): Channel is locked and granted exclusive access to the Master Bus Interface. Value After Reset: 0x0 Exists: Always
51:47	CH_PRIOR	R/W	Channel Priority. A priority of DMAX_NUM_CHANNELS-1 is the highest priority, and 0 is the lowest. This field must be programmed within the following range: 0: 3 A programmed value outside this range will cause erroneous behavior. Value After Reset: 4 - x Exists: Always
46:39	RSVD_DMAC_CHx_CFG_39to46	R	DMAC Channelx Transfer Configuration Register (bits 39 to 46) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
38	DST_HWHS_POL	R	Destination Hardware Handshaking Interface Polarity. 0: ACTIVE HIGH. 1: ACTIVE LOW. Values: ■ 0x0 (ACTIVE_HIGH): Polarity of the Handshaking

Bits	Name	Access	Description
			Interface used for the Destination peripheral is Active High. ■ 0x1 (ACTIVE_LOW): Polarity of the Handshaking Interface used for the Destination peripheral is Active Low. Value After Reset: 0x0 Exists: Always
37	SRC_HWHS_POL	R	Source Hardware Handshaking Interface Polarity. 0: ACTIVE HIGH. 1: ACTIVE LOW. Values: ■ 0x0 (ACTIVE_HIGH): Polarity of the Handshaking Interface used for the Source peripheral is Active High. ■ 0x1 (ACTIVE_LOW): Polarity of the Handshaking Interface used for the Source peripheral is Active Low. Value After Reset: 0x0 Exists: Always
36	HS_SEL_DST	R/W	Destination Software or Hardware Handshaking Select. This register selects which of the handshaking interfaces (hardware or software) is active for destination requests on this channel. ■ 0: Hardware handshaking interface. Software-initiated transaction requests are ignored. ■ 1: Software handshaking interface. Hardware-initiated transaction requests are ignored. If the destination peripheral is memory, then this bit is ignored. Values: ■ 0x0 (HARDWARE_HS): Hardware Handshaking Interface is used for the Destination peripheral. ■ 0x1 (SOFTWARE_HS): Software Handshaking Interface is used for the Destination peripheral. Value After Reset: 0x1 Exists: Always
35	HS_SEL_SRC	R/W	Source Software or Hardware Handshaking Select. This register selects which of the handshaking interfaces (hardware or software) is active for source

Bits	Name	Access	Description
			requests on this channel. ■ 0: Hardware handshaking interface. Software-initiated transaction requests are ignored. ■ 1: Software handshaking interface. Hardware-initiated transaction requests are ignored. If the source peripheral is memory, then this bit is ignored. Values: ■ 0x0 (HARDWARE_HS): Hardware Handshaking Interface is used for the Source peripheral. ■ 0x1 (SOFTWARE_HS): Software Handshaking Interface is used for the Source peripheral. Value After Reset: 0x1 Exists: Always
34:32	TT_FC	R/W	Transfer Type and Flow Control. The following transfer types are supported. ■ Memory to Memory ■ Memory to Peripheral ■ Peripheral to Memory ■ Peripheral to Peripheral Flow Control can be assigned to the DW_axi_dmac, the source peripheral, or hte destination peripheral. Values: ■ 0x0 (MEM_TO_MEM_DMAC): Transfer Type is memory to memory and Flow Controller is DW_axi_dmac. ■ 0x1 (MEM_TO_PER_DMAC): Transfer Type is memory to peripheral and Flow Controller is DW_axi_dmac. ■ 0x2 (PER_TO_MEM_DMAC): Transfer Type is peripheral to memory and Flow Controller is DW_axi_dmac. ■ 0x3 (PER_TO_PER_DMAC): Transfer Type is peripheral to peripheral and Flow Controller is DW_axi_dmac. ■ 0x4 (PER_TO_MEM_SRC): Transfer Type is peripheral to Memory and Flow Controller is Source peripheral. ■ 0x5 (PER_TO_PER_SRC): Transfer Type is peripheral to peripheral and Flow Controller is Source

Bits	Name	Access	Description
			peripheral. ■ 0x6 (MEM_TO_PER_DST): Transfer Type is memory to peripheral and Flow Controller is Destination peripheral. ■ 0x7 (PER_TO_PER_DST): Transfer Type is peripheral to peripheral and Flow Controller is Destination peripheral. Value After Reset: 3 Exists: Always
31:18	RSVD_DMAC_CHx_CFG_18to31	R	DMAC Channelx Transfer Configuration Register (bits 18 to 31) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
17	RSVD_DMAC_CHx_CFG_17	R	DMAC Channelx Transfer Configuration Register (bit 17) Reserved bit - Read Only Value After Reset: 0x0 Exists: Always
16:11	DST_PER	R/W	Assigns a hardware handshaking interface (0 - DMAX_NUM_HS_IF-1) to the destination of Channelx if the CHx_CFG.HS_SEL_DST field is 0; otherwise, this field is ignored. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. Note: For correct DW_axi_dmac operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. This field does not exist if the configuration parameter DMAX_NUM_HS_IF is set to 0. x = 11 if DMAC_NUM_HS_IF is 1. x = ceil(log2(DMAC_NUM_HS_IF)) + 10 if DMAC_NUM_HS_IF is greater than 1. Bits 16: (x+1) do not exist and return 0 on a read. Value After Reset: 0x0 Exists: Always
10	RSVD_DMAC_CHx_CFG_10	R	DMAC Channelx Transfer Configuration Register (bit 10) Reserved bit - Read Only Value After Reset: 0x0 Exists: Always

Bits	Name	Access	Description
9:4	SRC_PER	R/W	Assigns a hardware handshaking interface (0 - DMAX_NUM_HS_IF-1) to the source of Channelx if the CHx_CFG.HS_SEL_SRC field is 0; otherwise, this field is ignored. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. Note: For correct DW_axi_dmac operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. This field does not exist if the configuration parameter DMAX_NUM_HS_IF is set to 0. x = 4 if DMAC_NUM_HS_IF is 1. x = ceil(log2(DMAC_NUM_HS_IF) + 3 if DMAC_NUM_HS_IF is greater than 1. Bits 9: (x+1) do not exist and return 0 on a read. Value After Reset: 0x0 Exists: Always
3:2	DST_MULTBLK_TYPE	R/W	Destination Multi Block Transfer Type. These bits define the type of multi-block transfer used for destination peripheral. ■ 00: Contiguous ■ 01: Reload ■ 10: Shadow Register ■ 11: Linked List If the type selected is Contiguous, the CHx_DAR register is loaded with the value of the end source address of previous block + 1 at the end of every block for multi-block transfers. A new block transfer is then initiated. If the type selected is Reload, the CHx_DAR register is reloaded from the initial value of DAR at the end of every block for multi-block transfers. A new block transfer is then initiated. If the type selected is Shadow Register, the CHx_DAR register is loaded from the content of its shadow register if CHx_CTL.ShadowReg_Or_LLI_Valid bit is set to 1 at the end of every block for multi-block transfers. A new block transfer is then initiated. If the type selected is Linked List, the CHx_DAR register is loaded from the Linked List if CTL.ShadowReg_Or_LLI_Valid bit is set to 1 at the end of every block for multi-block transfers. A new block transfer is then initiated.

Bits	Name	Access	Description
			CHx_CTL and CHx_BLOCK_TS registers are loaded from their initial values or from the contents of their shadow registers (if CHx_CTL.ShadowReg_Or_LLI_Valid bit is set to 1) or from the linked list (if CTL.ShadowReg_Or_LLI_Valid bit is set to 1) at the end of every block for multi-block transfers based on the multi-block transfer type programmed for source and destination peripherals. Contiguous transfer on both source and destination peripheral is not a valid multi-block transfer configuration. This field does not exist if the configuration parameter DMAX_CHx_MULTI_BLK_EN is not selected; in that case, the read-back value is always 0. Values: ■ 0x0 (CONTINGUOUS): Contiguous Multiblock Type used for Destination Transfer. ■ 0x1 (RELOAD): Reload Multiblock Type used for Destination Transfer. ■ 0x2 (SHADOW_REGISTER): Shadow Register based Multiblock Type used for Destination Transfer. ■ 0x3 (LINKED_LIST): Linked List based Multiblock Type used for Destination Transfer. Value After Reset: 0 Exists: Always
1:0	SRC_MULTBLK_TYPE	R/W	Source Multi Block Transfer Type. These bits define the type of multi-block transfer used for source peripheral. ■ 00: Contiguous ■ 01: Reload ■ 10: Shadow Register ■ 11: Linked List If the type selected is Contiguous, the CHx_SAR register is loaded with the value of the end source address of previous block + 1 at the end of every block for multi-block transfers. A new block transfer is then initiated. If the type selected is Reload, the CHx_SAR register is reloaded from the initial value of SAR at the end of every block for multi-block transfers. A new block transfer is then initiated.

Bits	Name	Access	Description
			If the type selected is Shadow Register, the CHx_SAR register is loaded from the content of its shadow register if CHx_CTL.ShadowReg_Or_LLI_Valid bit is set to 1 at the end of every block for multi-block transfers. A new block transfer is then initiated. If the type selected is Linked List, the CHx_SAR register is loaded from the Linked List if CTL.ShadowReg_Or_LLI_Valid bit is set to 1 at the end of every block for multi-block transfers. A new block transfer is then initiated. CHx_CTL and CHx_BLOCK_TS registers are loaded from their initial values or from the contents of their shadow registers (if CHx_CTL.ShadowReg_Or_LLI_Valid bit is set to 1) or from the linked list (if CTL.ShadowReg_Or_LLI_Valid bit is set to 1) at the end of every block for multi-block transfers based on the multi-block transfer type programmed for source and destination peripherals. Contiguous transfer on both source and destination peripheral is not a valid multi-block transfer configuration. This field does not exist if the configuration parameter DMAX_CHx_MULTI_BLK_EN is not selected; in that case, the read-back value is always 0. Values: ■ 0x0 (CONTINGUOUS): Contiguous Multiblock Type used for Source Transfer. ■ 0x1 (RELOAD): Reload Multiblock Type used for Source Transfer. ■ 0x2 (SHADOW_REGISTER): Shadow Register based Multiblock Type used for Source Transfer. ■ 0x3 (LINKED_LIST): Linked List based Multiblock Type used for Source Transfer. Value After Reset: 0 Exists: Always

14.5.2.7 CHx_LLP (for x = 1; x <= 4)

- Description: This is the Linked List Pointer register. This register must be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if linked-list-based block chaining is enabled. This register is updated with new value of linked list pointer during the LLI update stage of dma transfer.

- Size: 64 bits
- Offset: 0x128 + (x-1)*0x100
- Exists: Yes

Figure & Table 14-25 Fields for register: CHx_LLP (for x = 1; x <= 4)

Bits	Name	Access	Description
63:6	LOC	R/W	Starting Address Memory of LLI block. Starting Address In Memory of next LLI if block chaining is enabled. The six LSBs of the starting address are not stored because the address is assumed to be aligned to a 64-byte boundary. LLI access always uses the burst size (arsize/awsize) that is same as the data bus width and cannot be changed or programmed to anything other than this. Burst length (awlen/arlen) is chosen based on the data bus width so that the access does not cross one complete LLI structure of 64 bytes. DW_axi_dmac will fetch the entire LLI (40 bytes) in one AXI burst if the burst length is not limited by other settings. Value After Reset: 0x0 Exists: Always Volatile: True
5:1	RSVD_DMAC_CHx_LLP_1to5	R	DMAC Channelx Linked List Pointer Register (bits 1 to 5) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always Volatile: True
0	LMS	R	LLI master Select. This bit identifies the AXI layer/interface where the memory device that stores the next linked list item resides. ■ 0: AXI Master 1 ■ 1: AXI Master 2 This field does not exist if the configuration parameter DMAX_CHx_LMS is not set to NO_HARDCODE. In this case, the read-back value is always the hardcoded value. The maximum value of this field that can be read back is 'DMAX_NUM_MASTER_IF-1'. Values: ■ 0x0 (MASTER1_INTF): Next Linked List item resides on AXI Master1 interface.

Bits	Name	Access	Description
			■ 0x1 (MASTER2_INTF): Next Linked List item resides on AXI Master2 interface. Value After Reset: 0x0 Exists: Always Volatile: True

14.5.2.8 CHx_STATUSREG (for x = 1; x <= 4)

- Description: Channelx Status Register contains fields that indicate the status of DMA transfers for Channelx.
- Size: 64 bits
- Offset: 0x130 + (x-1)*0x100
- Exists: Yes

Figure & Table 14-26 Fields for register: CHx_STATUSREG (for x = 1; x <= 4)

Bits	Name	Access	Description
63:47	RSVD_DMAC_CHx_STATUSREG _47to63	R	DMAC Channelx Status Register (bits 47 to 63) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always Volatile: True
46:32	DATA_LEFT_IN_FIFO	R	Data Left in FIFO. This bit indicates the total number of data left in DW_axi_dmac channel FIFO after completing the current block transfer. The width of the data in channel FIFO is equal to CHx_CTL.SRC_TR_WIDTH. For normal block transfer completion without errors, Data_Left_In_FIFO = 0. If any error occurs during the dma transfer, the block transfer might be terminated early and in such a case, Data_Left_In_FIFO indicates the data remaining in channel FIFO which could not be transferred to destination peripheral. This field is cleared to zero on enabling the channel. Note: If CHx_CTL.DST_TR_WIDTH > CHx_CTL.SRC_TR_WIDTH, there may be residual data left in the FIFO which is not enough to form one CHx_CTL.SRC_TR_WIDTH of data and Data_Left_In_FIFO will return 0 in this case.

Bits	Name	Access	Description
			Value After Reset: 0x0 Exists: Always Volatile: True
31:22	RSVD_DMAC_CHx_STATUSREG_22to31	R	DMAC Channelx Status Register (bits 22 to 31) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always Volatile: True
21:0	CMPLTD_BLK_TFR_SIZE	R	Completed Block Transfer Size. This bit indicates the total number of data of width CHx_CTL.SRC_TR_WIDTH transferred for the previous block transfer. For normal block transfer completion without any errors, this value will be equal to the value programmed in BLOCK_TS field of CHx_BLOCK_TS register. If any error occurs during the dma transfer, the block transfer might be terminated early and in such a case, this value indicates the actual data transferred without error in the current block. This field is cleared to zero on enabling the channel. Value After Reset: 0x0 Exists: Always Volatile: True

14.5.2.9 CHx_SWHSSRCREG (for x = 1; x <= 4)

- Description: Channelx Software handshake Source Register.
- Size: 64 bits
- Offset: 0x138 + (x-1)*0x100
- Exists: Yes

Figure & Table 14-27 Fields for register: CHx_SWHSSRCREG (for x = 1; x <= 4)

Bits	Name	Access	Description
63:6	RSVD_DMAC_CHx_SWHSSRCREG_6to63	R	DMAC Channelx Software Handshake Source Register (bits 6 to 63) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always Volatile: True

Bits	Name	Access	Description
5	SWHS_LST_SRC_WE	W	Write Enable bit for Software Handshake Last Request for Channel Source. Values: ■ 0x1 (ENABLE_SWHS_LAST_SRC): Enables write to the SWHS_LAST_SRC bit. ■ 0x0 (DISABLE_SWHS_LAST_SRC): Disables write to the SWHS_LAST_SRC bit. Value After Reset: 0x0 Exists: Always Volatile: True
4	SWHS_LST_SRC	R/W	Software Handshake Last Request for Channel Source. This bit is used to request LAST dma source data transfer if software handshaking method is selected for the source of the corresponding channel. This bit is ignored if software handshaking is not enabled for the source of the Channelx or if the source of Channelx is not the flow controller. CHx_SWHSSrcReg.SWHS_Req_Src bit must be set to 1 for DW_axi_dmac to treat it as a valid software handshaking request. If CHx_SWHSSrcReg.SWHS_SglReq_Src is set to 1, the LAST request is for SINGLE dma transaction (AXI burst length = 1), else the request is treated as a BURST transaction request. DW_axi_dmac clears this bit to 0 once software reads CHx_SWHSSrcReg.SWHS_Ack_Src bit and sees it as 1. Software can only set this bit to 1; it is not allowed to clear this bit to 0; only DW_axi_dmac can clear this bit. Note: SWHS_Lst_Src bit is written only if the corresponding write enable bit, SWHS_Lst_Src_WE is asserted on the same register write operation and if the Channelx is enabled in the DMAC_ChEnReg register. This allows software to set a bit in the CHx_SWHSSrcReg register without performing a read-modified write operation. Values: ■ 0x1 (ACTIVE_SWHS_LAST_SRC): Source peripheral indication to dmac that the current transfer is the last transfer. ■ 0x0 (INACTIVE_SWHS_LAST_SRC): Source peripheral indication that the current transfer is

Bits	Name	Access	Description
			not the last transfer. Value After Reset: 0x0 Exists: Always Volatile: True
3	SWHS_SGLREQ_SRC_WE	W	Write Enable bit for Software Handshake Single Request for Channel Source. Values: ■ 0x1 (ENABLE_SWHS_SGLREQ_SRC): Enables write to the SWHS_SGLREQ_SRC bit. ■ 0x0 (DISABLE_SWHS_SGLREQ_SRC): Disables write to the SWHS_SGLREQ_SRC bit. Value After Reset: 0x0 Exists: Always Volatile: True
2	SWHS_SGLREQ_SRC	R/W	Software Handshake Single Request for Channel Source. This bit is used to request SINGLE (AXI burst length = 1) dma source data transfer if software handshaking method is selected for the source of the corresponding channel. This bit is ignored if software handshaking is not enabled for the source of the Channelx. The functionality of this field depends on whether the peripheral is the flow controller. DW_axi_dmac clears this bit to 0 once software reads CHx_SWHSSrcReg.SWHS_Ack_Src bit and sees it as 1. Software can only set this bit to 1; it is not allowed to clear this bit to 0; only DW_axi_dmac can clear this bit. Note: SWHS_SglReq_Src bit is written only if the corresponding write enable bit, SWHS_SglReq_Src_WE is asserted on the same register write operation and if the Channelx is enabled in the DMAC_ChEnReg register. This allows software to set a bit in the CHx_SWHSSrcReg register without performing a read-modified write operation. Values: ■ 0x1 (ACTIVE_SWHS_SGLREQ_SRC): Source peripheral request for a single dma transfer. ■ 0x0 (INACTIVE_SWHS_SGLREQ_SRC): Source peripheral is not requesting for a single transfer. Value After Reset: 0x0

Bits	Name	Access	Description
			Exists: Always Volatile: True
1	SWHS_REQ_SRC_WE	W	Write Enable bit for Software Handshake Request for Channel Source. Note: This bit always returns 0 on a read back. Values: ■ 0x1 (ENABLE_SWHS_REQ_SRC): Enables write to the SWHS_REQ_SRC bit. ■ 0x0 (DISABLE_SWHS_REQ_SRC): Disables write to the SWHS_REQ_SRC bit. Value After Reset: 0x0 Exists: Always Volatile: True
0	SWHS_REQ_SRC	R/W	Software Handshake Request for Channel Source. This bit is used to request dma source data transfer if software handshaking method is selected for the source of the corresponding channel. This bit is ignored if software handshaking is not enabled for the source of the Channelx. The functionality of this field depends on whether the peripheral is the flow controller or not. DW_axi_dmac clears this bit to 0 once software reads CHx_SWHSSrcReg.SWHS_Ack_Src bit and sees it as 1. Software can only set this bit to 1; it is not allowed to clear this bit to 0; only DW_axi_dmac can clear this bit. Note: SWHS_Req_Src bit is written only if the corresponding write enable bit, SWHS_Req_Src_WE is asserted on the same register write operation and if the Channelx is enabled in the DMAC_ChEnReg register. This allows software to set a bit in the CHx_SWHSSrcReg register without performing a read-modified write operation. Values: ■ 0x1 (ACTIVE_SWHS_REQ_SRC): Source peripheral request for a dma transfer. ■ 0x0 (INACTIVE_SWHS_REQ_SRC): Source peripheral is not requesting for a burst transfer. Value After Reset: 0x0 Exists: Always

Bits	Name	Access	Description
			Volatile: true

14.5.2.10 CHx_SWHSDSTREG (for x = 1; x <= 4)

- Description: Channelx Software handshake Destination Register.
- Size: 64 bits
- Offset: 0x140 + (x-1)*0x100
- Exists: Yes

Figure & Table 14-28 Fields for register: CHx_SWHSDSTREG (for x = 1; x <= 4)

Bits	Name	Access	Description
63:6	RSVD_DMAC_CHx_SWHSDSTREG_6to63	R	DMAC Channelx Software Handshake Destination Register (bits 6 to 63) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always Volatile: True
5	SWHS_LST_DST_WE	W	Write Enable bit for Software Handshake Last Request for Channel Destination. Note: This bit always returns 0 on a read back. Values: ■ 0x1 (ENABLE_SWHS_LAST_DST): Enables write to the SWHS_LAST_DST bit. ■ 0x0 (DISABLE_SWHS_LAST_DST): Disables write to the SWHS_LAST_DST bit. Value After Reset: 0x0 Exists: Always Volatile: True
4	SWHS_LST_DST	R/W	Software Handshake Last Request for Channel Destination. This bit is used to request LAST dma destination data transfer if software handshaking method is selected for the destination of the corresponding channel. This bit is ignored if software handshaking is not enabled for the destination of the Channelx or if the destination of Channelx is not the flow controller. CHx_SWHSDstReg.SWHS_Req_Dst bit must be set to 1 for DW_axi_dmac to treat it as a valid software handshaking request. If CHx_SWHSDstReg.SWHS_SglReq_Dst is set to 1, the LAST request is for SINGLE dma transaction (AXI burst

Bits	Name	Access	Description
			length = 1), else the request is treated as a BURST transaction request. DW_axi_dmac clears this bit to 0 once software reads CHx_SWHSDstReg.SWHS_Ack_Dst bit and sets it as 1. Software can only set this bit to 1; it is not allowed to clear this bit to 0; only DW_axi_dmac can clear this bit. Note: SWHS_Lst_Src bit is written only if the corresponding write enable bit, SWHS_Lst_Src_WE is asserted on the same register write operation and if the Channelx is enabled in the DMAC_ChEnReg register. This allows software to set a bit in the CHx_SWHSDstReg register without performing a read-modified write operation. Values: ■ 0x1 (ACTIVE_SWHS_LAST_DST): Destination peripheral indication to dmac that the current transfer is the last transfer. ■ 0x0 (INACTIVE_SWHS_LAST_DST): Destination peripheral indication that the current transfer is not the last transfer. Value After Reset: 0x0 Exists: Always Volatile: True
3	SWHS_SGLREQ_DST_WE	W	Write Enable bit for Software Handshake Single Request for Channel Destination. Note: This bit always returns 0 on a read block. Values: ■ 0x1 (ENABLE_SWHS_SGLREQ_DST): Enables write to the SWHS_SGLREQ_DST bit. ■ 0x0 (DISABLE_SWHS_SGLREQ_DST): Disables write to the SWHS_SGLREQ_DST bit. Value After Reset: 0x0 Exists: Always Volatile: True
2	SWHS_SGLREQ_DST	R/W	Software Handshake Single Request for Channel Destination. This bit is used to request SINGLE (AXI burst length = 1) dma destination data transfer if software handshaking method is selected for the destination of the corresponding channel.

Bits	Name	Access	Description
			This bit is ignored if software handshaking is not enabled for the destination of the Channelx. The functionality of this field depends on whether the peripheral is the flow controller. DW_axi_dmac clears this bit to 0 once software reads CHx_SWHSDstReg.SWHS_Ack_Dst bit and sees it as 1. Software can only set this bit to 1; it is not allowed to clear this bit to 0; only DW_axi_dmac can clear this bit. Note: SWHS_SglReq_Dst bit is written only if the corresponding write enable bit, SWHS_SglReq_Dst_WE is asserted on the same register write operation and if the Channelx is enabled in the DMAC_ChEnReg register. This allows software to set a bit in the CHx_SWHSDstReg register without performing a read-modified write operation. Values: ■ 0x1 (ACTIVE_SWHS_SGLREQ_DST): Destination peripheral request for a single dma transfer. ■ 0x0 (INACTIVE_SWHS_SGLREQ_DST): Destination peripheral is not requesting for a single transfer. Value After Reset: 0x0 Exists: Always Volatile: True
1	SWHS_REQ_DST_WE	W	Write Enable bit for Software Handshake Request for Channel Destination. Note: This bit always returns 0 on a read block. Values: ■ 0x1 (ENABLE_SWHS_REQ_DST): Enables write to the SWHS_REQ_DST bit. ■ 0x0 (DISABLE_SWHS_REQ_DST): Disables write to the SWHS_REQ_DST bit. Value After Reset: 0x0 Exists: Always Volatile: True
0	SWHS_REQ_DST	R/W	Software Handshake Request for Channel Destination. This bit is used to request dma destination data transfer if software handshaking method is selected for the destination of the corresponding channel. This bit is ignored if software handshaking is not enabled for the source of the Channelx. The

Bits	Name	Access	Description
			functionality of this field depends on whether the peripheral is the flow controller. DW_axi_dmac clears this bit to 0 once software reads CHx_SWHSDstReg.SWHS_Ack_Dst bit and sees it as 1. Software can only set this bit to 1; it is not allowed to clear this bit to 0; only DW_axi_dmac can clear this bit. Note: SWHS_Req_Dst bit is written only if the corresponding write enable bit, SWHS_Req_Dst_WE is asserted on the same register write operation and if the Channelx is enabled in the DMAC_ChEnReg register. This allows software to set a bit in the CHx_SWHSDstReg register without performing a read-modified write operation. Values: ■ 0x1 (ACTIVE_SWHS_REQ_DST): Destination peripheral request for a DMA transfer. ■ 0x0 (INACTIVE_SWHS_REQ_DST): Destination peripheral is not requesting for a burst transfer. Value After Reset: 0x0 Exists: Always Volatile: True

14.5.2.11 CHx_BLK_TFR_RESUMEREQREG (for x = 1; x <= 4)

- Description: Channelx Block Transfer Resume Request Register. This register is used during Linked List or Shadow Register based multi-block transfer.
  - For Linked-List-based multi-block transfer, ShadowReg_Or_LLI_Valid bit in LLI.CHx_CTL indicates whether the linked list item fetched from the memory is valid (0: LLI is invalid, 1: LLI is valid). On noticing this bit as 0, DW_axi_dmac discards the LLI and generates ShadowReg_Or_LLI_Invalid_ERR Interrupt if the corresponding channel error interrupt mask bit is set to 0. This error condition causes the DW_axi_dmac to halt the corresponding channel gracefully. DW_axi_dmac waits till software writes (any value) to CHx_BLK_TFR_ResumeReqReg to indicate valid LLI availability, before attempting another LLI read operation.
  - For Shadow-Register-based multi-block transfer, ShadowReg_Or_LLI_Valid bit in CHx_CTL register indicates whether the shadow register contents are valid (0: Shadow Register contents are invalid, 1: Shadow Register contents are valid). On noticing this bit as 0 during shadow register fetch phase, DW_axi_dmac discards the Shadow Register contents and generates ShadowReg_Or_LLI_Invalid_ERR Interrupt. DW_axi_dmac waits till software writes (any value) to CHx_BLK_TFR_ResumeReqReg to indicate valid shadow register

availability, before attempting another shadow register fetch operation and continue the next block transfer.

- Size: 64 bits
- Offset: 0x148 + (x-1)*0x100
- Exists: Yes

Figure & Table 14-29 Fields for register: CHx_BLK_TFR_RESUMEREQREG (for x = 1; x <= 4)

Bits	Name	Access	Description
63:1	RSVD_DMAC_CHx_BLK_TFR_RESUMEREQREG_1to63	W	DMAC Channelx Block Transfer Resume Request Register (bits 1 to 63) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
0	BLK_TFR_RESUMEREQ	W	Block Transfer Resume Request during Linked-List or Shadow-Register-based multi-block transfer. Values: ■ 0x0 (INACTIVE_BLK_TFR_RESUMEREQ): No request to resume the block transfer. ■ 0x1 (ACTIVE_BLK_TFR_RESUMEREQ): Request for resuming the block transfer. Value After Reset: 0x0 Exists: Always

14.5.2.12 CHx_AXI_IDREG (for x = 1; x <= 4)

- Description: Channelx AXI ID Register. This register is allowed to be updated only when the channel is disabled, which means that it remains fixed for the entire DMA transfer.
- Size: 64 bits
- Offset: 0x150 + (x-1)*0x100
- Exists: Yes

Figure & Table 14-30 Fields for register: CHx_AXI_IDREG (for x = 1; x <= 4)

Bits	Name	Access	Description
63:32	RSVD_DMAC_CHx_AXI_IDREG_32to63	R	DMAC Channelx AXI ID Register (bits 32 to 63) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
31:19	RSVD_DMAC_CHx_AXI_IDREG_IDW_L2NCm32to63	R	DMAC Channelx AXI ID Register (bits (IDW-L2NC-1) to 32) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always

Bits	Name	Access	Description
18:16	AXI_WRITE_ID_SUFFIX	R/W	AXI Write ID Suffix. These bits form part of the AWID output of AXI3/AXI4 master interface. IDW = DMAX_M_ID_WIDTH L2NC = log2(DMAX_NUM_CHANNELS) The upper L2NC+1 bits of awidN is derived from the channel number which is currently accessing the master interface. This varies for LLI fetch and source data transfer. For source data transfer, awidN for channel1 4'b0000, awidN for channel8 4'b0111 and so on. For LLI fetch access, awidN for channel1 4'b1000, awidN for channel8 4'b1111 and so on. Lower bits are same as the value programmed in CHx_AXI_IDReg.AXI_Write_ID_Suffix field. Value After Reset: 0x0 Exists: Always
15:3	RSVD_DMAC_CHx_AXI_IDREG_ IDW_L2NCm1to31	R	DMAC Channelx AXI ID Register (bits (IDW-L2NC-1) to 31) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
2:0	AXI_READ_ID_SUFFIX	R/W	AXI Read ID Suffix. These bits form part of the ARID output of AXI3/AXI4 master interface. IDW = DMAX_M_ID_WIDTH L2NC = log2(DMAX_NUM_CHANNELS) The upper L2NC+1 bits of aridN is derived from the channel number which is currently accessing the master interface. This varies for LLI fetch and source data transfer. For source data transfer, aridN for channel1 4'b0000, aridN for channel8 4'b0111 and so on. For LLI fetch access, aridN for channel1 4'b1000, aridN for channel8 4'b1111 and so on. Lower bits are same as the value programmed in CHx_AXI_IDReg.AXI_Read_ID_Suffix field. Value After Reset: 0x0 Exists: Always

14.5.2.13 CHx_AXI_QOSREG (for x = 1; x <= 4)

- Description: Channelx AXI QOS Register. This register is allowed to be updated only when the channel is disabled, which means that it remains fixed for the entire DMA transfer.
- Size: 64 bits
- Offset: 0x158 + (x-1) * 0x100
- Exists: Yes

Figure & Table 14-31 Fields for register: CHx_AXI_QOSREG (for x = 1; x <= 4)

Bits	Name	Access	Description
63:8	RSVD_DMAC_CHx_AXI_QOSREG_8to63	R	DMAC Channelx AXI QOS Register (bits 8 to 63) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always
7:4	AXI_ARQOS	R/W	AXI ARQOS. These bits form the arqos output of AXI4 master interface. Value After Reset: 0x0 Exists: Always
3:0	AXI_AWQOS	R/W	AXI AWQOS. These bits form the awqos output of AXI4 master interface. Value After Reset: 0x0 Exists: Always

14.5.2.14 CHx_INTSTATUS_ENABLEREG (for x = 1; x <= 4)

- Description: Writing 1 to specific field enables the corresponding interrupt status generation in Channelx Interrupt Status Register (CH1_IntStatusReg).
- Size: 64 bits
- Offset: 0x180 + (x-1)*0x100
- Exists: Yes

Figure & Table 14-32 Fields for register: CHx_INTSTATUS_ENABLEREG (for x = 1; x <= 4)

Bits	Name	Access	Description
63:32	RSVD_DMAC_CHx_INTSTATUS_ENABLEREG_32to63	R	DMAC Channelx Interrupt Status Register (bits 32 to 63) Reserved bits - Read Only Value After Reset: 0xffffffff Exists: Always
31	Enable_CH_ABORTED_IntStat	R/W	Channel Aborted Status Enable.

Bits	Name	Access	Description
			■ 0: Disable the generation of Channel Aborted Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Channel Aborted Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_CH_ABORTED): Enable the generation of Channel Aborted Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_CH_ABORTED): Disable the generation of Channel Aborted Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
30	Enable_CH_DISABLED_IntStat	R/W	Channel Disabled Status Enable. ■ 0: Disable the generation of Channel Disabled Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Channel Disabled Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_CH_DISABLED): Enable the generation of Channel Disabled Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_CH_DISABLED): Disable the generation of Channel Disabled Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
29	Enable_CH_SUSPENDED_IntStat	R/W	Channel Suspended Status Enable. ■ 0: Disable the generation of Channel Suspended Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Channel Suspended Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_CH_SUSPENDED): Enable the generation of Channel Suspended Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_CH_SUSPENDED): Disable the generation of Channel Suspended Interrupt in CH1_INTSTATUSREG.

Bits	Name	Access	Description
			Value After Reset: 0x1 Exists: Always
28	Enable_CH_SRC_SUSPENDED_ IntStat	R/W	Channel Source Suspended Status Enable. ■ 0: Disable the generation of Channel Source Suspended Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Channel Source Suspended Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_CH_SRC_SUSPENDED): Enable the generation of Channel Source Suspended Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_CH_SRC_SUSPENDED): Disable the generation of Channel Source Suspended Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
27	Enable_CH_LOCK_CLEARED_In tStat	R/W	Channel Lock Cleared Status Enable. ■ 0: Disable the generation of Channel LOCK CLEARED Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Channel LOCK CLEARED Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_CH_LOCK_CLEARED): Enable the generation of Channel LOCK CLEARED Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_CH_LOCK_CLEARED): Disable the generation of Channel LOCK CLEARED Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
26:22	RSVD_DMAC_CHx_INTSTATUS_ ENABLEREG_22to26	R	DMAC Channelx Interrupt Status Register (bits 22 to 26) Reserved bits - Read Only Value After Reset: 0x1f Exists: Always
21	Enable_SLVIF_WRONHOLD_ER R_IntStat	R/W	Slave Interface Write On Hold Error Status Enable. ■ 0: Disable the generation of Slave Interface Write On Hold Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Slave Interface Write

Bits	Name	Access	Description
			On Hold Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_SLVIF_WRONHOLD_ERR): Enable the generation of Slave Interface Write On Hold Error Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_SLVIF_WRONHOLD_ERR): Disable the generation of Slave Interface Write On Hold Error Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
20	Enable_SLVIF_SHADOWREG_WRON_VALID_ERR_IntStat	R/W	Shadow Register Write On Valid Error Status Enable. ■ 0: Disable the generation of Shadow Register Write On Valid Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Shadow register Write On Valid Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_SLVIF_SHADOWREG_WRON_VALID_ERR): Enable the generation of Shadow register Write On Valid Error Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_SLVIF_SHADOWREG_WRON_VALID_ERR): Disable the generation of Shadow Register Write On Valid Error Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
19	Enable_SLVIF_WRONCHEN_ERR_IntStat	R/W	Slave Interface Write On Channel Enabled Error Status Enable. ■ 0: Disable the generation of Slave Interface Write On Channel enabled Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Slave Interface Write On Channel enabled Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_SLVIF_WRONCHEN_ERR): Enable the generation of Slave Interface Write On Channel enabled Error Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_SLVIF_WRONCHEN_ERR): Disable the generation of Slave Interface Write On Channel

Bits	Name	Access	Description
			enabled Error Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
18	Enable_SLVIF_RD2RWO_ERR_IntStat	R/W	Slave Interface Read to write Only Error Status Enable. ■ 0: Disable the generation of Slave Interface Read to Write only Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Slave Interface Read to Write Only Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_SLVIF_RD2RWO_ERR): Enable the generation of Slave Interface Read to Write Only Error Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_SLVIF_RD2RWO_ERR): Disable the generation of Slave Interface Read to Write only Error Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
17	Enable_SLVIF_WR2RO_ERR_IntStat	R/W	Slave Interface Write to Read Only Error Status Enable. ■ 0: Disable the generation of Slave Interface Write to Read only Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Slave Interface Write to Read Only Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_SLVIF_WR2RO_ERR): Enable the generation of Slave Interface Write to Read Only Error Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_SLVIF_WR2RO_ERR): Disable the generation of Slave Interface Write to Read only Error Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
16	Enable_SLVIF_DEC_ERR_IntStat	R/W	Slave Interface Decode Error Status Enable. ■ 0: Disable the generation of Slave Interface Decode Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Slave Interface Decode Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_SLVIF_DEC_ERR): Enable the generation of Slave Interface Decode Error

Bits	Name	Access	Description
			Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_SLVIF_DEC_ERR): Disable the generation of Slave Interface Decode Error Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
15	RSVD_DMAC_CHx_INTSTATUS_ENABLEREG_15	R	DMAC Channelx Interrupt Status Register (bit 15) Reserved bit - Read Only Value After Reset: 0x1 Exists: Always
14	Enable_SLVIF_MULTIBLKTYPE_ERR_IntStat	R/W	Slave Interface Multi Block type Error Status Enable. ■ 0: Disable the generation of Slave Interface Multi Block type Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Slave Interface Multi Block type Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_SLVIF_MULTIBLKTYPE_ERR): Enable the generation of Slave Interface Multi Block type Error Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_SLVIF_MULTIBLKTYPE_ERR): Disable the generation of Slave Interface Multi Block type Error Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
13	Enable_SHADOWREG_OR_LLI_INVALID_ERR_IntStat	R/W	Shadow register or LLI Invalid Error Status Enable. ■ 0: Disable the generation of Shadow Register or LLI Invalid Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Shadow Register or LLI Invalid Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_SHADOWREG_OR_LLI_INVALID_ERR): Enable the generation of Shadow Register or LLI Invalid Error Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_SHADOWREG_OR_LLI_INVALID_ERR): Disable the generation of Shadow Register or LLI Invalid Error Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always

Bits	Name	Access	Description
12	Enable_LLI_WR_SLV_ERR_IntStat	R/W	LLI WRITE Slave Error Status Enable. ■ 0: Disable the generation of LLI WRITE Slave Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of LLI WRITE Slave Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_LLI_WR_SLV_ERR): Enable the generation of LLI WRITE Slave Error Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_LLI_WR_SLV_ERR): Disable the generation of LLI WRITE Slave Error Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
11	Enable_LLI_RD_SLV_ERR_IntStat	R/W	LLI Read Slave Error Status Enable. ■ 0: Disable the generation of LLI Read Slave Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of LLI Read Slave Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_LLI_RD_SLV_ERR): Enable the generation of LLI Read Slave Error Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_LLI_RD_SLV_ERR): Disable the generation of LLI Read Slave Error Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
10	Enable_LLI_WR_DEC_ERR_IntStat	R/W	LLI WRITE Decode Error Status Enable. ■ 0: Disable the generation of LLI WRITE Decode Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of LLI WRITE Decode Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_LLI_WR_DEC_ERR): Enable the generation of LLI WRITE Decode Error Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_LLI_WR_DEC_ERR): Disable the generation of LLI WRITE Decode Error Interrupt in

Bits	Name	Access	Description
			CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
9	Enable_LLI_RD_DEC_ERR_IntStat	R/W	LLI Read Decode Error Status Enable. ■ 0: Disable the generation of LLI Read Decode Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of LLI Read Decode Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_LLI_RD_DEC_ERR): Enable the generation of LLI Read Decode Error Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_LLI_RD_DEC_ERR): Disable the generation of LLI Read Decode Error Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
8	Enable_DST_SLV_ERR_IntStat	R/W	Destination Slave Error Status Enable. ■ 0: Disable the generation of Destination Slave Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Destination Slave Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_DST_SLV_ERR): Enable the generation of Destination Slave Error Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_DST_SLV_ERR): Disable the generation of Destination Slave Error Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
7	Enable_SRC_SLV_ERR_IntStat	R/W	Source Slave Error Status Enable. ■ 0: Disable the generation of Source Slave Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Source Slave Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_SRC_SLV_ERR): Enable the generation of Source Slave Error Interrupt in

Bits	Name	Access	Description
			CH1_INTSTATUSREG. ■ 0x0 (DISABLE_SRC_SLV_ERR): Disable the generation of Source Slave Error Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
6	Enable_DST_DEC_ERR_IntStat	R/W	Destination Decode Error Status Enable. ■ 0: Disable the generation of Destination Decode Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Destination Decode Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_DST_DEC_ERR): Enable the generation of Destination Decode Error Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_DST_DEC_ERR): Disable the generation of Destination Decode Error Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
5	Enable_SRC_DEC_ERR_IntStat	R/W	Source Decode Error Status Enable. ■ 0: Disable the generation of Source Decode Error Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Source Decode Error Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_SRC_DEC_ERR): Enable the generation of Source Decode Error Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_SRC_DEC_ERR): Disable the generation of Source Decode Error Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
4	Enable_DST_TRANSCOMP_IntStat	R/W	Destination Transaction Completed Status Enable. ■ 0: Disable the generation of Destination Transaction complete Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Destination

Bits	Name	Access	Description
			Transaction complete Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_DST_TRANSCOMP): Enable the generation of Destination Transaction complete Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_DST_TRANSCOMP): Disable the generation of Destination Transaction complete Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
3	Enable_SRC_TRANSCOMP_IntStat	R/W	Source Transaction Completed Status Enable. ■ 0: Disable the generation of Source Transaction Complete Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Source Transaction Complete Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_SRC_TRANSCOMP): Enable the generation of Source Transaction Complete Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_SRC_TRANSCOMP): Disable the generation of Source Transaction Complete Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
2	RSVD_DMAC_CHx_INTSTATUS_ENABLEREG_2	R	DMAC Channelx Interrupt Status Register (bit 2) Reserved bit - Read Only Value After Reset: 0x1 Exists: Always
1	Enable_DMA_TFR_DONE_IntStat	R/W	DMA Transfer Done Interrupt Status Enable. ■ 0: Disable the generation of DMA Transfer Done Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of DMA Transfer Done Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_DMA_TFR_DONE): Enable the generation of DMA Transfer Done Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_DMA_TFR_DONE): Disable the

Bits	Name	Access	Description
			generation of DMA Transfer Done Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always
0	Enable_BLOCK_TFR_DONE_IntStat	R/W	Block Transfer Done Interrupt Status Enable. ■ 0: Disable the generation of Block Transfer Done Interrupt in CHx_INTSTATUSREG. ■ 1: Enable the generation of Block Transfer Done Interrupt in CHx_INTSTATUSREG. Values: ■ 0x1 (ENABLE_BLOCK_TFR_DONE): Enable the generation of Block Transfer Done Interrupt in CH1_INTSTATUSREG. ■ 0x0 (DISABLE_BLOCK_TFR_DONE): Disable the generation of Block Transfer Done Interrupt in CH1_INTSTATUSREG. Value After Reset: 0x1 Exists: Always

14.5.2.15 CHx_INTSTATUS (for x = 1; x <= 4)

- Description: Channelx Interrupt Status Register captures the Channelx specific interrupts
- Size: 64 bits
- Offset: 0x188 + (x-1)*0x100
- Exists: Yes

Figure & Table 14-33 Fields for register: CHx_INTSTATUS (for x = 1; x <= 4)

Bits	Name	Access	Description
63:32	RSVD_DMAC_CHx_INTSTATUSREG_32to63	R	DMAC Channelx Specific Interrupt Register (bits 32 to 63) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always Volatile: True
31	CH_ABORTED_IntStat	R	Channel Aborted. This indicates to the software that the corresponding channel in DW_axi_dmac is aborted. ■ 0: Channel is not aborted. ■ 1: Channel is aborted. Error Interrupt is generated if the corresponding bit in

Bits	Name	Access	Description
			CHx_INTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_CH_ABORTED): Channel is aborted. ■ 0x0 (INACTIVE_CH_ABORTED): Channel is not aborted. Value After Reset: 0x0 Exists: Always Volatile: True
30	CH_DISABLED_IntStat	R	Channel Disabled. This indicates to the software that the corresponding channel in DW_axi_dmac is disabled. ■ 0: Channel is not disabled. ■ 1: Channel is disabled. Error Interrupt is generated if the corresponding bit in CHx_INTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_CH_DISABLED): Channel is disabled. ■ 0x0 (INACTIVE_CH_DISABLED): Channel is not disabled. Value After Reset: 0x0 Exists: Always Volatile: True
29	CH_SUSPENDED_IntStat	R	Channel Suspended. This indicates to the software that the corresponding channel in DW_axi_dmac is suspended. ■ 0: Channel is not suspended. ■ 1: Channel is suspended. Error Interrupt is generated if the corresponding bit in CHx_INTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_CH_SUSPENDED): Channel is suspended.

Bits	Name	Access	Description
			■ 0x0 (INACTIVE_CH_SUSPENDED): Channel is not suspended. Value After Reset: 0x0 Exists: Always Volatile: True
28	CH_SRC_SUSPENDED_IntStat	R	Channel Source Suspended. This indicates to the software that the corresponding channel source data transfer in DW_axi_dmac is suspended. ■ 0: Channel source is not suspended. ■ 1: Channel Source is suspended. Error Interrupt is generated if the corresponding bit in CHx_INTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_CH_SRC_SUSPENDED): Channel Source is suspended. ■ 0x0 (INACTIVE_CH_SRC_SUSPENDED): Channel source is not suspended. Value After Reset: 0x0 Exists: Always Volatile: True
27	CH_LOCK_CLEARED_IntStat	R	Channel Lock Cleared. This indicates to the software that the locking of the corresponding channel in DW_axi_dmac is cleared. ■ 0: Channel locking is not cleared. ■ 1: Channel locking is cleared. Channel locking is cleared by DW_axi_dmac during the following situations: ■ Channel locking is cleared and the channel locking settings in CHx_CFG register is reset if DW_axi_dmac disables the channel upon request from software. ■ Channel locking is cleared and the channel locking settings in CHx_CFG register is reset if DW_axi_dmac disables the channel upon receiving error response on the master interface. This bit is cleared to 0 on enabling the channel.

Bits	Name	Access	Description
			Values: ■ 0x1 (ACTIVE_CH_LOCK_CLEARED): Channel Locking is cleared. ■ 0x0 (INACTIVE_CH_LOCK_CLEARED): Channel locking is not cleared, if present. Value After Reset: 0x0 Exists: Always Volatile: True
26:22	RSVD_DMAC_CHx_INTSTATUS REG_22to26	R	DMAC Channelx Specific Interrupt Register (bits 22 to 26) Reserved bits - Read Only Value After Reset: 0x0 Exists: Always Volatile: True
21	SLVIF_WRONHOLD_ERR_IntStat	R	Slave Interface Write On Hold Error. This error occurs if an illegal write operation is performed on a register; this happens if a write operation is performed on a channel register when DW_axi_dmac is in Hold mode. ■ 0: No Slave Interface Write On Hold Errors. ■ 1: Slave Interface Write On Hold Error detected. Error Interrupt is generated if the corresponding bit in CHx_INTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_SLVIF_WRONHOLD_ERR): Slave Interface Write On Hold Error detected. ■ 0x0 (INACTIVE_SLVIF_WRONHOLD_ERR): No Slave Interface Write On Hold Errors. Value After Reset: 0x0 Exists: Always Volatile: True
20	SLVIF_SHADOWREG_WRON_V ALID_ERR_IntStat	R	Shadow Register Write On Valid Error. This error occurs if shadow register based multi-block transfer is enabled and software tries to write to the shadow register when CHx_CTL.ShadowReg_Or_LLI_Valid bit is 1. ■ 0: No Slave Interface Shadow Register Write On

Bits	Name	Access	Description
			Valid Errors. ■ 1: Slave Interface Shadow Register Write On Valid Error detected. Error Interrupt is generated if the corresponding bit in CHx_INTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_SLVIF_SHADOWREG_WRON_VALID_ERR): Slave Interface Shadow Register Write On Valid Error detected. ■ 0x0 (INACTIVE_SLVIF_SHADOWREG_WRON_VALID_ERR): No Slave Interface Shadow Register Write On Valid Errors. Value After Reset: 0x0 Exists: Always Volatile: True
19	SLVIF_WRONCHEN_ERR_IntSta t	R	Slave Interface Write On Channel Enabled Error. This error occurs if an illegal write operation is performed on a register; this happens if a write operation is performed on a register when the channel is enabled and if it is not allowed for the corresponding register as per the DW_axi_dmac specification. ■ 0: No Slave Interface Write On Channel Enabled Errors. ■ 1: Slave Interface Write On Channel Enabled Error detected. Error Interrupt is generated if the corresponding bit in CHx_INTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_SLVIF_WRONCHEN_ERR): Slave Interface Write On Channel Enabled Error detected. ■ 0x0 (INACTIVE_SLVIF_WRONCHEN_ERR): No Slave Interface Write On Channel Enabled Errors. Value After Reset: 0x0 Exists: Always

Bits	Name	Access	Description
			Volatile: True
18	SLVIF_RD2RWO_ERR_IntStat	R	Slave Interface Read to write Only Error. This error occurs if read operation is performed to a Write Only register. ■ 0: No Slave Interface Read to Write Only Errors. ■ 1: Slave Interface Read to Write Only Error detected. Error Interrupt is generated if the corresponding bit in CHx_INTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_SLVIF_RD2RWO_ERR): Slave Interface Read to Write Only Error detected. ■ 0x0 (INACTIVE_SLVIF_RD2RWO_ERR): No Slave Interface Read to Write Only Errors. Value After Reset: 0x0 Exists: Always Volatile: True
17	SLVIF_WR2RO_ERR_IntStat	R	Slave Interface Write to Read Only Error. This error occurs if write operation is performed to a Read Only register. ■ 0: No Slave Interface Write to Read Only Errors. ■ 1: Slave Interface Write to Read Only Error detected. Error Interrupt is generated if the corresponding bit in CHx_INTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_SLVIF_WR2RO_ERR): Slave Interface Write to Read Only Error detected. ■ 0x0 (INACTIVE_SLVIF_WR2RO_ERR): No Slave Interface Write to Read Only Errors. Value After Reset: 0x0 Exists: Always Volatile: True
16	SLVIF_DEC_ERR_IntStat	R	Slave Interface Decode Error.

Bits	Name	Access	Description
			Decode Error generated by DW_axi_dmac during register access. This error occurs if the register access is to invalid address in Channelx register space resulting in error response by DW_axi_dmac slave interface. ■ 0: No Slave Interface Decode errors. ■ 1: Slave Interface Decode Error detected. Error Interrupt is generated if the corresponding bit in CHxINTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_SLVIF_DEC_ERR): Slave Interface Decode Error detected. ■ 0x0 (INACTIVE_SLVIF_DEC_ERR): No Slave Interface Decode errors. Value After Reset: 0x0 Exists: Always Volatile: True
15	RSVD_DMAC_CHx_INTSTATUS REG_15	R	DMAC Channelx Specific Interrupt Register (bit 15) Reserved bit - Read Only Value After Reset: 0x0 Exists: Always Volatile: True
14	SLVIF_MULTIBLKTYPE_ERR_Int Stat	R	Slave Interface Multi Block type Error. This error occurs if multi-block transfer type programmed in CHx_CFG register (SRC_MLTBLK_TYPE and DST_MLTBLK_TYPE) is invalid. This error condition causes the DW_axi_dmac to halt the corresponding channel gracefully; Error Interrupt is generated if the corresponding channel error interrupt mask bit is set to 0 and the channel waits till software writes (any value) to CHx_BLK_TFR_ResumeReqReg to indicate valid multiblock transfer type availability. ■ 0: No Multi-block transfer type Errors. ■ 1: Multi-block transfer type Error detected. Error Interrupt is generated if the corresponding bit in CHx_INTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register.

Bits	Name	Access	Description
			Values: ■ 0x1 (ACTIVE_SLVIF_MULTIBLKTYPE_ERR): Multi-block transfer type Error detected. ■ 0x0 (INACTIVE_SLVIF_MULTIBLKTYPE_ERR): No Multi-block transfer type Errors. Value After Reset: 0x0 Exists: Always Volatile: True
13	SHADOWREG_OR_LLI_INVALID_ERR_IntStat	R	Shadow register or LLI Invalid Error. This error occurs if CHx_CTL.ShadowReg_Or_LLI_Valid bit is seen to be 0 during DW_axi_dmac Shadow Register / LLI fetch phase. This error condition causes the DW_axi_dmac to halt the corresponding channel gracefully; Error Interrupt is generated if the corresponding channel error interrupt mask bit is set to 0 and the channel waits till software writes (any value) to CHx_BLK_TFR_ResumeReqReg to indicate valid Shadow Register availability. In the case of LLI pre-fetching, ShadowReg_Or_LLI_Invalid_ERR Interrupt is not generated even if ShadowReg_Or_LLI_Valid bit is seen to be 0 for the pre-fetched LLI. In this case, DW_axi_dmac re-attempts the LLI fetch operation after completing the current block transfer and generates ShadowReg_Or_LLI_Invalid_ERR Interrupt only if ShadowReg_Or_LLI_Valid bit is still seen to be 0. ■ 0: No Shadow Register / LLI Invalid errors. ■ 1: Shadow Register / LLI Invalid error detected. Error Interrupt is generated if the corresponding bit in CHx_INTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_SHADOWREG_OR_LLI_INVALID_ERR): Shadow Register / LLI Invalid error detected. ■ 0x0 (INACTIVE_SHADOWREG_OR_LLI_INVALID_ERR): No Shadow Register / LLI Invalid errors. Value After Reset: 0x0 Exists: Always Volatile: True

Bits	Name	Access	Description
12	LLI_WR_SLV_ERR_IntStat	R	LLI WRITE Slave Error. Slave Error detected by Master Interface during LLI writeback operation. This error occurs if the slave interface on which LLI resides issues a Slave Error. This error condition causes the DW_axi_dmac to disable the corresponding channel gracefully; the DMAC_ChEnReg.CH_EN1 bit which received the error is set to 0. ■ 0: No LLI write Slave Errors. ■ 1: LLI Write SLAVE Error detected. Error Interrupt is generated if the corresponding bit in CHx_INTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_LLI_WR_SLV): LLI Write SLAVE Error detected. ■ 0x0 (INACTIVE_LLI_WR_SLV): No LLI write Slave Errors. Value After Reset: 0x0 Exists: Always Volatile: True
11	LLI_RD_SLV_ERR_IntStat	R	LLI Read Slave Error. Slave Error detected by Master Interface during LLI read operation. This error occurs if the slave interface on which LLI resides issues a Slave Error. This error condition causes the DW_axi_dmac to disable the corresponding channel gracefully; the DMAC_ChEnReg.CH_EN1 bit which received the error is set to 0. ■ 0: No LLI Read Slave Errors. ■ 1: LLI read Slave Error detected. Error Interrupt is generated if the corresponding bit in CHx_INTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_LLI_RD_SLV_ERR): LLI read Slave Error detected. ■ 0x0 (INACTIVE_LLI_RD_SLV_ERR): No LLI Read Slave

Bits	Name	Access	Description
			Errors. Value After Reset: 0x0 Exists: Always Volatile: True
10	LLI_WR_DEC_ERR_IntStat	R	LLI WRITE Decode Error. Decode Error detected by Master Interface during LLI writeback operation. This error occurs if the access is to invalid address and a Decode Error is returned from interconnect/slave. This error condition causes the DW_axi_dmac to disable the corresponding channel gracefully; the DMAC_ChEnReg.CH_EN1 bit which received the error is set to 0. ■ 0: NO LLI Write Decode Errors. ■ 1: LLI write Decode Error detected. Error Interrupt is generated if the corresponding bit in CHx_INTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_LLI_WR_DEC_ERR): LLI write Decode Error detected. ■ 0x0 (INACTIVE_LLI_WR_DEC_ERR): NO LLI Write Decode Errors. Value After Reset: 0x0 Exists: Always Volatile: True
9	LLI_RD_DEC_ERR_IntStat	R	LLI Read Decode Error. Decode Error detected by Master Interface during LLI read operation. This error occurs if the access is to invalid address and a Decode Error is returned from interconnect/slave. This error condition causes the DW_axi_dmac to disable the corresponding channel gracefully; the DMAC_ChEnReg.CH_EN1 bit which received the error is set to 0. ■ 0: NO LLI Read Decode Errors. ■ 1: LLI Read Decode Error detected. Error Interrupt is generated if the corresponding bit in CHx_INTSTATUS_ENABLEReg is enabled. This bit is cleared to 0 on writing 1 to the corresponding

Bits	Name	Access	Description
			channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVELLI_RD_DEC_ERR_): LLI Read Decode Error detected. ■ 0x0 (INACTIVE_LLI_RD_DEC_ERR): NO LLI Read Decode Errors. Value After Reset: 0x0 Exists: Always Volatile: True
8	DST_SLV_ERR_IntStat	R	Destination Slave Error. Slave Error detected by Master Interface during destination data transfer. This error occurs if the slave interface to which the data is written issues a Slave Error. This error condition causes the DW_axi_dmac to disable the corresponding channel gracefully; the DMAC_ChEnReg.CH_EN bit corresponding to the channel which received the error is set to 0. ■ 0: No Destination Slave Errors. ■ 1: Destination Slave Errors Detected. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_DST_SLV_ERR): Destination Slave Errors Detected. ■ 0x0 (INACTIVE_DST_SLV_ERR): No Destination Slave Errors. Value After Reset: 0x0 Exists: Always Volatile: True
7	SRC_SLV_ERR_IntStat	R	Source Slave Error. Slave Error detected by Master Interface during source data transfer. This error occurs if the slave interface from which the data is read issues a Slave Error. This error condition causes the DW_axi_dmac to disable the corresponding channel gracefully; the DMAC_ChEnReg.CH_EN bit corresponding to the channel which received the error is set to 0. ■ 0: No Source Slave Errors. ■ 1: Source Slave Error Detected.

Bits	Name	Access	Description
			This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_SRC_SLV_ERR): Source Slave Error Detected. ■ 0x0 (INACTIVE_SRC_SLV_ERR): No Source Slave Errors. Value After Reset: 0x0 Exists: Always Volatile: True
6	DST_DEC_ERR_IntStat	R	Destination Decode Error. Decode Error detected by Master Interface during destination data transfer. This error occurs if the access is to invalid address and a Decode Error is returned from interconnect/slave. This error condition causes the DW_axi_dmac to disable the corresponding channel gracefully; the DMAC_ChEnReg.CH_EN bit corresponding to the channel which received the error is set to 0. ■ 0: No destination Decode Errors. ■ 1: Destination Decode Error Detected. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_DST_DEC_ERR): Destination Decode Error Detected. ■ 0x0 (INACTIVE_DST_DEC_ERR): No destination Decode Errors. Value After Reset: 0x0 Exists: Always Volatile: True
5	SRC_DEC_ERR_IntStat	R	Source Decode Error. Decode Error detected by Master Interface during source data transfer. This error occurs if the access is to invalid address and a Decode Error is returned from interconnect/slave. This error condition causes the DW_axi_dmac to disable the corresponding channel gracefully; the DMAC_ChEnReg.CH_EN bit corresponding to the channel which received the error is set to 0.

Bits	Name	Access	Description
			■ 0: No Source Decode Errors. ■ 1: Source Decode Error detected. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (ACTIVE_SRC_DEC_ERR): Source Decode Error detected. ■ 0x0 (INACTIVE_SRC_DEC_ERR): No Source Decode Errors. Value After Reset: 0x0 Exists: Always Volatile: True
4	DST_TRANSCOMP_IntStat	R	Destination Transaction Completed. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register or on enabling the channel (needed when interrupt is not enabled. Values: ■ 0x1 (ACTIVE_DST_TRANSCOMP): Destination transaction is complete. ■ 0x0 (INACTIVE_DST_TRANSCOMP): Destination transaction is not complete. Value After Reset: 0x0 Exists: Always Volatile: True
3	SRC_TRANSCOMP_IntStat	R	Source Transaction Completed. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register or on enabling the channel (needed when interrupt is not enabled. Values: ■ 0x1 (ACTIVE_SRC_TRANSCOMP): Source transaction is complete. ■ 0x0 (INACTIVE_SRC_TRANSCOMP): Source transaction is not complete. Value After Reset: 0x0 Exists: Always Volatile: True

Bits	Name	Access	Description
2	RSVD_DMAC_CHx_INTSTATUS REG_2	R	DMAC Channelx Specific Interrupt Register (bit 2) Reserved bit - Read Only Value After Reset: 0x0 Exists: Always Volatile: True
1	DMA_TFR_DONE_IntStat	R	DMA Transfer Done. This indicates to the software that the DW_axi_dmac has completed the requested DMA transfer. The DW_axi_dmac sets this bit to 1 along with setting CHx_INTSTATUS.BLOCK_TFR_DONE bit to 1 when the last block transfer is completed. ■ 0: DMA Transfer not completed. ■ 1: DMA Transfer Completed. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (DMA_TFR_COMPLETED): DMA Transfer completed. ■ 0x0 (DMA_TFR_NOT_COMPLETE): DMA Transfer not complete. Value After Reset: 0x0 Exists: Always Volatile: True
0	BLOCK_TFR_DONE_IntStat	R	Block Transfer Done. This indicates to the software that the DW_axi_dmac has completed the requested block transfer. The DW_axi_dmac sets this bit to 1 when the transfer is successfully completed. ■ 0: Block Transfer not completed. ■ 1: Block Transfer completed. This bit is cleared to 0 on writing 1 to the corresponding channel interrupt clear bit in CHx_IntClearReg register. Values: ■ 0x1 (BLOCK_TFR_COMPLETED): Block Transfer completed. ■ 0x0 (BLOCK_TFR_NOT_COMPLETE): Block Transfer not complete. Value After Reset: 0x0

Bits	Name	Access	Description
			Exists: Always Volatile: True

14.5.2.16 CHx_INTSIGNAL_ENABLEREG (for x = 1; x <= 4)

- Description: This register contains fields that are used to enable the generation of port level interrupt at the channel level.
- Size: 64 bits
- Offset: 0x190 + (x-1)*0x100
- Exists: Yes

Figure & Table 14-34 Fields for register: CHx_INTSIGNAL_ENABLEREG (for x = 1; x <= 4)

Bits	Name	Access	Description
63:32	RSVD_DMAC_CHx_INTSTATUS_ENABLEREG_32to63	R	DMAC Channelx Interrupt Status Enable Register (bits 32 to 63) Reserved bits - Read Only Value After Reset: 0xffffffff Exists: Always
31	Enable_CH_ABORTED_IntSignal	R/W	Channel Aborted Signal Enable. ■ 0: Disable the propagation of Channel Aborted Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Channel Aborted Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_CH_ABORTED_IntSignal): Enable the propagation of Channel Aborted Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_CH_ABORTED_IntSignal): Disable the propagation of Channel Aborted Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
30	Enable_CH_DISABLED_IntSignal	R/W	Channel Disabled Signal Enable. ■ 0: Disable the propagation of Channel Disabled Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Channel Disabled Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_CH_DISABLED_IntSignal): Enable the

Bits	Name	Access	Description
			propagation of Channel Disabled Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_CH_DISABLED_IntSignal): Disable the propagation of Channel Disabled Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
29	Enable_CH_SUSPENDED_IntSignal	R/W	Channel Suspended Signal Enable. ■ 0: Disable the propagation of Channel Suspended Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Channel Suspended Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_CH_SUSPENDED_IntSignal): Enable the propagation of Channel Suspended Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_CH_SUSPENDED_IntSignal): Disable the propagation of Channel Suspended Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
28	Enable_CH_SRC_SUSPENDED_IntSignal	R/W	Channel Source Suspended Signal Enable. ■ 0: Disable the propagation of Channel Source Suspended Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Channel Source Suspended Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_CH_SRC_SUSPENDED_IntSignal): Enable the propagation of Channel Source Suspended Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_CH_SRC_SUSPENDED_IntSignal): Disable the propagation of Channel Source Suspended Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always

Bits	Name	Access	Description
27	Enable_CH_LOCK_CLEARED_IntSignal	R/W	Channel Lock Cleared Signal Enable. ■ 0: Disable the propagation of Channel Lock Cleared Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Channel Lock Cleared Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_CH_LOCK_CLEARED_IntSignal): Enable the propagation of Channel Lock Cleared Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_CH_LOCK_CLEARED_IntSignal): Disable the propagation of Channel Lock Cleared Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
26:22	RSVD_DMAC_CHx_INTSTATUS_ENABLEREG_22to26	R	DMAC Channelx Interrupt Status Enable Register (bits 22 to 26) Reserved bits - Read Only Value After Reset: 0x1f Exists: Always
21	Enable_SLVIF_WRONHOLD_ERR_IntSignal	R/W	Slave Interface Write On Hold Error Signal Enable. ■ 0: Disable the propagation of Slave Interface Write On Hold Error Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Slave Interface Write On Hold Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_SLVIF_WRONHOLD_ERR_IntSignal): Enable the propagation of Slave Interface Write On Hold Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_SLVIF_WRONHOLD_ERR_IntSignal): Disable the propagation of Slave Interface Write On Hold Error Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
20	Enable_SLVIF_SHADOWREG_WRON_VALID_ERR_IntSignal	R/W	Shadow Register Write On Valid Error Signal Enable. ■ 0: Disable the propagation of Shadow Register Write On Valid Error Interrupt to generate a port

Bits	Name	Access	Description
			level interrupt. ■ 1: Enable the propagation of Shadow register Write On Valid Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_SLVIF_SHADOWREG_WRON_VALID_ERR_IntSignal): Enable the propagation of Shadow register Write On Valid Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_SLVIF_SHADOWREG_WRON_VALID_ERR_IntSignal): Disable the propagation of Shadow Register Write On Valid Error Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
19	Enable_SLVIF_WRONCHEN_ERR_IntSignal	R/W	Slave Interface Write On Channel Enabled Error Signal Enable. ■ 0: Disable the propagation of Slave Interface Write On Channel enabled Error Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Slave Interface Write On Channel enabled Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_SLVIF_WRONCHEN_ERR_IntSignal): Enable the propagation of Slave Interface Write On Channel enabled Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_SLVIF_WRONCHEN_ERR_IntSignal): Disable the propagation of Slave Interface Write On Channel enabled Error Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
18	Enable_SLVIF_RD2RWO_ERR_IntSignal	R/W	Slave Interface Read to write Only Error Signal Enable. ■ 0: Disable the propagation of Slave Interface Read to Write only Error Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Slave Interface Read

Bits	Name	Access	Description
			to Write Only Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_SLVIF_RD2RWO_ERR_IntSignal): Enable the propagation of Slave Interface Read to Write Only Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_SLVIF_RD2RWO_ERR_IntSignal): Disable the propagation of Slave Interface Read to Write only Error Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
17	Enable_SLVIF_WR2RO_ERR_Int Signal	R/W	Slave Interface Write to Read Only Error Signal Enable. ■ 0: Disable the propagation of Slave Interface Write to Read only Error Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Slave Interface Write to Read Only Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_SLVIF_WR2RO_ERR_IntSignal): Enable the propagation of Slave Interface Write to Read Only Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_SLVIF_WR2RO_ERR_IntSignal): Disable the propagation of Slave Interface Write to Read only Error Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
16	Enable_SLVIF_DEC_ERR_IntSig nal	R/W	Slave Interface Decode Error Signal Enable. ■ 0: Disable the propagation of Slave Interface Decode Error Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Slave Interface Decode Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_SLVIF_DEC_ERR_IntSignal): Enable

Bits	Name	Access	Description
			the propagation of Slave Interface Decode Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_SLVIF_DEC_ERR_IntSignal): Disable the propagation of Slave Interface Decode Error Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
15	RSVD_DMAC_CHx_INTSTATUS_ENABLEREG_15	R	DMAC Channelx Interrupt Status Enable Register (bit 15) Reserved bit - Read Only Value After Reset: 0x1 Exists: Always
14	Enable_SLVIF_MULTIBLKTYPE_ERR_IntSignal	R/W	Slave Interface Multi Block type Error Signal Enable. ■ 0: Disable the propagation of Slave Interface Multi Block type Error Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Slave Interface Multi Block type Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_SLVIF_MULTIBLKTYPE_ERR_IntSignal): Enable the propagation of Slave Interface Multi Block type Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_SLVIF_MULTIBLKTYPE_ERR_IntSignal): Disable the propagation of Slave Interface Multi Block type Error Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
13	Enable_SHADOWREG_OR_LLI_INVALID_ERR_IntSignal	R/W	Shadow register or LLI Invalid Error Signal Enable. ■ 0: Disable the propagation of Shadow Register or LLI Invalid Error Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Shadow Register or LLI Invalid Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_SHADOWREG_OR_LLI_INVALID_ERR_IntSignal): Enable the propagation of Shadow Register

Bits	Name	Access	Description
			or LLI Invalid Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_SHADOWREG_OR_LLI_INVALID_ERR_IntSignal): Disable the propagation of Shadow Register or LLI Invalid Error Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
12	Enable_LLI_WR_SLV_ERR_IntSignal	R/W	LLI WRITE Slave Error Signal Enable. ■ 0: Disable the propagation of LLI WRITE Slave Error Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of LLI WRITE Slave Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_LLI_WR_SLV_ERR_IntSignal): Enable the propagation of LLI WRITE Slave Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_LLI_WR_SLV_ERR_IntSignal): Disable the propagation of LLI WRITE Slave Error Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
11	Enable_LLI_RD_SLV_ERR_IntSignal	R/W	LLI Read Slave Error Signal Enable. ■ 0: Disable the propagation of LLI Read Slave Error Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of LLI Read Slave Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_LLI_RD_SLV_ERR_IntSignal): Enable the propagation of LLI Read Slave Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_LLI_RD_SLV_ERR_IntSignal): Disable the propagation of LLI Read Slave Error Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
10	Enable_LLI_WR_DEC_ERR_IntSignal	R/W	LLI WRITE Decode Error Signal Enable. ■ 0: Disable the propagation of LLI WRITE Decode

Bits	Name	Access	Description
			Error Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of LLI WRITE Decode Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_LLI_WR_DEC_ERR_IntSignal): Enable the propagation of LLI WRITE Decode Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_LLI_WR_DEC_ERR_IntSignal): Disable the propagation of LLI WRITE Decode Error Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
9	Enable_LLI_RD_DEC_ERR_IntSignal	R/W	LLI Read Decode Error Signal Enable. ■ 0: Disable the propagation of LLI Read Decode Error Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of LLI Read Decode Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_LLI_RD_DEC_ERR_IntSignal): Enable the propagation of LLI Read Decode Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_LLI_RD_DEC_ERR_IntSignal): Disable the propagation of LLI Read Decode Error Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
8	Enable_DST_SLV_ERR_IntSignal	R/W	Destination Slave Error Signal Enable. ■ 0: Disable the propagation of Destination Slave Error Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Destination Slave Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_DST_SLV_ERR_IntSignal): Enable the propagation of Destination Slave Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_DST_SLV_ERR_IntSignal): Disable the propagation of Destination Slave Error Interrupt to generate a port level interrupt. Value After Reset: 0x1

Bits	Name	Access	Description
			Exists: Always
7	Enable_SRC_SLV_ERR_IntSignal	R/W	Source Slave Error Signal Enable. ■ 0: Disable the propagation of Source Slave Error Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Source Slave Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_SRC_SLV_ERR_IntSignal): Enable the propagation of Source Slave Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_SRC_SLV_ERR_IntSignal): Disable the propagation of Source Slave Error Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
6	Enable_DST_DEC_ERR_IntSignal	R/W	Destination Decode Error Signal Enable. ■ 0: Disable the propagation of Destination Decode Error Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Destination Decode Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_DST_DEC_ERR_IntSignal): Enable the propagation of Destination Decode Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_DST_DEC_ERR_IntSignal): Disable the propagation of Destination Decode Error Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
5	Enable_SRC_DEC_ERR_IntSignal	R/W	Source Decode Error Signal Enable. ■ 0: Disable the propagation of Source Decode Error Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Source Decode Error Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_SRC_DEC_ERR_IntSignal): Enable the propagation of Source Decode Error Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_SRC_DEC_ERR_IntSignal): Disable the

Bits	Name	Access	Description
			propagation of Source Decode Error Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
4	Enable_DST_TRANSCOMP_IntSignal	R/W	Destination Transaction Completed Signal Enable. ■ 0: Disable the propagation of Destination Transaction complete Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Destination Transaction complete Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_DST_TRANSCOMP_IntSignal): Enable the propagation of Destination Transaction complete Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_DST_TRANSCOMP_IntSignal): Disable the propagation of Destination Transaction complete Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
3	Enable_SRC_TRANSCOMP_IntSignal	R/W	Source Transaction Completed Signal Enable. ■ 0: Disable the propagation of Source Transaction Complete Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Source Transaction Complete Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_SRC_TRANSCOMP_IntSignal): Enable the propagation of Source Transaction Complete Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_SRC_TRANSCOMP_IntSignal): Disable the propagation of Source Transaction Complete Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
2	RSVD_DMAC_CHx_INTSTATUS_	R	DMAC Channelx Interrupt Status Enable Register (bit 2)

Bits	Name	Access	Description
	ENABLEREG_2		Reserved bit - Read Only Value After Reset: 0x1 Exists: Always
1	Enable_DMA_TFR_DONE_IntSignal	R/W	DMA Transfer Done Interrupt Signal Enable. ■ 0: Disable the propagation of DMA Transfer Done Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of DMA Transfer Done Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_DMA_TFR_DONE_IntSignal): Enable the propagation of DMA Transfer Done Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_DMA_TFR_DONE_IntSignal): Disable the propagation of DMA Transfer Done Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always
0	Enable_BLOCK_TFR_DONE_IntSignal	R/W	Block Transfer Done Interrupt Signal Enable. ■ 0: Disable the propagation of Block Transfer Done Interrupt to generate a port level interrupt. ■ 1: Enable the propagation of Block Transfer Done Interrupt to generate a port level interrupt. Values: ■ 0x1 (ENABLE_BLOCK_TFR_DONE_IntSignal): Enable the propagation of Block Transfer Done Interrupt to generate a port level interrupt. ■ 0x0 (DISABLE_BLOCK_TFR_DONE_IntSignal): Disable the propagation of Block Transfer Done Interrupt to generate a port level interrupt. Value After Reset: 0x1 Exists: Always

14.5.2.17 CHx_INTCLEARREG (for x = 1; x <= 4)

- Description: Writing 1 to specific field will clear the corresponding field in Channelx Interrupt Status Register (CHx_IntStatusReg).
- Size: 64 bits
- Offset: 0x198 + (x-1)*0x100
- Exists: Yes

Figure & Table 14-35 Fields for register: CHx_INTCLEARREG (for x = 1; x <= 4)

Bits	Name	Access	Description
63:32	RSVD_DMAC_CHx_INTCLEARREG_32to63	W	DMAC Channelx Interrupt Clear Register (bits 32 to 63) Reserved bit - Read Only Value After Reset: 0x0 Exists: Always
31	Clear_CH_ABORTED_IntStat	W	Channel Aborted Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_CH_ABORTED): Clear the CH_ABORTED interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
30	Clear_CH_DISABLED_IntStat	W	Channel Disabled Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_CH_DISABLED): Clear the CH_DISABLED interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
29	Clear_CH_SUSPENDED_IntStat	W	Channel Suspended Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_CH_SUSPENDED): Clear the CH_SUSPENDED interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
28	Clear_CH_SRC_SUSPENDED_IntStat	W	Channel Source Suspended Interrupt Clear Bit. This bit is used to clear the corresponding channel

Bits	Name	Access	Description
			interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_CH_SRC_SUSPENDED): Clear the CH_SRC_SUSPENDED interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
27	Clear_CH_LOCK_CLEARED_IntStat	W	Channel Lock Cleared Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_CH_LOCK_CLEARED): Clear the CH_LOCK_CLEARED interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
26:22	RSVD_DMAC_CHx_INTCLEARREG_22to26	W	DMAC Channelx Interrupt Clear Register (bits 22to26) Reserved bit - Read Only Value After Reset: 0x0 Exists: Always
21	Clear_SLVIF_WRONHOLD_ERR_IntStat	W	Slave Interface Write On Hold Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_SLVIF_WRONHOLD_ERR): Clear the SLVIF_WRONHOLD_ERR interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
20	Clear_SLVIF_SHADOWREG_WRON_VALID_ERR_IntStat	W	Shadow Register Write On Valid Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values:

Bits	Name	Access	Description
			■ 0x1 (CLEAR_SLVIF_SHADOWREG_WRON_VALID_ERR): Clear the SLVIF_SHADOWREG_WRON_VALID_ERR interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
19	Clear_SLVIF_WRONCHEN_ERR_IntStat	W	Slave Interface Write On Channel Enabled Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_SLVIF_WRONCHEN_ERR): Clear the SLVIF_WRONCHEN_ERR interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
18	Clear_SLVIF_RD2RWO_ERR_IntStat	W	Slave Interface Read to write Only Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_SLVIF_RD2RWO_ERR): Clear the SLVIF_RD2RWO_ERR interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
17	Clear_SLVIF_WR2RO_ERR_IntStat	W	Slave Interface Write to Read Only Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_SLVIF_WR2RO_ERR): Clear the SLVIF_WR2RO_ERR interrupt in the Interrupt Status Register (CH1_IntStatusReg).

Bits	Name	Access	Description
			■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
16	Clear_SLVIF_DEC_ERR_IntStat	W	Slave Interface Decode Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_SLVIF_DEC_ERR): Clear the SLVIF_DEC_ERR interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
15	RSVD_DMAC_CHx_INTCLEARREG_15	W	DMAC Channelx Interrupt Clear Register (bit 15) Reserved bit - Read Only Value After Reset: 0x0 Exists: Always
14	Clear_SLVIF_MULTIBLKTYPE_ERR_IntStat	W	Slave Interface Multi Block type Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_SLVIF_MULTIBLKTYPE_ERR): Clear the SLVIF_MULTIBLKTYPE_ERR interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
13	Clear_SHADOWREG_OR_LLI_INVALID_ERR_IntStat	W	Shadow register or LLI Invalid Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_SHADOWREG_OR_LLI_INVALID_ERR): Clear the SHADOWREG_OR_LLI_INVALID_ERR interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0

Bits	Name	Access	Description
			Exists: Always
12	Clear_LLI_WR_SLV_ERR_IntStat	W	LLI WRITE Slave Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_LLI_WR_SLV_ERR): Clear the LLI_WR_SLV_ERR interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
11	Clear_LLI_RD_SLV_ERR_IntStat	W	LLI Read Slave Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_LLI_RD_SLV_ERR): Clear the LLI_RD_SLV_ERR interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
10	Clear_LLI_WR_DEC_ERR_IntSta t	W	LLI WRITE Decode Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_LLI_WR_DEC_ERR): Clear the LLI_WR_DEC_ERR interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
9	Clear_LLI_RD_DEC_ERR_IntStat	W	LLI Read Decode Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_LLI_RD_DEC_ERR): Clear the LLI_RD_DEC_ERR interrupt in the Interrupt Status

Bits	Name	Access	Description
			Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
8	Clear_DST_SLV_ERR_IntStat	W	Destination Slave Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_DST_SLV_ERR): Clear the DST_SLV_ERR interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
7	Clear_SRC_SLV_ERR_IntStat	W	Source Slave Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_SRC_SLV_ERR): Clear the SRC_SLV_ERR interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
6	Clear_DST_DEC_ERR_IntStat	W	Destination Decode Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_DST_DEC_ERR): Clear the DST_DEC_ERR interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
5	Clear_SRC_DEC_ERR_IntStat	W	Source Decode Error Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG.

Bits	Name	Access	Description
			Values: ■ 0x1 (CLEAR_SRC_DEC_ERR): Clear the SRC_DEC_ERR interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
4	Clear_DST_TRANSCOMP_IntSta t	W	Destination Transaction Completed Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_DST_TRANSCOMP): Clear the DST_TRANSCOMP interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
3	Clear_SRC_TRANSCOMP_IntSta t	W	Source Transaction Completed Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_SRC_TRANSCOMP): Clear the SRC_TRANSCOMP interrupt in the Interrupt Status Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
2	RSVD_DMAC_CHx_INTCLEARR EG_2	W	DMAC Channelx Interrupt Clear Register (bit 2) Reserved bit - Read Only Value After Reset: 0x0 Exists: Always
1	Clear_DMA_TFR_DONE_IntStat	W	DMA Transfer Done Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CHx_INTSTATUSREG. Values: ■ 0x1 (CLEAR_DMA_TFR_DONE): Clear the DMA_TFR_DONE interrupt in the Interrupt Status

Bits	Name	Access	Description
			Register (CH1_IntStatusReg). ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always
0	Clear_BLOCK_TFR_DONE_IntStat	W	Block Transfer Done Interrupt Clear Bit. This bit is used to clear the corresponding channel interrupt status bit in CH1_INTSTATUSREG. Values: ■ 0x1 (CLEAR_BLOCK_TFR_DONE): Clear the interrupt in the Interrupt Status Register (CHx_IntStatusReg). Writing a 1 to this register field clears the corresponding bit in the CHx_IntStatusReg register. ■ 0x0 (NO_ACTION): Inactive signal. No action taken. Value After Reset: 0x0 Exists: Always

15 PVT

15.1 Overview

PVT monitors provide real time information about performance around each chip, which enable optimization schemes to be implemented. The optimization schemes can target maximizing processing performance, minimizing power consumption or maximizing device lifetime or a combination of these in the presence of those difficult challenges. Not all regions of large chips are the same. Some regions will have faster process performance and do not need the full process guard band. Similarly, with temperature, some regions are likely to run hotter or cooler than others. By including a fabric of PVT sensors at key points around a chip, real time information can be derived, which enables processing performance, power consumption and/or reliability to be optimized.

The process detector circuit provides means to detect the process variation brought about by manufacturing variability and drift of advanced node core digital MOS devices. The process detector can be used to enable a continuous DVFS optimization system, monitor manufacturing variations on and if required, across the chip, gate delay measurements, critical path analysis, critical voltage analysis and to monitor silicon 'ageing'. The process detector is supplied with 6 embedded delay chain structures that can be used to assess silicon speed.

The voltage monitor is a low power self-contained IP block specially designed to monitor differential voltage levels within the core logic voltage domains. The block includes a single step production test calibration capability to increase accuracy, which requires no knowledge of die temperature.

The temperature sensor is a high precision low power junction temperature sensor that has been developed to be embedded into ASIC designs. The block can be used uncalibrated or for higher accuracy, using one- or two-point temperature calibration. Typical temperature sensor uses include thermal management, clock speed optimization, power management and silicon characterization.

15.2 Main Features

- 2 embedded temperature sensors
- ±3℃ uncalibrated accuracy
- ±1.25℃ calibrated accuracy
- 12-bit resolution (10-bit and 8-bit alternatives at lower accuracy)
- 1 embedded voltage sensor with 15 channels
- ±1% (target) uncalibrated accuracy
- ±0.6% (target) calibrated accuracy
- up to 14-bit resolution
- 11 embedded process detector sensors
- Measurement for thin oxide MOS speed

15.3 Function Description

15.3.1 Positions of PVT Sensors in Chip

Inside the chip, there are 2 temperature sensors, 1 voltage monitor with 16 channels, 11 process detectors. The connections or positions of these sensors are shown as below:

Figure & Table 15-1 Sensor positions inside chip

Sensor	Position
Process detector: PD0	Beside C910 CPU core
Process detector: PD1	Beside C910 memory
Process detector: PD2	Inside of GPU
Process detector: PD3	Inside of VO_SUBSYS
Process detector: PD4	Inside of VI_SUBSYS
Process detector: PD5	Inside of top logic
Process detector: PD6	Inside of VENC
Process detector: PD7	Inside of VP_SUBSYS
Process detector: D8	Inside of DDR_SUBSYS
Process detector: PD9	Inside of DDR_SUBSYS
Process detector: PD10	Inside of AON_SUBSYS
VM0 – CH0	External PAD input: PVT_VIN_HI/PVT_VIN_LO
VM0 – CH1	Power supply for C910 core 0
VM0 – CH2	Power supply for C910 core 1
VM0 – CH3	Power supply for C910 core 2
VM0 – CH4	Power supply for C910 core 3
VM0 – CH5	Power supply for C910 top logic
VM0 – CH6	Power supply for DDR
VM0 – CH7	Power supply for DDR
VM0 – CH8	Power supply for NPU
VM0 – CH9	Power supply for GPU
VM0 – CH10	Power supply for DSP0
VM0 – CH11	Power supply for DSP1

Sensor	Position
VM0 - CH12	Power supply for ISP
VM0 - CH13	Power supply for top logic
VM0 - CH14	Power supply for AON_SUBSYS logic
TS0	C910 CPU
TS1	DDR

15.3.2 Process Detector

The process detector is used to detect the process variation brought about by manufacturing variability and drift of advanced node core digital MOS devices, monitor manufacturing variations on and if required, across the chip, gate delay measurements, critical path analysis, critical voltage analysis and to monitor silicon 'ageing'. The process detector is supplied with 6 embedded delay chain structures that can be used to assess silicon speed.
The digital output is converted to frequency by using the following equation:

$$F_{Loop} = \frac{N_{BS} * A * B * F_{CLK}}{W}$$

Where:

- F_{loop}: Frequency of oscillation of the delay loop structure
- N_{BS}: Output data from PD
- A: Pre-scaler divide ratio A, set by PD module configuration
- B: Pre-scaler divide ratio B: 4
- F_{CLK}: Frequency of input clock signal
- W: Size of the counting widow, set by PD module configuration

If individual gate delay speed is required, this is calculated using the following equation:

$$Gate_{Delay} = \frac{1}{F_{Loop} * 2 * N_{Gates}}$$

Where:

- $Gates_{Delay}$: Gate delay (in seconds) of the individual delay element
- F_{loop}: Frequency of oscillation of the delay loop structure
- N_{gates}: The number of elements in the delay loop structure: 91

15.3.2.1 Process Detector Configuration Registers

15.3.2.1.1 Output Control Register (cfg1)

Figure & Table 15-2 Configure register 1 in process detector

7	6	5	4	3	2	1	0
Reserved			ser_mode	pri_mode		sec_mode	

Description		cfg1[3:2]	cfg1[1:0]	Output Mode
Process Detector Mode		00	00	Process Speed
			01	Undefined
			10	
			11	
Fault Debug Mode		01	00	Fault Word
			01	Undefined
			10	
			11	
Signature Mode	Direct Mode	10	00	12'hBA2
	Direct Mode - Inverted		01	12'h45D
	Conversion Mode		10	12'hBA2
	Conversion Mode - Inverted		11	12'h45D
Undefined		11		-

15.3.2.1.2 Port Control Register (cfg2)

Figure & Table 15-3 Configure register 2 in process detector

7	6	5	4	3	2	1	0
port_sel							

Description	cfg2[7:5]	Pre-scale 'B'	Ngates
No delay chain selected	000	-	-
SVT 16nm thin oxide delay chain	001	4	91
LVT 16nm thin oxide delay chain	010	4	91
ULVT 16nm thin oxide delay chain	011	4	91
SVT 20nm thin oxide delay chain	100	4	91
LVT 20nm thin oxide delay chain	101	4	91
ULVT 20nm thin oxide delay chain	110	4	91

15.3.2.1.3 Algorithm Control Register (cfg3)

Figure & Table 15-4 Configure register 3 in process detector

7	6	5	4	3	2	1	0
count_win_size (W)				pre_scale_div (A)			

cfg3[7:4]	Count Win 'W'
0000	255
0001	127
0010	63
0011	31
cfg3[7:4]	**Count Win 'W'**
0000	4
0001	8
0010	16
0011	1

15.3.3 Voltage Monitor

This is the 'basic' conversion of data to measured voltage. It does not require any calibration or offset correction. The digital output (N) is converted to voltage (V) by using the following equation:

$$V = \frac{VREF}{5} * \left(\frac{6 * N}{2^{14}} - \frac{3}{2^R} - 1\right)$$

Where:

- V: Measured voltage [V]
- N: Value on dout at the end of conversion
- VREF: Reference value: 1.2077
- R: Resolution selected, e.g. 8, 10, 12 or 14

This can be re-arranged for a given resolution setting as:

$$V = K_1 * N - Offset_1$$

Where K_1 and $Offset_1$ are pre-computed.

$$K_1 = \frac{VREF}{5} * \frac{6}{2^{14}}$$

$$Offset_1 = \frac{VREF}{5} * \left(\frac{3}{2^R} + 1\right)$$

15.3.3.1 Voltage Monitor Registers

15.3.3.1.1 Output Control Register (cfg1)

Figure & Table 15-5 Configure register 1 in voltage monitor

7	6	5	4	3	2	1	0
Reserved	resolution		ser_mode	pri_mode		sec_mode	

Description		cfg1[3:2]	cfg1[1:0]	Output Mode
Voltage Monitor Mode		00	00	Voltage Measurement
			01	Undefined
			10	
			11	
Status Mode		01	00	Status Word
			01	Undefined
			10	
			11	
Signature Mode	Direct Mode	10	00	12'h30BC
	Direct Mode - Inverted		01	12'h0F43
	Conversion Mode		10	12'h30BC
	Conversion Mode - Inverted		11	12'h0F43
Undefined		11		-

Description	cfg1[6:5]
14-bit resolution	00
12-bit resolution	01
10-bit resolution	10
8-bit resolution	11

15.3.3.1.2 Input Control Register (cfg2)

Figure & Table 15-6 Configure register 2 in voltage monitor

7	6	5	4	3	2	1	0
ext_ref	Reserved		input_sel				

Description	cfg2[4:0]	Comment
Input select	00000	External PAD input: PVT_VIN_HI/PVT_VIN_LO

	00001	Power supply for C910 core 0
	00010	Power supply for C910 core 1
	00011	Power supply for C910 core 2
	00100	Power supply for C910 core 3
	00101	Power supply for C910 top logic
	00110	Power supply for DDR
	00111	Power supply for DDR
	01000	Power supply for NPU
	01001	Power supply for GPU
	01010	Power supply for DSP0
	01011	Power supply for DSP1
	01100	Power supply for ISP
	01101	Power supply for top logic
	01110	Power supply for AON_SUBSYS logic
	1xxxx	VDD and VSS of current VM sensor
Description	**cfg2[7]**	**Comment**
Voltage Reference Select	0	Internal reference
	1	External reference

15.3.4 Temperature Sensor

Digital output is converted to a temperature reading by using the following equation:

$$Temp(C) = A + B * Eq_{bs} + C * F_{clkm}$$

Where:

$$Eq_{bs} = \frac{N_{bs}}{cal5} - 0.5$$

$$F_{clkm} = Fclk\ (in\ MHz)$$

Where:

- Temp: Temperature in degrees centigrade
- NBS: Output (digital output, dout)
- A: 42.74
- B: 220.5
- C: -0.16
- cal5: 4094

15.3.4.1 Temperature Sensor Registers

15.3.4.1.1 Output Control Register (cfg)

Figure & Table 15-7 Configure register in temperature sensor

7	6	5	4	3	2	1	0
resolution			ser_mode	conv_mode			

Description		cfg[3:0]	Output Mode
Process Detector Mode		0000	Temperature, using A & B
		0001	Temperature, using G & H
Signature Mode	Direct Mode	1000	12'hB32
	Direct Mode - Inverted	1001	12'h4CD
	Conversion Mode	1010	12'hB32
	Conversion Mode - Inverted	1011	12'h4CD

Description	cfg[7:5]	Accuracy Degradation	Comments
12-bit resolution	000	-	On dout[11:0]
10-bit resolution	001	±0.4℃	On dout[11:2]
8-bit resolution	010	±1.5℃	On dout[11:4]

15.4 Usage

15.4.1 PVT Alive

1. Read the PVT_COMP_ID register and check whether the return value is 0x9B487060. Refer to the register description for details.
2. Read the PVT_IP_CFG register and check whether the return value is 0x10010B02. Refer to the register description for details.
3. Read the PVT_ID_NUM register and check whether the return value is 0x12345678. Refer to the register description for details.
4. Read the PVT_TM_SCRATCH register and check whether the reset default value of the register is 0x0.
5. Write a random value to the PVT_TM_SCRATCH register.
6. Read the PVT_TM_SCRATCH register and check whether the return value is the random value written in the previous step.

15.4.2 PVT Clock Configuration

The input clocks of PD, VM, and TS are the same and come from AON_SUBSYS. It is necessary to know the clock configuration in AON_SUBSYS and understand the input clock frequency of PVT sensor. The working frequency of PD, VM, and TS is the frequency division of the input clock and the clock frequency after frequency division is required to be 4MHz-8MHz. PD, VM, and TS have their own divider registers and configuration of the divider registers has certain requirements. There are CLK_SYNTH_SYNC, CLK_SYNTH_HI, and CLK_SYNTH_LO in the divider register.
The working frequency of the sensor: Fclk = Fsys/((CLK_SYNTH_HI + 1) + (CLK_SUNTH_LO + 1))
Refer to the register description for configuration of the CLK_SYNTH_HOLD register.

15.4.3 PVT Run Once

15.4.3.1 PD

1. Write 0x0 to the PD_CMN_SDIF_HALT register, release PD.
2. Write 0x0 to the PD_CMN_SDIF_DISABLE register, enable PD.
3. Set the PD_CMN_CLK_SYNTH register, configure the frequency division of PD clock. Refer to the previous chapter for details.
4. Set PD_CMN_SDIF = 0x88000002, release PD reset.
5. Set PD_CMN_SDIF = 0x89102010, configure PD channels, different channels correspond to oscillation loops formed by different devices.
6. Set PD_CMN_SDIF = 0x88000106, configure PD working mode to run once.
7. Read the PD_00_SDIF_DONE register until the value is 0, indicating that the PD sampling is completed.
8. Read the corresponding value according to the previously selected channel, such as reading the PD_00_SDIF_DATA register for the corresponding channel 1.
9. Convert the read value into a frequency value according to the PD conversion formula.

NOTE

Every time you set the PD_CMN_SDIF register, you need to read the PD_CMN_SDIF_STATUS register and check if [0] is 0.

15.4.3.2 VM

1. Write 0x0 to the VM_CMN_SDIF_HALT register, release VM.
2. Write 0x0 to the VM_CMN_SDIF_DISABLE register, enable VM.
3. Set the VM_CMN_CLK_SYNTH register and configure the VM clock frequency division. Refer to the previous chapter for details.
4. Set VM_CMN_SDIF = 0x88000402, release VM reset.
5. Set VM_CMN_SDIF = 0x89017000, configure VM sampling resolution and sampling channel.
6. Set VM_CMN_SDIF = 0x88000506, configure VM working mode to run once.

7. Read the VM_00_SDIF_DONE register until the value is 0, indicating that the VM sampling is completed.
8. Read the corresponding value according to the previously selected channel, such as reading the VM_00_CH_00_SDIF_DATA register for the corresponding channel 1.
9. Convert the read value into a frequency value according to the VM conversion formula.

NOTE

Every time you set the VM_CMN_SDIF register, you need to read the VM_CMN_SDIF_STATUS register and check if [0] is 0.

15.4.3.3 TS

1. Write 0x0 to the TS_CMN_SDIF_HALT register, release TS.
2. Write 0x0 to the TS_CMN_SDIF_DISABLE register, enable TS.
3. Set the TS_CMN_CLK_SYNTH register, configure the TS clock frequency division. Refer to the previous chapter for details.
4. Set TS_CMN_SDIF = 0x89000040, configure TS sampling to 8bit mode.
5. Set TS_CMN_SDIF = 0x8D000200, configure TS power up delay time to 200 cycles.
6. Set TS_CMN_SDIF = 0x88000105, configure TS working mode to run once.
7. Read the TS_00_SDIF_DONE register until the value is 0, indicating that TS sampling is completed.
8. Read the TS_00_SDIF_DATA register to get TS sampling data.
9. Convert the read value into a temperature value according to the TS conversion formula.

NOTE

Every time you set the TS_CMN_SDIF register, you need to read the TS_CMN_SDIF_STATUS register and check if [0] is 0.

15.5 Register Description

15.5.1 Register Bank

Figure & Table 15-8 Register bank start address

Register Bank	C910 Start Address	E902 Start Address
Common registers	0xFFFFF4E000	0xFFF4E000
Interrupt registers	0xFFFFF4E040	0xFFF4E040
TS common registers	0xFFFFF4E080	0xFFF4E080
TS0 registers	0xFFFFF4E0C0	0xFFF4E0C0
TS1 registers	0xFFFFF4E100	0xFFF4E100
PD common registers	0xFFFFF4E180	0xFFF4E180
PD0 registers	0xFFFFF4E1C0	0xFFF4E1C0

Register Bank	C910 Start Address	E902 Start Address
PD1 registers	0xFFFFF4E200	0xFFF4E200
PD2 registers	0xFFFFF4E240	0xFFF4E240
PD3 registers	0xFFFFF4E280	0xFFF4E280
PD4 registers	0xFFFFF4E2C0	0xFFF4E2C0
PD5 registers	0xFFFFF4E300	0xFFF4E300
PD6 registers	0xFFFFF4E340	0xFFF4E340
PD7 registers	0xFFFFF4E380	0xFFF4E380
PD8 registers	0xFFFFF4E3C0	0xFFF4E3C0
PD9 registers	0xFFFFF4E400	0xFFF4E400
PD10 registers	0xFFFFF4E440	0xFFF4E440
VM common registers	0xFFFFF4E800	0xFFF4E800
VM0 registers	0xFFFFF4EA00	0xFFF4EA00

15.5.2 Register Memory Map

Figure & Table 15-9 Register memory map

Register	Offset	Description	Section/Page
PVT_COMP_ID	0x0000	PVT controller ID and revision	15.5.3.1/885
PVT_IP_CFG	0x0004	PVT controller module configuration	15.5.3.2/885
PVT_ID_NUM	0x0008	PVT customer defined controller information	15.5.3.3/886
PVT_TM_SCRATCH	0x000c	PVT scratch test register	15.5.3.4/886
PVT_REG_LOCK	0x0010	PVT soft lock register. Any write to register locks certain controllers' registers. Unlocked by writing 0x1ACCE551.	15.5.3.5/886
PVT_LOCK_STATUS	0x0014	PVT lock status. Reading returns the current lock status.	15.5.3.6/887
PVT_TAM_STATUS	0x0018	PVT test access status. Read of register indicates that the TAM has been active.	15.5.3.7/887
PVT_TAM_CLEAR	0x001c	PVT test access clear. Write to this register clears the TAM status register.	15.5.3.8/887
PVT_TMR_CTRL	0x0020	PVT timer control register. R/W to set timers	15.5.3.9/888

Register	Offset	Description	Section/Page
		behavior.	
PVT_TMR_STATUS	0x0024	PVT timer status register. Read of register returns timer status if timer is enabled.	15.5.3.10/888
PVT_TMR_IRQ_CLEAR	0x0028	PVT timer IRQ clear register. Write to register clears timer IRQ.	15.5.3.11/888
PVT_TMR_IRQ_TEST	0x002c	PVT timer IRQ test register. Write to register will trigger a timer IRQ if timer IRQ enabled.	15.5.3.12/889
IRQ_EN	0x0040	PVT master IRQ register, enables IRQ from the module blocks and timer.	15.5.3.13/889
IRQ_TR_MASK	0x0050	PVT master IRQ mask register, allows masking of Timer IRQ. Write 1 to mask IRQ source.	15.5.3.14/890
IRQ_TS_MASK	0x0054	PVT master IRQ mask register, allows masking of TS IRQ. Write 1 to mask IRQ source.	15.5.3.15/890
IRQ_VM_MASK	0x0058	PVT master IRQ mask register, allows masking of VM IRQ. Write 1 to mask IRQ source.	15.5.3.16/890
IRQ_PD_MASK	0x005c	PVT master IRQ mask register, allows masking of PD IRQ. Write 1 to mask IRQ source.	15.5.3.17/891
IRQ_TR_STATUS	0x0060	PVT master IRQ status register. Reading gives Timer IRQ status (after mask, if applied).	15.5.3.18/891
IRQ_TS_STATUS	0x0064	PVT master IRQ status register. Reading gives TS IRQ status (after masking, if applied).	15.5.3.19/891
IRQ_VM_STATUS	0x0068	PVT master IRQ status register. Reading gives VM IRQ status (after masking, if applied).	15.5.3.20/892
IRQ_PD_STATUS	0x006c	PVT master IRQ status register. Reading gives PD IRQ status (after masking, if applied).	15.5.3.21/892
IRQ_TR_RAW	0x0070	PVT master IRQ raw status register. Reading gives Timer IRQ status no masking.	15.5.3.22/892
IRQ_TS_RAW	0x0074	PVT master IRQ raw status register. Reading gives TS IRQ status no masking.	15.5.3.23/893

Register	Offset	Description	Section/Page
IRQ_VM_RAW	0x0078	PVT master IRQ raw status register. Reading gives VM IRQ status no masking.	15.5.3.24/893
IRQ_PD_RAW	0x007c	PVT master IRQ raw status register. Reading gives PD IRQ status no masking.	15.5.3.25/893
TS_CMN_CLK_SYNTH	0x0080	TS clock synthesiser control register	15.5.3.26/894
TS_CMN_SDIF_DISABLE	0x0084	TS SDIF disable (active high). When asserted completely disables the selected TS instance(s), by forcing the TS macro clock and reset low.	15.5.3.27/894
TS_CMN_SDIF_STATUS	0x0088	TS SDIF status register	15.5.3.28/895
TS_CMN_SDIF	0x008c	TS SDIF write data register	15.5.3.29/895
TS_CMN_SDIF_HALT	0x0090	TS SDIF halt register. Halts all SDIF data transfer and resets SDIF slave.	15.5.3.30/896
TS_CMN_SDIF_CTRL	0x0094	TS SDIF programming inhibit (active high). When asserted inhibits serial programming of the selected TS instance(s).	15.5.3.31/896
TS_CMN_SMPL_CTRL	0x00a0	TS SDIF sample counter control	15.5.3.32/897
TS_CMN_SMPL_CLR	0x00a4	TS SDIF sample counter clear	15.5.3.33/897
TS_CMN_SMPL_CNT	0x00a8	TS SDIF sample counter current value	15.5.3.34/898
TS_00_IRQ_ENABLE	0x00c0	TS-00 IRQ enable register, enables individual IRQ sources from the TS.	15.5.3.35/898
TS_00_IRQ_STATUS	0x00c4	TS-00 IRQ status register, reports status of individual IRQ sources from the TS.	15.5.3.36/899
TS_00_IRQ_CLEAR	0x00c8	TS-00 IRQ clear register, clears individual IRQ sources from the TS.	15.5.3.37/899
TS_00_IRQ_TEST	0x00cc	TS-00 IRQ test register. Write to register will trigger a TS IRQ if the IRQ enabled.	15.5.3.38/900
TS_00_SDIF_RDATA	0x00d0	TS-00 read data register	15.5.3.39/901
TS_00_SDIF_DONE	0x00d4	TS-00 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.	15.5.3.40/901
TS_00_SDIF_DATA	0x00d8	TS-00 SDIF sample data register	15.5.3.41/901
TS_00_ALARMA_CFG	0x00e0	TS-00 Alarm A configuration	15.5.3.42/902
TS_00_ALARMB_CFG	0x00e4	TS-00 Alarm B configuration	15.5.3.43/902

Register	Offset	Description	Section/Page
TS_00_SMPL_HILO	0x00e8	TS-00 sample max/min high/low value	15.5.3.44/903
TS_00_HILO_RESET	0x00ec	TS-00 reset sample high/low register	15.5.3.45/903
TS_01_IRQ_ENABLE	0x0100	TS-01 IRQ enable register, enables individual IRQ sources from the TS.	15.5.3.46/904
TS_01_IRQ_STATUS	0x0104	TS-01 IRQ status register, reports status of individual IRQ sources from the TS.	15.5.3.47/904
TS_01_IRQ_CLEAR	0x0108	TS-01 IRQ clear register, clears individual IRQ sources from the TS.	15.5.3.48/905
TS_01_IRQ_TEST	0x010c	TS-01 IRQ test register. Write to register will trigger a TS IRQ if the IRQ enabled.	15.5.3.49/905
TS_01_SDIF_RDATA	0x0110	TS-01 read data register	15.5.3.50/906
TS_01_SDIF_DONE	0x0114	TS-01 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.	15.5.3.51/906
TS_01_SDIF_DATA	0x0118	TS-01 SDIF sample data register	15.5.3.52/907
TS_01_ALARMA_CFG	0x0120	TS-01 Alarm A configuration	15.5.3.53/907
TS_01_ALARMB_CFG	0x0124	TS-01 Alarm B configuration	15.5.3.54/908
TS_01_SMPL_HILO	0x0128	TS-01 sample max/min high/low value	15.5.3.55/908
TS_01_HILO_RESET	0x012c	TS-01 reset sample high/low register	15.5.3.56/909
PD_CMN_CLK_SYNTH	0x0180	PD clock synthesiser control register	15.5.3.57/909
PD_CMN_SDIF_DISABLE	0x0184	PD SDIF disable (active high). When asserted completely disables the selected PD instance(s), by forcing the PD macro clock and reset low.	15.5.3.58/910
PD_CMN_SDIF_STATUS	0x0188	PD SDIF status register	15.5.3.59/910
PD_CMN_SDIF	0x018c	PD SDIF write data register	15.5.3.60/911
PD_CMN_SDIF_HALT	0x0190	PD SDIF halt register. Halts all SDIF data transfer and resets SDIF slave.	15.5.3.61/911
PD_CMN_SDIF_CTRL	0x0194	PD SDIF programming inhibit (active high). When asserted inhibits serial programming of the selected PD instance(s).	15.5.3.62/912
PD_CMN_SMPL_CTRL	0x01a0	PD SDIF sample counter control	15.5.3.63/912
PD_CMN_SMPL_CLR	0x01a4	PD SDIF sample counter clear	15.5.3.64/913

Register	Offset	Description	Section/Page
PD_CMN_SMPL_CNT	0x01a8	PD SDIF sample counter current value	15.5.3.65/913
PD_00_IRQ_ENABLE	0x01c0	PD-00 IRQ enable register, enables individual IRQ sources from the PD.	15.5.3.66/914
PD_00_IRQ_STATUS	0x01c4	PD-00 IRQ status register, reports status of individual IRQ sources from the PD.	15.5.3.67/914
PD_00_IRQ_CLEAR	0x01c8	PD-00 IRQ clear register, clears individual IRQ sources from the PD.	15.5.3.68/915
PD_00_IRQ_TEST	0x01cc	PD-00 IRQ test register. Write to register will trigger a PD IRQ if the IRQ enabled.	15.5.3.69/915
PD_00_SDIF_RDATA	0x01d0	PD-00 read data register.	15.5.3.70/916
PD_00_SDIF_DONE	0x01d4	PD-00 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.	15.5.3.71/916
PD_00_SDIF_DATA	0x01d8	PD-00 SDIF sample data register	15.5.3.72/917
PD_00_ALARMA_CFG	0x01e0	PD-00 Alarm A configuration	15.5.3.73/917
PD_00_ALARMB_CFG	0x01e4	PD-00 Alarm B configuration	15.5.3.74/918
PD_00_SMPL_HILO	0x01e8	PD-00 sample max/min high/low value	15.5.3.75/918
PD_00_HILO_RESET	0x01ec	PD-00 reset sample high/low register	15.5.3.76/919
PD_01_IRQ_ENABLE	0x0200	PD-01 IRQ enable register, enables individual IRQ sources from the PD.	15.5.3.77/919
PD_01_IRQ_STATUS	0x0204	PD-01 IRQ status register, reports status of individual IRQ sources from the PD.	15.5.3.78/920
PD_01_IRQ_CLEAR	0x0208	PD-01 IRQ clear register, clears individual IRQ sources from the PD.	15.5.3.79/920
PD_01_IRQ_TEST	0x020c	PD-01 IRQ test register. Write to register will trigger a PD IRQ if the IRQ enabled.	15.5.3.80/921
PD_01_SDIF_RDATA	0x0210	PD-01 read data register	15.5.3.81/921
PD_01_SDIF_DONE	0x0214	PD-01 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.	15.5.3.82/922
PD_01_SDIF_DATA	0x0218	PD-01 SDIF sample data register	15.5.3.83/922
PD_01_ALARMA_CFG	0x0220	PD-01 Alarm A configuration	15.5.3.84/923
PD_01_ALARMB_CFG	0x0224	PD-01 Alarm B configuration	15.5.3.85/923

Register	Offset	Description	Section/Page
PD_01_SMPL_HILO	0x0228	PD-01 sample max/min high/low value	15.5.3.86/924
PD_01_HILO_RESET	0x022c	PD-01 reset sample high/low register	15.5.3.87/924
PD_02_IRQ_ENABLE	0x0240	PD-02 IRQ enable register, enables individual IRQ sources from the PD.	15.5.3.88/924
PD_02_IRQ_STATUS	0x0244	PD-02 IRQ status register, reports status of individual IRQ sources from the PD.	15.5.3.89/925
PD_02_IRQ_CLEAR	0x0248	PD-02 IRQ clear register, clears individual IRQ sources from the PD.	15.5.3.90/926
PD_02_IRQ_TEST	0x024c	PD-02 IRQ test register. Write to register will trigger a PD IRQ if the IRQ enabled.	15.5.3.91/926
PD_02_SDIF_RDATA	0x0250	PD-02 read data register	15.5.3.92/927
PD_02_SDIF_DONE	0x0254	PD-02 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.	15.5.3.93/927
PD_02_SDIF_DATA	0x0258	PD-02 SDIF sample data register	15.5.3.94/927
PD_02_ALARMA_CFG	0x0260	PD-02 Alarm A configuration	15.5.3.95/928
PD_02_ALARMB_CFG	0x0264	PD-02 Alarm B configuration	15.5.3.96/928
PD_02_SMPL_HILO	0x0268	PD-02 sample max/min high/low value	15.5.3.97/929
PD_02_HILO_RESET	0x026c	PD-02 reset sample high/low register	15.5.3.98/929
PD_03_IRQ_ENABLE	0x0280	PD-03 IRQ enable register, enables individual IRQ sources from the PD.	15.5.3.99/930
PD_03_IRQ_STATUS	0x0284	PD-03 IRQ status register, reports status of individual IRQ sources from the PD.	15.5.3.100/930
PD_03_IRQ_CLEAR	0x0288	PD-03 IRQ clear register, clears individual IRQ sources from the PD.	15.5.3.101/931
PD_03_IRQ_TEST	0x028c	PD-03 IRQ test register. Write to register will trigger a PD IRQ if the IRQ enabled.	15.5.3.102/932
PD_03_SDIF_RDATA	0x0290	PD-03 read data register	15.5.3.103/932
PD_03_SDIF_DONE	0x0294	PD-03 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.	15.5.3.104/932
PD_03_SDIF_DATA	0x0298	PD-03 SDIF sample data register	15.5.3.105/933
PD_03_ALARMA_CFG	0x02a0	PD-03 Alarm A configuration	15.5.3.106/933

Register	Offset	Description	Section/Page
PD_03_ALARMB_CFG	0x02a4	PD-03 Alarm B configuration	15.5.3.107/934
PD_03_SMPL_HILO	0x02a8	PD-03 sample max/min high/low value	15.5.3.108/934
PD_03_HILO_RESET	0x02ac	PD-03 reset sample high/low register	15.5.3.109/935
PD_04_IRQ_ENABLE	0x02c0	PD-04 IRQ enable register, enables individual IRQ sources from the PD.	15.5.3.110/935
PD_04_IRQ_STATUS	0x02c4	PD-04 IRQ status register, reports status of individual IRQ sources from the PD.	15.5.3.111/936
PD_04_IRQ_CLEAR	0x02c8	PD-04 IRQ clear register, clears individual IRQ sources from the PD.	15.5.3.112/936
PD_04_IRQ_TEST	0x02cc	PD-04 IRQ test register. Write to register will trigger a PD IRQ if the IRQ enabled.	15.5.3.113/937
PD_04_SDIF_RDATA	0x02d0	PD-04 read data register	15.5.3.114/937
PD_04_SDIF_DONE	0x02d4	PD-04 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.	15.5.3.115/938
PD_04_SDIF_DATA	0x02d8	PD-04 SDIF sample data register	15.5.3.116/938
PD_04_ALARMA_CFG	0x02e0	PD-04 Alarm A configuration	15.5.3.117/939
PD_04_ALARMB_CFG	0x02e4	PD-04 Alarm B configuration	15.5.3.118/939
PD_04_SMPL_HILO	0x02e8	PD-04 sample max/min high/low value	15.5.3.119/940
PD_04_HILO_RESET	0x02ec	PD-04 reset sample high/low register	15.5.3.120/940
PD_05_IRQ_ENABLE	0x0300	PD-05 IRQ enable register, enables individual IRQ sources from the PD.	15.5.3.121/940
PD_05_IRQ_STATUS	0x0304	PD-05 IRQ status register, reports status of individual IRQ sources from the PD.	15.5.3.122/941
PD_05_IRQ_CLEAR	0x0308	PD-05 IRQ clear register, clears individual IRQ sources from the PD.	15.5.3.123/942
PD_05_IRQ_TEST	0x030c	PD-05 IRQ test register. Write to register will trigger a PD IRQ if the IRQ enabled.	15.5.3.124/942
PD_05_SDIF_RDATA	0x0310	PD-05 read data register	15.5.3.125/943
PD_05_SDIF_DONE	0x0314	PD-05 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.	15.5.3.126/943
PD_05_SDIF_DATA	0x0318	PD-05 SDIF sample data register	15.5.3.127/944

Register	Offset	Description	Section/Page
PD_05_ALARMA_CFG	0x0320	PD-05 Alarm A configuration	15.5.3.128/944
PD_05_ALARMB_CFG	0x0324	PD-05 Alarm B configuration	15.5.3.129/945
PD_05_SMPL_HILO	0x0328	PD-05 sample max/min high/low value	15.5.3.130/945
PD_05_HILO_RESET	0x032c	PD-05 reset sample high/low register	15.5.3.131/945
PD_06_IRQ_ENABLE	0x0340	PD-06 IRQ enable register, enables individual IRQ sources from the PD.	15.5.3.132/946
PD_06_IRQ_STATUS	0x0344	PD-06 IRQ status register, reports status of individual IRQ sources from the PD.	15.5.3.133/946
PD_06_IRQ_CLEAR	0x0348	PD-06 IRQ clear register, clears individual IRQ sources from the PD.	15.5.3.134/947
PD_06_IRQ_TEST	0x034c	PD-06 IRQ test register. Write to register will trigger a PD IRQ if the IRQ enabled.	15.5.3.135/948
PD_06_SDIF_RDATA	0x0350	PD-06 read data register	15.5.3.136/948
PD_06_SDIF_DONE	0x0354	PD-06 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.	15.5.3.137/948
PD_06_SDIF_DATA	0x0358	PD-06 SDIF sample data register	15.5.3.138/949
PD_06_ALARMA_CFG	0x0360	PD-06 Alarm A configuration	15.5.3.139/949
PD_06_ALARMB_CFG	0x0364	PD-06 Alarm B configuration	15.5.3.140/950
PD_06_SMPL_HILO	0x0368	PD-06 sample max/min high/low value	15.5.3.141/950
PD_06_HILO_RESET	0x036c	PD-06 reset sample high/low register	15.5.3.142/951
PD_07_IRQ_ENABLE	0x0380	PD-07 IRQ enable register, enables individual IRQ sources from the PD.	15.5.3.143/951
PD_07_IRQ_STATUS	0x0384	PD-07 IRQ status register, reports status of individual IRQ sources from the PD.	15.5.3.144/952
PD_07_IRQ_CLEAR	0x0388	PD-07 IRQ clear register, clears individual IRQ sources from the PD.	15.5.3.145/952
PD_07_IRQ_TEST	0x038c	PD-07 IRQ test register. Write to register will trigger a PD IRQ if the IRQ enabled.	15.5.3.146/953
PD_07_SDIF_RDATA	0x0390	PD-07 read data register	15.5.3.147/953
PD_07_SDIF_DONE	0x0394	PD-07 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.	15.5.3.148/954

Register	Offset	Description	Section/Page
PD_07_SDIF_DATA	0x0398	PD-07 SDIF sample data register	15.5.3.149/954
PD_07_ALARMA_CFG	0x03a0	PD-07 Alarm A configuration	15.5.3.150/955
PD_07_ALARMB_CFG	0x03a4	PD-07 Alarm B configuration	15.5.3.151/955
PD_07_SMPL_HILO	0x03a8	PD-07 sample max/min high/low value	15.5.3.152/956
PD_07_HILO_RESET	0x03ac	PD-07 reset sample high/low register	15.5.3.153/956
PD_08_IRQ_ENABLE	0x03c0	PD-08 IRQ enable register, enables individual IRQ sources from the PD.	15.5.3.154/956
PD_08_IRQ_STATUS	0x03c4	PD-08 IRQ status register, reports status of individual IRQ sources from the PD.	15.5.3.155/957
PD_08_IRQ_CLEAR	0x03c8	PD-08 IRQ clear register, clears individual IRQ sources from the PD.	15.5.3.156/958
PD_08_IRQ_TEST	0x03cc	PD-08 IRQ test register. Write to register will trigger a PD IRQ if the IRQ enabled.	15.5.3.157/958
PD_08_SDIF_RDATA	0x03d0	PD-08 read data register	15.5.3.158/959
PD_08_SDIF_DONE	0x03d4	PD-08 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.	15.5.3.159/959
PD_08_SDIF_DATA	0x03d8	PD-08 SDIF sample data register	15.5.3.160/960
PD_08_ALARMA_CFG	0x03e0	PD-08 Alarm A configuration	15.5.3.161/960
PD_08_ALARMB_CFG	0x03e4	PD-08 Alarm B configuration	15.5.3.162/961
PD_08_SMPL_HILO	0x03e8	PD-08 sample max/min high/low value	15.5.3.163/961
PD_08_HILO_RESET	0x03ec	PD-08 reset sample high/low register	15.5.3.164/961
PD_09_IRQ_ENABLE	0x0400	PD-09 IRQ enable register, enables individual IRQ sources from the PD.	15.5.3.165/962
PD_09_IRQ_STATUS	0x0404	PD-09 IRQ status register, reports status of individual IRQ sources from the PD.	15.5.3.166/962
PD_09_IRQ_CLEAR	0x0408	PD-09 IRQ clear register, clears individual IRQ sources from the PD.	15.5.3.167/963
PD_09_IRQ_TEST	0x040c	PD-09 IRQ test register. Write to register will trigger a PD IRQ if the IRQ enabled.	15.5.3.168/964
PD_09_SDIF_RDATA	0x0410	PD-09 read data register	15.5.3.169/964
PD_09_SDIF_DONE	0x0414	PD-09 SDIF sample done register. Indicates sample data is available, cleared by of SDIF	15.5.3.170/964

Register	Offset	Description	Section/Page
		sample data register.	
PD_09_SDIF_DATA	0x0418	PD-09 SDIF sample data register	15.5.3.171/965
PD_09_ALARMA_CFG	0x0420	PD-09 Alarm A configuration	15.5.3.172/965
PD_09_ALARMB_CFG	0x0424	PD-09 Alarm B configuration	15.5.3.173/966
PD_09_SMPL_HILO	0x0428	PD-09 sample max/min high/low value	15.5.3.174/966
PD_09_HILO_RESET	0x042c	PD-09 reset sample high/low register	15.5.3.175/967
PD_10_IRQ_ENABLE	0x0440	PD-10 IRQ enable register, enables individual IRQ sources from the PD.	15.5.3.176/967
PD_10_IRQ_STATUS	0x0444	PD-10 IRQ status register, reports status of individual IRQ sources from the PD.	15.5.3.177/968
PD_10_IRQ_CLEAR	0x0448	PD-10 IRQ clear register, clears individual IRQ sources from the PD.	15.5.3.178/968
PD_10_IRQ_TEST	0x044c	PD-10 IRQ test register. Write to register will trigger a PD IRQ if the IRQ enabled.	15.5.3.179/969
PD_10_SDIF_RDATA	0x0450	PD-10 read data register	15.5.3.180/969
PD_10_SDIF_DONE	0x0454	PD-10 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.	15.5.3.181/970
PD_10_SDIF_DATA	0x0458	PD-10 SDIF sample data register	15.5.3.182/970
PD_10_ALARMA_CFG	0x0460	PD-10 Alarm A configuration	15.5.3.183/971
PD_10_ALARMB_CFG	0x0464	PD-10 Alarm B configuration	15.5.3.184/971
PD_10_SMPL_HILO	0x0468	PD-10 sample max/min high/low value	15.5.3.185/972
PD_10_HILO_RESET	0x046c	PD-10 reset sample high/low register	15.5.3.186/972
VM_CMN_CLK_SYNTH	0x0800	VM clock synthesiser control register	15.5.3.187/972
VM_CMN_SDIF_DISABLE	0x0804	VM SDIF disable (active high). When asserted completely disables the selected VM instance(s), by forcing the VM macro clock and reset low.	15.5.3.188/973
VM_CMN_SDIF_STATUS	0x0808	VM SDIF status register	15.5.3.189/974
VM_CMN_SDIF	0x080c	VM SDIF write data register	15.5.3.190/974
VM_CMN_SDIF_HALT	0x0810	VM SDIF halt register. Halts all SDIF data transfer and resets SDIF slave.	15.5.3.191/975

Register	Offset	Description	Section/Page
VM_CMN_SDIF_CTRL	0x0814	VM SDIF programming inhibit (active high). When asserted inhibits serial programming of the selected VM instance(s).	15.5.3.192/975
VM_CMN_SMPL_CTRL	0x0820	VM SDIF sample counter control	15.5.3.193/976
VM_CMN_SMPL_CLR	0x0824	VM SDIF sample counter clear	15.5.3.194/976
VM_CMN_SMPL_CNT	0x0828	VM SDIF sample counter current value	15.5.3.195/977
VM_00_IRQ_ENABLE	0x0a00	VM-00 IRQ enable register, enables individual IRQ sources from the VM.	15.5.3.196/977
VM_00_IRQ_STATUS	0x0a04	VM-00 IRQ status register, reports status of individual IRQ sources from the VM.	15.5.3.197/977
VM_00_IRQ_CLEAR	0x0a08	VM-00 IRQ clear register, clears individual IRQ sources from the VM.	15.5.3.198/978
VM_00_IRQ_TEST	0x0a0c	VM-00 IRQ test register. Write to register will trigger a VM IRQ if the IRQ enabled.	15.5.3.199/978
VM_00_IRQ_ALARMA_ENABLE	0x0a10	VM-00 Alarm-A IRQ enable register, enables individual IRQ sources from the VM.	15.5.3.200/979
VM_00_IRQ_ALARMA_STATUS	0x0a14	VM-00 Alarm-A IRQ status register, reports status of individual IRQ sources from the VM.	15.5.3.201/979
VM_00_IRQ_ALARMA_CLR	0x0a18	VM-00 Alarm-A IRQ clear register, clears individual IRQ sources from the VM.	15.5.3.202/979
VM_00_IRQ_ALARMA_TEST	0x0a1c	VM-00 Alarm-A IRQ test register. Write to register will trigger a VM IRQ if the IRQ enabled.	15.5.3.203/979
VM_00_IRQ_ALARMB_ENABLE	0x0a20	VM-00 Alarm-B IRQ enable register, enables individual IRQ sources from the VM.	15.5.3.204/980
VM_00_IRQ_ALARMB_STATUS	0x0a24	VM-00 Alarm-B IRQ status register, reports status of individual IRQ sources from the VM.	15.5.3.205/980
VM_00_IRQ_ALARMB_CLR	0x0a28	VM-00 Alarm-B IRQ clear register, clears individual IRQ sources from the VM.	15.5.3.206/980
VM_00_IRQ_ALARMB_TEST	0x0a2c	VM-00 Alarm-B IRQ test register. Write to register will trigger a VM IRQ if the IRQ enabled.	15.5.3.207/981

Register	Offset	Description	Section/Page
VM_00_SDIF_RDATA	0x0a30	VM read data register	15.5.3.208/981
VM_00_SDIF_DONE	0x0a34	VM SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.	15.5.3.209/981
VM_00_CH_00_SDIF_DATA	0x0a40	VM-00 SDIF channel 00 sample data register	15.5.3.210/982
VM_00_CH_01_SDIF_DATA	0x0a44	VM-00 SDIF channel 01 sample data register	15.5.3.211/982
VM_00_CH_02_SDIF_DATA	0x0a48	VM-00 SDIF channel 02 sample data register	15.5.3.212/983
VM_00_CH_03_SDIF_DATA	0x0a4c	VM-00 SDIF channel 03 sample data register	15.5.3.213/984
VM_00_CH_04_SDIF_DATA	0x0a50	VM-00 SDIF channel 04 sample data register	15.5.3.214/984
VM_00_CH_05_SDIF_DATA	0x0a54	VM-00 SDIF channel 05 sample data register	15.5.3.215/985
VM_00_CH_06_SDIF_DATA	0x0a58	VM-00 SDIF channel 06 sample data register	15.5.3.216/986
VM_00_CH_07_SDIF_DATA	0x0a5c	VM-00 SDIF channel 07 sample data register	15.5.3.217/986
VM_00_CH_08_SDIF_DATA	0x0a60	VM-00 SDIF channel 08 sample data register	15.5.3.218/987
VM_00_CH_09_SDIF_DATA	0x0a64	VM-00 SDIF channel 09 sample data register	15.5.3.219/988
VM_00_CH_10_SDIF_DATA	0x0a68	VM-00 SDIF channel 10 sample data register	15.5.3.220/988
VM_00_CH_11_SDIF_DATA	0x0a6c	VM-00 SDIF channel 11 sample data register	15.5.3.221/989
VM_00_CH_12_SDIF_DATA	0x0a70	VM-00 SDIF channel 12 sample data register	15.5.3.222/990
VM_00_CH_13_SDIF_DATA	0x0a74	VM-00 SDIF channel 13 sample data register	15.5.3.223/990
VM_00_CH_14_SDIF_DATA	0x0a78	VM-00 SDIF channel 14 sample data register	15.5.3.224/991
VM_00_CH_15_SDIF_DATA	0x0a7c	VM-00 SDIF channel 15 sample data	15.5.3.225/992

Register	Offset	Description	Section/Page
		register	
VM_00_CH_00_ALARMA_CFG	0x0a80	VM-00 channel 00 Alarm A configuration	15.5.3.226/992
VM_00_CH_00_ALARMB_CFG	0x0a84	VM-00 channel 00 Alarm B configuration	15.5.3.227/993
VM_00_CH_00_SMPL_HILO	0x0a88	VM-00 channel 00 sample max/min high/low value	15.5.3.228/993
VM_00_CH_00_HILO_RESET	0x0a8c	VM-00 channel 00 reset sample high/low register	15.5.3.229/993
VM_00_CH_01_ALARMA_CFG	0x0a90	VM-00 channel 01 Alarm A configuration	15.5.3.230/994
VM_00_CH_01_ALARMB_CFG	0x0a94	VM-00 channel 01 Alarm B configuration	15.5.3.231/994
VM_00_CH_01_SMPL_HILO	0x0a98	VM-00 channel 01 sample max/min high/low value	15.5.3.232/995
VM_00_CH_01_HILO_RESET	0x0a9c	VM-00 channel 01 reset sample high/low register	15.5.3.233/995
VM_00_CH_02_ALARMA_CFG	0x0aa0	VM-00 channel 02 Alarm A configuration	15.5.3.234/995
VM_00_CH_02_ALARMB_CFG	0x0aa4	VM-00 channel 02 Alarm B configuration	15.5.3.235/996
VM_00_CH_02_SMPL_HILO	0x0aa8	VM-00 channel 02 sample max/min high/low value	15.5.3.236/996
VM_00_CH_02_HILO_RESET	0x0aac	VM-00 channel 02 Reset sample high/low register	15.5.3.237/997
VM_00_CH_03_ALARMA_CFG	0x0ab0	VM-00 channel 03 Alarm A configuration	15.5.3.238/997
VM_00_CH_03_ALARMB_CFG	0x0ab4	VM-00 channel 03 Alarm B configuration	15.5.3.239/997
VM_00_CH_03_SMPL_HILO	0x0ab8	VM-00 channel 03 sample max/min high/low value	15.5.3.240/998
VM_00_CH_03_HILO_RESET	0x0abc	VM-00 channel 03 reset sample high/low register	15.5.3.241/998
VM_00_CH_04_ALARMA_CFG	0x0ac0	VM-00 channel 04 Alarm A configuration	15.5.3.242/999
VM_00_CH_04_ALARMB_CFG	0x0ac4	VM-00 channel 04 Alarm B configuration	15.5.3.243/999
VM_00_CH_04_SMPL_HILO	0x0ac8	VM-00 channel 04 sample max/min high/low value	15.5.3.244/999
VM_00_CH_04_HILO_RESET	0x0acc	VM-00 channel 04 reset sample high/low register	15.5.3.245/1000
VM_00_CH_05_ALARMA_CFG	0x0ad0	VM-00 channel 05 Alarm A configuration	15.5.3.246/1000

Register	Offset	Description	Section/Page
VM_00_CH_05_ALARMB_CFG	0x0ad4	VM-00 channel 05 Alarm B configuration	15.5.3.247/1001
VM_00_CH_05_SMPL_HILO	0x0ad8	VM-00 channel 05 sample max/min high/low value	15.5.3.248/1001
VM_00_CH_05_HILO_RESET	0x0adc	VM-00 channel 05 reset sample high/low register	15.5.3.249/1001
VM_00_CH_06_ALARMA_CFG	0x0ae0	VM-00 channel 06 Alarm A configuration	15.5.3.250/1002
VM_00_CH_06_ALARMB_CFG	0x0ae4	VM-00 channel 06 Alarm B configuration	15.5.3.251/1002
VM_00_CH_06_SMPL_HILO	0x0ae8	VM-00 channel 06 sample max/min high/low value	15.5.3.252/1003
VM_00_CH_06_HILO_RESET	0x0aec	VM-00 channel 06 reset sample high/low register	15.5.3.253/1003
VM_00_CH_07_ALARMA_CFG	0x0af0	VM-00 channel 07 Alarm A configuration	15.5.3.254/1003
VM_00_CH_07_ALARMB_CFG	0x0af4	VM-00 channel 07 Alarm B configuration	15.5.3.255/1004
VM_00_CH_07_SMPL_HILO	0x0af8	VM-00 channel 07 sample max/min high/low value	15.5.3.256/1004
VM_00_CH_07_HILO_RESET	0x0afc	VM-00 channel 07 reset sample high/low register	15.5.3.257/1005
VM_00_CH_08_ALARMA_CFG	0x0b00	VM-00 channel 08 Alarm A configuration	15.5.3.258/1005
VM_00_CH_08_ALARMB_CFG	0x0b04	VM-00 channel 08 Alarm B configuration	15.5.3.259/1005
VM_00_CH_08_SMPL_HILO	0x0b08	VM-00 channel 08 sample max/min high/low value	15.5.3.260/1006
VM_00_CH_08_HILO_RESET	0x0b0c	VM-00 channel 08 reset sample high/low register	15.5.3.261/1006
VM_00_CH_09_ALARMA_CFG	0x0b10	VM-00 channel 09 Alarm A configuration	15.5.3.262/1007
VM_00_CH_09_ALARMB_CFG	0x0b14	VM-00 channel 09 Alarm B configuration	15.5.3.263/1007
VM_00_CH_09_SMPL_HILO	0x0b18	VM-00 channel 09 sample max/min high/low value	15.5.3.264/1007
VM_00_CH_09_HILO_RESET	0x0b1c	VM-00 channel 09 reset sample high/low register	15.5.3.265/1008
VM_00_CH_10_ALARMA_CFG	0x0b20	VM-00 channel 10 Alarm A configuration	15.5.3.266/1008
VM_00_CH_10_ALARMB_CFG	0x0b24	VM-00 channel 10 Alarm B configuration	15.5.3.267/1009
VM_00_CH_10_SMPL_HILO	0x0b28	VM-00 channel 10 sample max/min high/low value	15.5.3.268/1009

Register	Offset	Description	Section/Page
VM_00_CH_10_HILO_RESET	0x0b2c	VM-00 channel 10 reset sample high/low register	15.5.3.269/1009
VM_00_CH_11_ALARMA_CFG	0x0b30	VM-00 channel 11 Alarm A configuration	15.5.3.270/1010
VM_00_CH_11_ALARMB_CFG	0x0b34	VM-00 channel 11 Alarm B configuration	15.5.3.271/1010
VM_00_CH_11_SMPL_HILO	0x0b38	VM-00 channel 11 sample max/min high/low value	15.5.3.272/1011
VM_00_CH_11_HILO_RESET	0x0b3c	VM-00 channel 11 reset sample high/low register	15.5.3.273/1011
VM_00_CH_12_ALARMA_CFG	0x0b40	VM-00 channel 12 Alarm A configuration	15.5.3.274/1011
VM_00_CH_12_ALARMB_CFG	0x0b44	VM-00 channel 12 Alarm B configuration	15.5.3.275/1012
VM_00_CH_12_SMPL_HILO	0x0b48	VM-00 channel 12 sample max/min high/low value	15.5.3.276/1012
VM_00_CH_12_HILO_RESET	0x0b4c	VM-00 channel 12 reset sample high/low register	15.5.3.277/1013
VM_00_CH_13_ALARMA_CFG	0x0b50	VM-00 channel 13 Alarm A configuration	15.5.3.278/1013
VM_00_CH_13_ALARMB_CFG	0x0b54	VM-00 channel 13 Alarm B configuration	15.5.3.279/1013
VM_00_CH_13_SMPL_HILO	0x0b58	VM-00 channel 13 sample max/min high/low value	15.5.3.280/1014
VM_00_CH_13_HILO_RESET	0x0b5c	VM-00 channel 13 reset sample high/low register	15.5.3.281/1014
VM_00_CH_14_ALARMA_CFG	0x0b60	VM-00 channel 14 Alarm A configuration	15.5.3.282/1015
VM_00_CH_14_ALARMB_CFG	0x0b64	VM-00 channel 14 Alarm B configuration	15.5.3.283/1015
VM_00_CH_14_SMPL_HILO	0x0b68	VM-00 channel 14 sample max/min high/low value	15.5.3.284/1015
VM_00_CH_14_HILO_RESET	0x0b6c	VM-00 channel 14 reset sample high/low register	15.5.3.285/1016
VM_00_CH_15_ALARMA_CFG	0x0b70	VM-00 channel 15 Alarm A configuration	15.5.3.286/1016
VM_00_CH_15_ALARMB_CFG	0x0b74	VM-00 channel 15 Alarm B configuration	15.5.3.287/1017
VM_00_CH_15_SMPL_HILO	0x0b78	VM-00 channel 15 sample max/min high/low value	15.5.3.288/1017
VM_00_CH_15_HILO_RESET	0x0b7c	VM-00 channel 15 reset sample high/low register	15.5.3.289/1017

15.5.3 Register and Field Description

15.5.3.1 PVT_COMP_ID

- Description: PVT controller ID and revision
- Offset: 0x0000
- Default Value: 0x9b487060

Bits	Field Name	Access	Description
[31:18]	MOORTEC_ID	RO	Moortec ID, fixed value. Volatile: No Value After Reset: 0x26D2
[17:12]	COMPONENT_ID	RO	Component ID, fixed value. Volatile: No Value After Reset: 0x07
[11:10]	RESERVED_1	-	
[9:5]	REV_MAJOR	RO	Major component revision ID. Value change subject when module is revised. Volatile: No Value After Reset: 0x3
[4:0]	REV_MINOR	RO	Minor component revision ID. Value change subject when module is revised. Volatile: No Value After Reset: 0x0

15.5.3.2 PVT_IP_CFG

- Description: PVT controller IP configuration
- Offset: 0x0004
- Default Value: 0x10010b02

Bits	Field Name	Access	Description
[31:24]	CH_NUM	RO	Number of channels in VM module macro Volatile: No Value After Reset: 0x10
[23:16]	VM_NUM	RO	Number of VM module macros connected Volatile: No Value After Reset: 0x1

Bits	Field Name	Access	Description
[15:8]	PD_NUM	RO	Number of PD module macros connected Volatile: No Value After Reset: 0xB
[7:0]	TS_NUM	RO	Number of TS module macros connected Volatile: No Value After Reset: 0x2

15.5.3.3 PVT_ID_NUM

- Description: PVT customer defined controller information
- Offset: 0x0008
- Default Value: 0x12345678

Bits	Field Name	Access	Description
[31:0]	CUSTOM_ID	RW	User defined value Volatile: No Value After Reset: 0x12345678

15.5.3.4 PVT_TM_SCRATCH

- Description: PVT scratch test register
- Offset: 0x000c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SCRATCH	RW	Scratch, test register. Volatile: No Value After Reset: 0x0

15.5.3.5 PVT_REG_LOCK

- Description: PVT soft lock register. Any write to register locks certain controllers' registers. Unlocked by writing 0x1ACCE551.
- Offset: 0x0010
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	LOCK	RW	PVT soft lock register. Any write to register locks module macro registers. Software lock can be removed by writing 0x1ACCE551.

Bits	Field Name	Access	Description
			Volatile: No Value After Reset: 0x0

15.5.3.6 PVT_LOCK_STATUS

- Description: PVT lock status. Reading returns the current lock status.
- Offset: 0x0014
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	HW_LOCK_STATUS	RO	Indicates the status of the HW lock input to the PVT controller. Volatile: Yes Value After Reset: 0x0
[0]	SW_LOCK_STATUS	RO	Indicates the current state of the lock register. Volatile: Yes Value After Reset: 0x0

15.5.3.7 PVT_TAM_STATUS

- Description: PVT test access status. Read of register indicates that the TAM has been active.
- Offset: 0x0018
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	TAM_STATUS	RO	Indicates that TAM has been active. Volatile: Yes Value After Reset: 0x0

15.5.3.8 PVT_TAM_CLEAR

- Description: PVT test access clear. Write to this register clears the TAM status register.
- Offset: 0x001c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	

Bits	Field Name	Access	Description
[0]	TAM_STATUS_CLR	WO	Clear the TAM status. Volatile: No Value After Reset: 0x0

15.5.3.9 PVT_TMR_CTRL

- Description: PVT timer control register. R/W to set timers behavior.
- Offset: 0x0020
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:17]	RESERVED_1	-	
[16]	TMR_RUN	RW	Enables timer count function. Volatile: No Value After Reset: 0x0
[15:0]	TMR_DELAY	RW	Timer delay Volatile: No Value After Reset: 0x0

15.5.3.10 PVT_TMR_STATUS

- Description: PVT timer status register. Read of register returns timer status if timer is enabled.
- Offset: 0x0024
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	TMR_DONE	RO	Set when the counter delay has expired. Volatile: Yes Value After Reset: 0x0
[0]	TMR_BUSY	RO	Set while the counter is active. Volatile: Yes Value After Reset: 0x0

15.5.3.11 PVT_TMR_IRQ_CLEAR

- Description: PVT timer IRQ clear register. Write to register clears timer IRQ.
- Offset: 0x0028

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	TMR_IRQ_CLR	WO	Set while the counter is active. Volatile: No Value After Reset: 0x0

15.5.3.12 PVT_TMR_IRQ_TEST

- Description: PVT timer IRQ test register. Write to register will trigger a timer IRQ if timer IRQ enabled.
- Offset: 0x002c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	TMR_IRQ_TEST	RW	Set while the counter is active. Volatile: No Value After Reset: 0x0

15.5.3.13 IRQ_EN

- Description: PVT master IRQ register, enables IRQ from the module blocks and timer.
- Offset: 0x0040
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	PD_IRQ_ENABLE	RW	Enable TS IRQ source, set to enable the TS IRQ to the processor. Volatile: No Value After Reset: 0x0
[2]	VM_IRQ_ENABLE	RW	Enable TS IRQ source, set to enable the TS IRQ to the processor. Volatile: No Value After Reset: 0x0
[1]	TS_IRQ_ENABLE	RW	Enable TS IRQ source, set to enable the TS IRQ to the processor. Volatile: No

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[0]	TMR_IRQ_ENABLE	RW	Enable Timer IRQ source, set to enable the Timer IRQ to the processor. Volatile: No Value After Reset: 0x0

15.5.3.14 IRQ_TR_MASK

- Description: PVT master IRQ mask register, allows masking of timer IRQ. Write 1 to mask IRQ source.
- Offset: 0x0050
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	TMR_IRQ_MASK	RW	Mask Timer IRQ source, set to mask Timer IRQ to the processor. Volatile: No Value After Reset: 0x0

15.5.3.15 IRQ_TS_MASK

- Description: PVT master IRQ mask register, allows masking of TS IRQ. Write 1 to mask IRQ source.
- Offset: 0x0054
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1:0]	TS_IRQ_MASK	RW	Mask TS IRQ source, set to mask TS IRQ to the processor. Volatile: No Value After Reset: 0x0

15.5.3.16 IRQ_VM_MASK

- Description: PVT master IRQ mask register, allows masking of VM IRQ. Write 1 to mask IRQ source.
- Offset: 0x0058
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	VM_IRQ_MASK	RW	Mask VM IRQ source, set to mask VM IRQ to the processor. Volatile: No Value After Reset: 0x0

15.5.3.17 IRQ_PD_MASK

- Description: PVT master IRQ mask register, allows masking of PD IRQ. Write 1 to mask IRQ source.
- Offset: 0x005c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:0]	PD_IRQ_MASK	RW	Mask PD IRQ source, set to mask PD IRQ to the processor. Volatile: No Value After Reset: 0x0

15.5.3.18 IRQ_TR_STATUS

- Description: PVT master IRQ status register. Reading gives timer IRQ status (after mask, if applied).
- Offset: 0x0060
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	TMR_IRQ_STATUS	RO	Timer IRQ status, after the mask has been applied. Volatile: Yes Value After Reset: 0x0

15.5.3.19 IRQ_TS_STATUS

- Description: PVT master IRQ status register. Reading gives TS IRQ status (after masking, if applied).
- Offset: 0x0064
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1:0]	TS_IRQ_STATUS	RO	TS IRQ status, after the mask has been applied. Volatile: Yes Value After Reset: 0x0

15.5.3.20 IRQ_VM_STATUS

- Description: PVT master IRQ status register. Reading gives VM IRQ status (after masking, if applied).
- Offset: 0x0068
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	VM_IRQ_STATUS	RO	VM IRQ status, after the mask has been applied. Volatile: Yes Value After Reset: 0x0

15.5.3.21 IRQ_PD_STATUS

- Description: PVT master IRQ status register. Reading gives PD IRQ status (after masking, if applied).
- Offset: 0x006c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:0]	PD_IRQ_STATUS	RO	PD IRQ status, after the mask has been applied. Volatile: Yes Value After Reset: 0x0

15.5.3.22 IRQ_TR_RAW

- Description: PVT master IRQ raw status register. Reading gives Timer IRQ status no masking.
- Offset: 0x0070
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	

Bits	Field Name	Access	Description
[0]	TMR_IRQ_RAW_STATUS	RO	Timer IRQ status, before the mask has been applied. Volatile: Yes Value After Reset: 0x0

15.5.3.23 IRQ_TS_RAW

- Description: PVT master IRQ raw status register. Reading gives TS IRQ status no masking.
- Offset: 0x0074
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1:0]	TS_IRQ_RAW_STATUS	RO	TS IRQ status, before the mask has been applied. Volatile: Yes Value After Reset: 0x0

15.5.3.24 IRQ_VM_RAW

- Description: PVT master IRQ raw status register. Reading gives VM IRQ status no masking.
- Offset: 0x0078
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	VM_IRQ_RAW_STATUS	RO	VM raw IRQ status, before the mask has been applied. Volatile: Yes Value After Reset: 0x0

15.5.3.25 IRQ_PD_RAW

- Description: PVT master IRQ raw status register. Reading gives PD IRQ status no masking.
- Offset: 0x007c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:0]	PD_IRQ_RAW_STATUS	RO	PD raw IRQ status, before mask has been applied. Volatile: Yes Value After Reset: 0x0

15.5.3.26 TS_CMN_CLK_SYNTH

- Description: TS clock synthesiser control register
- Offset: 0x0080
- Default Value: 0x10000

Bits	Field Name	Access	Description
[31:25]	RESERVED_2	-	
[24]	CLK_SYTH_EN	RW	Synthesized 'clk_ip' active high enable Volatile: No Value After Reset: 0x0
[23:20]	RESERVED_1	-	
[19:16]	CLK_SYNTH_HOLD	RW	SDA master to SDA slave output hold delay from posedge clk_ip and SDA slave to SDA master input setup delay from posedge 'clk_ip'. Expressed in units of 'clk_sys' cycles, the synth_strobe value must NOT exceed the synthesised clock period i.e. synth_setup <= synth_hi + synth_lo + 1. Volatile: No Value After Reset: 0x1
[15:8]	CLK_SYNTH_HI	RW	Synthesized 'clk_ip' high period zero indexed expressed in units of 'clk_sys' cycles. Volatile: No Value After Reset: 0x0
[7:0]	CLK_SYNTH_LO	RW	Synthesized 'clk_ip' low period zero indexed expressed in units of 'clk_sys' cycles. Volatile: No Value After Reset: 0x0

15.5.3.27 TS_CMN_SDIF_DISABLE

- Description: TS SDIF disable (active high). When asserted completely disables the selected TS instance(s), by forcing the TS macro clock and reset low.
- Offset: 0x0084
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1:0]	SDIF_DISABLE_TS_HHH	RW	Serial data interface (SDIF) disable (active high). When asserted completely disables the selected module

Bits	Field Name	Access	Description
			instance(s), by forcing the module macro clock and reset low. Any disables should be applied before SDIF programming begins. e.g. setting sdif_disable = 8'b1000_1011 will disable module instances 0, 1, 3 & 7. Volatile: No Value After Reset: 0x0

15.5.3.28 TS_CMN_SDIF_STATUS

- Description: TS SDIF status register
- Offset: 0x0088
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SDIF_LOCK	RO	SDIF locked (active high). Set when slave auto mode is requested to indicate the serial data interface (SDIF) is now a write only interface. Volatile: Yes Value After Reset: 0x0
[0]	SDIF_BUSY	RO	SDIF busy (active high). When asserted indicates the serial data interface (SDIF) is busy so any SDIF programming requests will be ignored. Or the clock synthesiser/disable SDIF state is being updated. Volatile: Yes Value After Reset: 0x0

15.5.3.29 TS_CMN_SDIF

- Description: TS SDIF write data register
- Offset: 0x008c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	SDIF_PROG	WO	Serial I/F program request (active high). This self-clearing bit will be ignored if the sdif_busy flag is set or if the sdif_lock flag is set and the request is a read request (sdif_wrn = 0). Volatile: No Value After Reset: 0x0

Bits	Field Name	Access	Description
[30:28]	RESERVED_1	-	
[27]	SDIF_WRN	RW	Serial I/F Write NOT Read control bit 1: Write 0: Read Volatile: No Value After Reset: 0x0
[26:24]	SDIF_ADDR	RW	Serial I/F register address, SDIF_ADDR[1:0] Volatile: No Value After Reset: 0x0
[23:0]	SDIF_WDATA	RW	Serial I/F write data, SDIF_DATA[23:0] Volatile: No Value After Reset: 0x0

15.5.3.30 TS_CMN_SDIF_HALT

- Description: TS SDIF halt register. Halts all SDIF data transfer and resets SDIF slave.
- Offset: 0x0090
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_STOP	WO	Serial I/F write data. Serial data interface (SDIF) stop (active high). This self-clearing bit immediately stops all SDIF programming activity. The feature provides a means to terminate serial data interface activity in the unlikely event of it becoming locked, it should not be required during normal operation. Volatile: No Value After Reset: 0x0

15.5.3.31 TS_CMN_SDIF_CTRL

- Description: TS SDIF programming inhibit (active high). When asserted inhibits serial programming of the selected TS instance(s).
- Offset: 0x0094
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1:0]	SDIF_INHIBIT_TS_HHH	RW	Serial data interface (SDIF) programming inhibit (active high). When asserted inhibits serial programming of the selected module instance(s). Inhibits should be applied before SDIF programming begins. e.g. setting sdif_inhibit = 8'b1000_1011 will disable programing of module instances 0, 1, 3 & 7. Volatile: No Value After Reset: 0x0

15.5.3.32 TS_CMN_SMPL_CTRL

- Description: TS SDIF sample counter control
- Offset: 0x00a0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	SMPL_DISCARD	RW	Sample discard (active high). This feature can be used to temporarily discard received data samples. When this bit is set data recovery is disabled but the external module may continue to run. Volatile: No Value After Reset: 0x0
[1]	SMPL_CTR_HOLD	RW	Sample counter hold (active high). When asserted the sample counter is prevented from rolling over when the maximum sample count is reached. Volatile: No Value After Reset: 0x0
[0]	SMPL_CTR_DISABLE	RW	Sample counter disable (active high) 0x0: Sample counter enabled. 0x1: Sample counter disabled. Volatile: No Value After Reset: 0x0

15.5.3.33 TS_CMN_SMPL_CLR

- Description: TS SDIF sample counter clear
- Offset: 0x00a4

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SMPL_CTR_DISABLE	WO	Sample counter clear (active high write). The sample counter value is set to zero when this self-clearing bit is written with '1'. Volatile: No Value After Reset: 0x0

15.5.3.34 TS_CMN_SMPL_CNT

- Description: TS SDIF sample counter current value
- Offset: 0x00a8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	SMPL_COUNT	RO	Sample counter. The 16-bit counter increments each time a new data sample is made available. The counter is cleared by writing '1' to 'smpl_ctr_clr'. The sample counter over-flow operation is determined by 'smpl_ctr_hold'. Volatile: Yes Value After Reset: 0x0

15.5.3.35 TS_00_IRQ_ENABLE

- Description: TS-00 IRQ enable register, enables individual IRQ sources from the TS.
- Offset: 0x00c0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_EN_ALARMB_TS_HHH	RW	Alarm B IRQ enable Volatile: No Value After Reset: 0x0
[3]	IRQ_EN_ALARMA_TS_HHH	RW	Alarm A IRQ enable Volatile: No Value After Reset: 0x0

Bits	Field Name	Access	Description
[2]	RESERVED_1	-	
[1]	IRQ_EN_DONE	RW	Sample done IRQ enable Volatile: No Value After Reset: 0x0
[0]	IRQ_EN_FAULT	RW	Fault IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.36 TS_00_IRQ_STATUS

- Description: TS-00 IRQ status register, reports status of individual IRQ sources from the TS.
- Offset: 0x00c4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_STATUS_ALARMB_TS_HHH	RO	Alarm B IRQ status Volatile: Yes Value After Reset: 0x0
[3]	IRQ_STATUS_ALARMA_TS_HHH	RO	Alarm A IRQ status Volatile: Yes Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_STATUS_DONE	RO	Sample done IRQ status Volatile: Yes Value After Reset: 0x0
[0]	IRQ_STATUS_FAULT	RO	Fault IRQ status Volatile: Yes Value After Reset: 0x0

15.5.3.37 TS_00_IRQ_CLEAR

- Description: TS-00 IRQ clear register, clears individual IRQ sources from the TS.
- Offset: 0x00c8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_TS_HHH	WO	Alarm B IRQ clear Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_TS_HHH	WO	Alarm A IRQ clear Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	WO	Sample done IRQ clear Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	WO	Fault IRQ clear Volatile: No Value After Reset: 0x0

15.5.3.38 TS_00_IRQ_TEST

- Description: TS-00 IRQ test register. Write to register will trigger a TS IRQ if the IRQ enabled.
- Offset: 0x00cc
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_TS_HHH	RW	Alarm B IRQ test Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_TS_HHH	RW	Alarm A IRQ test Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	RW	Sample done IRQ test Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	RW	Fault IRQ test

Bits	Field Name	Access	Description
			Volatile: No Value After Reset: 0x0

15.5.3.39 TS_00_SDIF_RDATA

- Description: TS-00 read data register
- Offset: 0x00d0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	SDIF_RDATA	RO	SDIF read data Volatile: Yes Value After Reset: 0x0

15.5.3.40 TS_00_SDIF_DONE

- Description: TS-00 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.
- Offset: 0x00d4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_SMPL_DONE	RO	Sample done flag (active high). The sample done flag is asserted when a new data sample is made available. The sample done flag is automatically cleared when the associated 'data' register is read. Volatile: Yes Value After Reset: 0x0

15.5.3.41 TS_00_SDIF_DATA

- Description: TS-00 SDIF sample data register
- Offset: 0x00d8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	SAMPLE_FAULT	RO	Sample fault. When set indicates that the module has

Bits	Field Name	Access	Description
			signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	SAMPLE_TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the [TS|PD]_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.42 TS_00_ALARMA_CFG

- Description: TS-00 Alarm A configuration
- Offset: 0x00e0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.43 TS_00_ALARMB_CFG

- Description: TS-00 Alarm B configuration
- Offset: 0x00e4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.44 TS_00_SMPL_HILO

- Description: TS-00 sample max/min high/low value
- Offset: 0x00e8
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.45 TS_00_HILO_RESET

- Description: TS-00 reset sample high/low register
- Offset: 0x00ec
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: No Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written.

Bits	Field Name	Access	Description
			Volatile: No Value After Reset: 0x0

15.5.3.46 TS_01_IRQ_ENABLE

- Description: TS-01 IRQ enable register, enables individual IRQ sources from the TS.
- Offset: 0x0100
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_EN_ALARMB_TS_HHH	RW	Alarm B IRQ enable Volatile: No Value After Reset: 0x0
[3]	IRQ_EN_ALARMA_TS_HHH	RW	Alarm A IRQ enable Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_EN_DONE	RW	Sample done IRQ enable Volatile: No Value After Reset: 0x0
[0]	IRQ_EN_FAULT	RW	Fault IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.47 TS_01_IRQ_STATUS

- Description: TS-01 IRQ status register, reports status of individual IRQ sources from the TS.
- Offset: 0x0104
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_STATUS_ALARMB_TS_HHH	RO	Alarm B IRQ status Volatile: Yes Value After Reset: 0x0
[3]	IRQ_STATUS_ALARMA_TS_HHH	RO	Alarm A IRQ status

Bits	Field Name	Access	Description
			Volatile: Yes Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_STATUS_DONE	RO	Sample done IRQ status Volatile: Yes Value After Reset: 0x0
[0]	IRQ_STATUS_FAULT	RO	Fault IRQ status Volatile: Yes Value After Reset: 0x0

15.5.3.48 TS_01_IRQ_CLEAR

- Description: TS-01 IRQ clear register, clears individual IRQ sources from the TS.
- Offset: 0x0108
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_TS_HHH	WO	Alarm B IRQ clear Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_TS_HHH	WO	Alarm A IRQ clear Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	WO	Sample done IRQ clear Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	WO	Fault IRQ clear Volatile: No Value After Reset: 0x0

15.5.3.49 TS_01_IRQ_TEST

- Description: TS-01 IRQ test register. Write to register will trigger a TS IRQ if the IRQ enabled.
- Offset: 0x010c

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_TS_HHH	RW	Alarm B IRQ test Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_TS_HHH	RW	Alarm A IRQ test Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	RW	Sample done IRQ test Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	RW	Fault IRQ test Volatile: No Value After Reset: 0x0

15.5.3.50 TS_01_SDIF_RDATA

- Description: TS-01 read data register
- Offset: 0x0110
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	SDIF_RDATA	RO	SDIF read data Volatile: Yes Value After Reset: 0x0

15.5.3.51 TS_01_SDIF_DONE

- Description: TS-01 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.
- Offset: 0x0114
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	

Bits	Field Name	Access	Description
[0]	SDIF_SMPL_DONE	RO	Sample done flag (active high). The sample done flag is asserted when a new data sample is made available. The sample done flag is automatically cleared when the associated 'data' register is read. Volatile: Yes Value After Reset: 0x0

15.5.3.52 TS_01_SDIF_DATA

- Description: TS-01 SDIF sample data register
- Offset: 0x0118
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	SAMPLE_FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	SAMPLE_TYPE	RO	Module sample type. 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the [TS|PD]_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.53 TS_01_ALARMA_CFG

- Description: TS-01 Alarm A configuration
- Offset: 0x0120
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.54 TS_01_ALARMB_CFG

- Description: TS-01 Alarm B configuration
- Offset: 0x0124
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.55 TS_01_SMPL_HILO

- Description: TS-01 sample max/min high/low value
- Offset: 0x0128
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.56 TS_01_HILO_RESET

- Description: TS-01 reset sample high/low register
- Offset: 0x012c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: No Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: No Value After Reset: 0x0

15.5.3.57 PD_CMN_CLK_SYNTH

- Description: PD clock synthesiser control register
- Offset: 0x0180
- Default Value: 0x10000

Bits	Field Name	Access	Description
[31:25]	RESERVED_2	-	
[24]	CLK_SYTH_EN	RW	Synthesized 'clk_ip' active high enable Volatile: No Value After Reset: 0x0
[23:20]	RESERVED_1	-	
[19:16]	CLK_SYNTH_HOLD	RW	SDA master to SDA slave output hold delay from posedge clk_ip and SDA slave to SDA master input setup delay from posedge 'clk_ip'. Expressed in units of 'clk_sys' cycles, the synth_strobe value must NOT exceed the synthesised clock period i.e. synth_setup <= synth_hi + synth_lo + 1. Volatile: No Value After Reset: 0x1
[15:8]	CLK_SYNTH_HI	RW	Synthesized 'clk_ip' high period zero indexed expressed in units of 'clk_sys' cycles.

Bits	Field Name	Access	Description
			Volatile: No Value After Reset: 0x0
[7:0]	CLK_SYNTH_LO	RW	Synthesized 'clk_ip' low period zero indexed expressed in units of 'clk_sys' cycles. Volatile: No Value After Reset: 0x0

15.5.3.58 PD_CMN_SDIF_DISABLE

- Description: PD SDIF disable (active high). When asserted completely disables the selected PD instance(s), by forcing the PD macro clock and reset low.
- Offset: 0x0184
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:0]	SDIF_DISABLE_PD_HHH	RW	Serial data interface (SDIF) disable (active high). When asserted completely disables the selected module instance(s), by forcing the module macro clock and reset low. Any disables should be applied before SDIF programming begins. e.g. setting sdif_disable = 8'b1000_1011 will disable module instances 0, 1, 3 & 7. Volatile: No Value After Reset: 0x0

15.5.3.59 PD_CMN_SDIF_STATUS

- Description: PD SDIF status register
- Offset: 0x0188
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SDIF_LOCK	RO	SDIF locked (active high). Set when slave auto mode is requested to indicate the SDIF is now a write only interface. Volatile: Yes Value After Reset: 0x0
[0]	SDIF_BUSY	RO	SDIF busy (active high). When asserted indicates the SDIF is busy so any SDIF programming requests will be

Bits	Field Name	Access	Description
			ignored. Or the clock synthesiser/disable SDIF state is being updated. Volatile: Yes Value After Reset: 0x0

15.5.3.60 PD_CMN_SDIF

- Description: PD SDIF write data register
- Offset: 0x018c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	SDIF_PROG	WO	Serial I/F program request (active high). This self-clearing bit will be ignored if the sdif_busy flag is set or if the sdif_lock flag is set and the request is a read request (sdif_wrn = 0). Volatile: No Value After Reset: 0x0
[30:28]	RESERVED_1	-	
[27]	SDIF_WRN	RW	Serial I/F Write NOT Read control bit 1: Write 0: Read Volatile: No Value After Reset: 0x0
[26:24]	SDIF_ADDR	RW	Serial I/F register address, SDIF_ADDR[1:0] Volatile: No Value After Reset: 0x0
[23:0]	SDIF_WDATA	RW	Serial I/F write data, SDIF_DATA[23:0] Volatile: No Value After Reset: 0x0

15.5.3.61 PD_CMN_SDIF_HALT

- Description: PD SDIF halt register. Halts all SDIF data transfer and resets SDIF slave.
- Offset: 0x0190
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_STOP	WO	Serial I/F write data. SDIF stop (active high). This self-clearing bit immediately stops all SDIF programming activity. The feature provides a means to terminate serial data interface activity in the unlikely event of it becoming locked, it should not be required during normal operation. Volatile: No Value After Reset: 0x0

15.5.3.62 PD_CMN_SDIF_CTRL

- Description: PD SDIF programming inhibit (active high). When asserted inhibits serial programming of the selected PD instance(s).
- Offset: 0x0194
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:0]	SDIF_INHIBIT_PD_HHH	RW	SDIF programming inhibit (active high). When asserted inhibits serial programming of the selected module instance(s). Inhibits should be applied before SDIF programming begins. e.g. setting sdif_inhibit = 8'b1000_1011 will disable programing of module instances 0, 1, 3 & 7. Volatile: No Value After Reset: 0x0

15.5.3.63 PD_CMN_SMPL_CTRL

- Description: PD SDIF sample counter control
- Offset: 0x01a0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	SMPL_DISCARD	RW	Sample discard (active high). This feature can be used to temporarily discard received data samples. When this bit is set data recovery is disabled but the external module may continue to run.

Bits	Field Name	Access	Description
			Volatile: No Value After Reset: 0x0
[1]	SMPL_CTR_HOLD	RW	Sample counter hold (active high). When asserted the sample counter is prevented from rolling over when the maximum sample count is reached. Volatile: No Value After Reset: 0x0
[0]	SMPL_CTR_DISABLE	RW	Sample counter disable (active high) 0x0: Sample counter enabled. 0x1: Sample counter disabled. Volatile: No Value After Reset: 0x0

15.5.3.64 PD_CMN_SMPL_CLR

- Description: PD SDIF sample counter clear
- Offset: 0x01a4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SMPL_CTR_DISABLE	WO	Sample counter clear (active high write). The sample counter value is set to zero when this selfclearing bit is written with '1'. Volatile: No Value After Reset: 0x0

15.5.3.65 PD_CMN_SMPL_CNT

- Description: PD SDIF sample counter current value
- Offset: 0x01a8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	SMPL_COUNT	RO	Sample counter. The 16-bit counter increments each time a new data sample is made available. The counter is cleared by writing '1' to 'smpl_ctr_clr'. The sample counter over-flow operation is determined by

Bits	Field Name	Access	Description
			'smpl_ctr_hold'. Volatile: Yes Value After Reset: 0x0

15.5.3.66 PD_00_IRQ_ENABLE

- Description: PD-00 IRQ enable register, enables individual IRQ sources from the PD.
- Offset: 0x01c0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_EN_ALARMB_PD_HHH	RW	Alarm B IRQ enable Volatile: No Value After Reset: 0x0
[3]	IRQ_EN_ALARMA_PD_HHH	RW	Alarm A IRQ enable Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_EN_DONE	RW	Sample done IRQ enable Volatile: No Value After Reset: 0x0
[0]	IRQ_EN_FAULT	RW	Fault IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.67 PD_00_IRQ_STATUS

- Description: PD-00 IRQ status register, reports status of individual IRQ sources from the PD.
- Offset: 0x01c4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_STATUS_ALARMB_PD_HHH	RO	Alarm B IRQ status Volatile: Yes Value After Reset: 0x0

Bits	Field Name	Access	Description
[3]	IRQ_STATUS_ALARMA_PD_HHH	RO	Alarm A IRQ status Volatile: Yes Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_STATUS_DONE	RO	Sample done IRQ status Volatile: Yes Value After Reset: 0x0
[0]	IRQ_STATUS_FAULT	RO	Fault IRQ status Volatile: Yes Value After Reset: 0x0

15.5.3.68 PD_00_IRQ_CLEAR

- Description: PD-00 IRQ clear register, clears individual IRQ sources from the PD.
- Offset: 0x01c8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	WO	Alarm B IRQ clear Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	WO	Alarm A IRQ clear Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	WO	Sample done IRQ clear Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	WO	Fault IRQ clear Volatile: No Value After Reset: 0x0

15.5.3.69 PD_00_IRQ_TEST

- Description: PD-00 IRQ test register. Write to register will trigger an PD IRQ if the IRQ enabled.

- Offset: 0x01cc
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	RW	Alarm B IRQ test Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	RW	Alarm A IRQ test Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	RW	Sample done IRQ test Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	RW	Fault IRQ test Volatile: No Value After Reset: 0x0

15.5.3.70 PD_00_SDIF_RDATA

- Description: PD-00 read data register
- Offset: 0x01d0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	SDIF_RDATA	RO	SDIF read data Volatile: Yes Value After Reset: 0x0

15.5.3.71 PD_00_SDIF_DONE

- Description: PD-00 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.
- Offset: 0x01d4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_SMPL_DONE	RO	Sample done flag (active high). The sample done flag is asserted when a new data sample is made available. The sample done flag is automatically cleared when the associated 'data' register is read. Volatile: Yes Value After Reset: 0x0

15.5.3.72 PD_00_SDIF_DATA

- Description: PD-00 SDIF sample data register
- Offset: 0x01d8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	SAMPLE_FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	SAMPLE_TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the [TS|PD]_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.73 PD_00_ALARMA_CFG

- Description: PD-00 Alarm A configuration
- Offset: 0x01e0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.74 PD_00_ALARMB_CFG

- Description: PD-00 Alarm B configuration
- Offset: 0x01e4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.75 PD_00_SMPL_HILO

- Description: PD-00 sample max/min high/low value
- Offset: 0x01e8
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.76 PD_00_HILO_RESET

- Description: PD-00 reset sample high/low register
- Offset: 0x01ec
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: No Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: No Value After Reset: 0x0

15.5.3.77 PD_01_IRQ_ENABLE

- Description: PD-01 IRQ enable register, enables individual IRQ sources from the PD.
- Offset: 0x0200
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_EN_ALARMB_PD_HHH	RW	Alarm B IRQ enable Volatile: No Value After Reset: 0x0
[3]	IRQ_EN_ALARMA_PD_HHH	RW	Alarm A IRQ enable Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_EN_DONE	RW	Sample done IRQ enable Volatile: No Value After Reset: 0x0
[0]	IRQ_EN_FAULT	RW	Fault IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.78 PD_01_IRQ_STATUS

- Description: PD-01 IRQ status register, reports status of individual IRQ sources from the PD.
- Offset: 0x0204
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_STATUS_ALARMB_PD_HHH	RO	Alarm B IRQ status Volatile: Yes Value After Reset: 0x0
[3]	IRQ_STATUS_ALARMA_PD_HHH	RO	Alarm A IRQ status Volatile: Yes Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_STATUS_DONE	RO	Sample done IRQ status Volatile: Yes Value After Reset: 0x0
[0]	IRQ_STATUS_FAULT	RO	Fault IRQ status Volatile: Yes Value After Reset: 0x0

15.5.3.79 PD_01_IRQ_CLEAR

- Description: PD-01 IRQ clear register, clears individual IRQ sources from the PD.
- Offset: 0x0208
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	WO	Alarm B IRQ clear Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	WO	Alarm A IRQ clear Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	

Bits	Field Name	Access	Description
[1]	IRQ_CLR_DONE	WO	Sample done IRQ clear Volatile: No. Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	WO	Fault IRQ clear Volatile: No Value After Reset: 0x0

15.5.3.80 PD_01_IRQ_TEST

- Description: PD-01 IRQ test register. Write to register will trigger an PD IRQ if the IRQ enabled.
- Offset: 0x020c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	RW	Alarm B IRQ test Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	RW	Alarm A IRQ test Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	RW	Sample done IRQ test Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	RW	Fault IRQ test Volatile: No Value After Reset: 0x0

15.5.3.81 PD_01_SDIF_RDATA

- Description: PD-01 read data register
- Offset: 0x0210
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	

Bits	Field Name	Access	Description
[23:0]	SDIF_RDATA	RO	SDIF read data Volatile: Yes Value After Reset: 0x0

15.5.3.82 PD_01_SDIF_DONE

- Description: PD-01 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.
- Offset: 0x0214
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_SMPL_DONE	RO	Sample done flag (active high). The sample done flag is asserted when a new data sample is made available. The sample done flag is automatically cleared when the associated 'data' register is read. Volatile: Yes Value After Reset: 0x0

15.5.3.83 PD_01_SDIF_DATA

- Description: PD-01 SDIF sample data register
- Offset: 0x0218
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	SAMPLE_FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	SAMPLE_TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0

Bits	Field Name	Access	Description
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the [TS|PD]_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.84 PD_01_ALARMA_CFG

- Description: PD-01 Alarm A configuration
- Offset: 0x0220
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.85 PD_01_ALARMB_CFG

- Description: PD-01 Alarm B configuration
- Offset: 0x0224
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.86 PD_01_SMPL_HILO

- Description: PD-01 sample max/min high/low value
- Offset: 0x0228
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.87 PD_01_HILO_RESET

- Description: PD-01 reset sample high/low register
- Offset: 0x022c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: No Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: No Value After Reset: 0x0

15.5.3.88 PD_02_IRQ_ENABLE

- Description: PD-02 IRQ enable register, enables individual IRQ sources from the PD.
- Offset: 0x0240
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	

Bits	Field Name	Access	Description
[4]	IRQ_EN_ALARMB_PD_HHH	RW	Alarm B IRQ enable Volatile: No Value After Reset: 0x0
[3]	IRQ_EN_ALARMA_PD_HHH	RW	Alarm A IRQ enable Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_EN_DONE	RW	Sample done IRQ enable Volatile: No Value After Reset: 0x0
[0]	IRQ_EN_FAULT	RW	Fault IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.89 PD_02_IRQ_STATUS

- Description: PD-02 IRQ status register, reports status of individual IRQ sources from the PD.
- Offset: 0x0244
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_STATUS_ALARMB_PD_HHH	RO	Alarm B IRQ status Volatile: Yes Value After Reset: 0x0
[3]	IRQ_STATUS_ALARMA_PD_HHH	RO	Alarm A IRQ status Volatile: Yes Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_STATUS_DONE	RO	Sample done IRQ status Volatile: Yes Value After Reset: 0x0
[0]	IRQ_STATUS_FAULT	RO	Fault IRQ status Volatile: Yes Value After Reset: 0x0

15.5.3.90 PD_02_IRQ_CLEAR

- Description: PD-02 IRQ clear register, clears individual IRQ sources from the PD.
- Offset: 0x0248
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	WO	Alarm B IRQ clear Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	WO	Alarm A IRQ clear Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	WO	Sample done IRQ clear Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	WO	Fault IRQ clear Volatile: No Value After Reset: 0x0

15.5.3.91 PD_02_IRQ_TEST

- Description: PD-02 IRQ test register. Write to register will trigger an PD IRQ if the IRQ enabled.
- Offset: 0x024c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	RW	Alarm B IRQ test Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	RW	Alarm A IRQ test Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	

Bits	Field Name	Access	Description
[1]	IRQ_CLR_DONE	RW	Sample done IRQ test Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	RW	Fault IRQ test Volatile: No Value After Reset: 0x0

15.5.3.92 PD_02_SDIF_RDATA

- Description: PD-02 read data register
- Offset: 0x0250
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	SDIF_RDATA	RO	SDIF read data Volatile: Yes Value After Reset: 0x0

15.5.3.93 PD_02_SDIF_DONE

- Description: PD-02 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.
- Offset: 0x0254
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_SMPL_DONE	RO	Sample done flag (active high). The sample done flag is asserted when a new data sample is made available. The sample done flag is automatically cleared when the associated 'data' register is read. Volatile: Yes Value After Reset: 0x0

15.5.3.94 PD_02_SDIF_DATA

- Description: PD-02 SDIF sample data register
- Offset: 0x0258

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	SAMPLE_FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	SAMPLE_TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the [TS|PD]_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.95 PD_02_ALARMA_CFG

- Description: PD-02 Alarm A configuration
- Offset: 0x0260
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.96 PD_02_ALARMB_CFG

- Description: PD-02 Alarm B configuration

- Offset: 0x0264
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.97 PD_02_SMPL_HILO

- Description: PD-02 sample max/min high/low value
- Offset: 0x0268
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.98 PD_02_HILO_RESET

- Description: PD-02 reset sample high/low register
- Offset: 0x026c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: No Value After Reset: 0x0

Bits	Field Name	Access	Description
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: No Value After Reset: 0x0

15.5.3.99 PD_03_IRQ_ENABLE

- Description: PD-03 IRQ enable register, enables individual IRQ sources from the PD.
- Offset: 0x0280
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_EN_ALARMB_PD_HHH	RW	Alarm B IRQ enable Volatile: No Value After Reset: 0x0
[3]	IRQ_EN_ALARMA_PD_HHH	RW	Alarm A IRQ enable Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_EN_DONE	RW	Sample done IRQ enable Volatile: No Value After Reset: 0x0
[0]	IRQ_EN_FAULT	RW	Fault IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.100 PD_03_IRQ_STATUS

- Description: PD-03 IRQ status register, reports status of individual IRQ sources from the PD.
- Offset: 0x0284
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_STATUS_ALARMB_PD_HHH	RO	Alarm B IRQ status Volatile: Yes

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[3]	IRQ_STATUS_ALARMA_PD_HHH	RO	Alarm A IRQ status Volatile: Yes Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_STATUS_DONE	RO	Sample done IRQ status Volatile: Yes Value After Reset: 0x0
[0]	IRQ_STATUS_FAULT	RO	Fault IRQ status Volatile: Yes Value After Reset: 0x0

15.5.3.101 PD_03_IRQ_CLEAR

- Description: PD-03 IRQ clear register, clears individual IRQ sources from the PD.
- Offset: 0x0288
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	WO	Alarm B IRQ clear Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	WO	Alarm A IRQ clear Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	WO	Sample done IRQ clear Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	WO	Fault IRQ clear Volatile: No Value After Reset: 0x0

15.5.3.102 PD_03_IRQ_TEST

- Description: PD-03 IRQ test register. Write to register will trigger a PD IRQ if the IRQ enabled.
- Offset: 0x028c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	RW	Alarm B IRQ test Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	RW	Alarm A IRQ test Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	RW	Sample done IRQ test Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	RW	Fault IRQ test Volatile: No Value After Reset: 0x0

15.5.3.103 PD_03_SDIF_RDATA

- Description: PD-03 read data register
- Offset: 0x0290
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	SDIF_RDATA	RO	SDIF read data Volatile: Yes Value After Reset: 0x0

15.5.3.104 PD_03_SDIF_DONE

- Description: PD-03 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.
- Offset: 0x0294

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_SMPL_DONE	RO	Sample done flag (active high). The sample done flag is asserted when a new data sample is made available. The sample done flag is automatically cleared when the associated 'data' register is read. Volatile: Yes Value After Reset: 0x0

15.5.3.105 PD_03_SDIF_DATA

- Description: PD-03 SDIF sample data register
- Offset: 0x0298
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	SAMPLE_FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	SAMPLE_TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the [TS|PD]_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.106 PD_03_ALARMA_CFG

- Description: PD-03 Alarm A configuration
- Offset: 0x02a0

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.107 PD_03_ALARMB_CFG

- Description: PD-03 Alarm B configuration
- Offset: 0x02a4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.108 PD_03_SMPL_HILO

- Description: PD-03 sample max/min high/low value
- Offset: 0x02a8
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes

Bits	Field Name	Access	Description
			Value After Reset: 0xFFFF

15.5.3.109 PD_03_HILO_RESET

- Description: PD-03 reset sample high/low register
- Offset: 0x02ac
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: No Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: No Value After Reset: 0x0

15.5.3.110 PD_04_IRQ_ENABLE

- Description: PD-04 IRQ enable register, enables individual IRQ sources from the PD.
- Offset: 0x02c0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_EN_ALARMB_PD_HHH	RW	Alarm B IRQ enable Volatile: No Value After Reset: 0x0
[3]	IRQ_EN_ALARMA_PD_HHH	RW	Alarm A IRQ enable Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_EN_DONE	RW	Sample done IRQ enable Volatile: No Value After Reset: 0x0

Bits	Field Name	Access	Description
[0]	IRQ_EN_FAULT	RW	Fault IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.111 PD_04_IRQ_STATUS

- Description: PD-04 IRQ status register, reports status of individual IRQ sources from the PD.
- Offset: 0x02c4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_STATUS_ALARMB_PD_HHH	RO	Alarm B IRQ status Volatile: Yes Value After Reset: 0x0
[3]	IRQ_STATUS_ALARMA_PD_HHH	RO	Alarm A IRQ status Volatile: Yes Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_STATUS_DONE	RO	Sample done IRQ status Volatile: Yes Value After Reset: 0x0
[0]	IRQ_STATUS_FAULT	RO	Fault IRQ status Volatile: Yes Value After Reset: 0x0

15.5.3.112 PD_04_IRQ_CLEAR

- Description: PD-04 IRQ clear register, clears individual IRQ sources from the PD.
- Offset: 0x02c8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	WO	Alarm B IRQ clear Volatile: No Value After Reset: 0x0

Bits	Field Name	Access	Description
[3]	IRQ_CLR_ALARMA_PD_HHH	WO	Alarm A IRQ clear Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	WO	Sample done IRQ clear Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	WO	Fault IRQ clear Volatile: No Value After Reset: 0x0

15.5.3.113 PD_04_IRQ_TEST

- Description: PD-04 IRQ test register. Write to register will trigger a PD IRQ if the IRQ enabled.
- Offset: 0x02cc
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	RW	Alarm B IRQ test Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	RW	Alarm A IRQ test Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	RW	Sample done IRQ test Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	RW	Fault IRQ test Volatile: No Value After Reset: 0x0

15.5.3.114 PD_04_SDIF_RDATA

- Description: PD-04 read data register

- Offset: 0x02d0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	SDIF_RDATA	RO	SDIF read data Volatile: Yes Value After Reset: 0x0

15.5.3.115 PD_04_SDIF_DONE

- Description: PD-04 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.
- Offset: 0x02d4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_SMPL_DONE	RO	Sample done flag (active high). The sample done flag is asserted when a new data sample is made available. The sample done flag is automatically cleared when the associated 'data' register is read. Volatile: Yes Value After Reset: 0x0

15.5.3.116 PD_04_SDIF_DATA

- Description: PD-04 SDIF sample data register
- Offset: 0x02d8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	SAMPLE_FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	SAMPLE_TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select

Bits	Field Name	Access	Description
			or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the [TS|PD]_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.117 PD_04_ALARMA_CFG

- Description: PD-04 Alarm A configuration
- Offset: 0x02e0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.118 PD_04_ALARMB_CFG

- Description: PD-04 Alarm B configuration
- Offset: 0x02e4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration.

Bits	Field Name	Access	Description
			Volatile: No Value After Reset: 0x0

15.5.3.119 PD_04_SMPL_HILO

- Description: PD-04 sample max/min high/low value
- Offset: 0x02e8
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.120 PD_04_HILO_RESET

- Description: PD-04 reset sample high/low register
- Offset: 0x02ec
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: No Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: No Value After Reset: 0x0

15.5.3.121 PD_05_IRQ_ENABLE

- Description: PD-05 IRQ enable register, enables individual IRQ sources from the PD.
- Offset: 0x0300
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_EN_ALARMB_PD_HHH	RW	Alarm B IRQ enable Volatile: No Value After Reset: 0x0
[3]	IRQ_EN_ALARMA_PD_HHH	RW	Alarm A IRQ enable Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_EN_DONE	RW	Sample done IRQ enable Volatile: No Value After Reset: 0x0
[0]	IRQ_EN_FAULT	RW	Fault IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.122 PD_05_IRQ_STATUS

- Description: PD-05 IRQ status register, reports status of individual IRQ sources from the PD.
- Offset: 0x0304
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_STATUS_ALARMB_PD_HHH	RO	Alarm B IRQ status Volatile: Yes Value After Reset: 0x0
[3]	IRQ_STATUS_ALARMA_PD_HHH	RO	Alarm A IRQ status Volatile: Yes Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_STATUS_DONE	RO	Sample done IRQ status Volatile: Yes Value After Reset: 0x0
[0]	IRQ_STATUS_FAULT	RO	Fault IRQ status

Bits	Field Name	Access	Description
			Volatile: Yes Value After Reset: 0x0

15.5.3.123 PD_05_IRQ_CLEAR

- Description: PD-05 IRQ clear register, clears individual IRQ sources from the PD.
- Offset: 0x0308
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	WO	Alarm B IRQ clear Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	WO	Alarm A IRQ clear Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	WO	Sample done IRQ clear Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	WO	Fault IRQ clear Volatile: No Value After Reset: 0x0

15.5.3.124 PD_05_IRQ_TEST

- Description: PD-05 IRQ test register. Write to register will trigger an PD IRQ if the IRQ enabled.
- Offset: 0x030c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	RW	Alarm B IRQ test Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	RW	Alarm A IRQ test

Bits	Field Name	Access	Description
			Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	RW	Sample done IRQ test Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	RW	Fault IRQ test Volatile: No Value After Reset: 0x0

15.5.3.125 PD_05_SDIF_RDATA

- Description: PD-05 read data register
- Offset: 0x0310
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	SDIF_RDATA	RO	SDIF read data Volatile: Yes Value After Reset: 0x0

15.5.3.126 PD_05_SDIF_DONE

- Description: PD-05 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.
- Offset: 0x0314
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_SMPL_DONE	RO	Sample done flag (active high). The sample done flag is asserted when a new data sample is made available. The sample done flag is automatically cleared when the associated 'data' register is read. Volatile: Yes Value After Reset: 0x0

15.5.3.127 PD_05_SDIF_DATA

- Description: PD-05 SDIF sample data register
- Offset: 0x0318
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	SAMPLE_FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	SAMPLE_TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the [TS|PD]_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.128 PD_05_ALARMA_CFG

- Description: PD-05 Alarm A configuration
- Offset: 0x0320
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.129 PD_05_ALARMB_CFG

- Description: PD-05 Alarm B configuration
- Offset: 0x0324
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.130 PD_05_SMPL_HILO

- Description: PD-05 sample max/min high/low value
- Offset: 0x0328
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.131 PD_05_HILO_RESET

- Description: PD-05 reset sample high/low register
- Offset: 0x032c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written.

Bits	Field Name	Access	Description
			Volatile: No Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: No Value After Reset: 0x0

15.5.3.132 PD_06_IRQ_ENABLE

- Description: PD-06 IRQ enable register, enables individual IRQ sources from the PD.
- Offset: 0x0340
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_EN_ALARMB_PD_HHH	RW	Alarm B IRQ enable Volatile: No Value After Reset: 0x0
[3]	IRQ_EN_ALARMA_PD_HHH	RW	Alarm A IRQ enable Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_EN_DONE	RW	Sample done IRQ enable Volatile: No Value After Reset: 0x0
[0]	IRQ_EN_FAULT	RW	Fault IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.133 PD_06_IRQ_STATUS

- Description: PD-06 IRQ status register, reports status of individual IRQ sources from the PD.
- Offset: 0x0344
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	

Bits	Field Name	Access	Description
[4]	IRQ_STATUS_ALARMB_PD_HHH	RO	Alarm B IRQ status Volatile: Yes Value After Reset: 0x0
[3]	IRQ_STATUS_ALARMA_PD_HHH	RO	Alarm A IRQ status Volatile: Yes Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_STATUS_DONE	RO	Sample done IRQ status Volatile: Yes Value After Reset: 0x0
[0]	IRQ_STATUS_FAULT	RO	Fault IRQ status Volatile: Yes Value After Reset: 0x0

15.5.3.134 PD_06_IRQ_CLEAR

- Description: PD-06 IRQ clear register, clears individual IRQ sources from the PD.
- Offset: 0x0348
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	WO	Alarm B IRQ clear Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	WO	Alarm A IRQ clear Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	WO	Sample done IRQ clear Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	WO	Fault IRQ clear Volatile: No Value After Reset: 0x0

15.5.3.135 PD_06_IRQ_TEST

- Description: PD-06 IRQ test register. Write to register will trigger an PD IRQ if the IRQ enabled.
- Offset: 0x034c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	RW	Alarm B IRQ test Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	RW	Alarm A IRQ test Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	RW	Sample done IRQ test Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	RW	Fault IRQ test Volatile: No Value After Reset: 0x0

15.5.3.136 PD_06_SDIF_RDATA

- Description: PD-06 read data register
- Offset: 0x0350
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	SDIF_RDATA	RO	SDIF read data Volatile: Yes Value After Reset: 0x0

15.5.3.137 PD_06_SDIF_DONE

- Description: PD-06 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.
- Offset: 0x0354

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_SMPL_DONE	RO	Sample done flag (active high). The sample done flag is asserted when a new data sample is made available. The sample done flag is automatically cleared when the associated 'data' register is read. Volatile: Yes Value After Reset: 0x0

15.5.3.138 PD_06_SDIF_DATA

- Description: PD-06 SDIF sample data register
- Offset: 0x0358
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	SAMPLE_FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	SAMPLE_TYPE	RO	Module sample type. 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the [TS|PD]_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.139 PD_06_ALARMA_CFG

- Description: PD-06 Alarm A configuration
- Offset: 0x0360

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.140 PD_06_ALARMB_CFG

- Description: PD-06 Alarm B configuration
- Offset: 0x0364
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.141 PD_06_SMPL_HILO

- Description: PD-06 sample max/min high/low value
- Offset: 0x0368
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes

Bits	Field Name	Access	Description
			Value After Reset: 0xFFFF

15.5.3.142 PD_06_HILO_RESET

- Description: PD-06 reset sample high/low register
- Offset: 0x036c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: No Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: No Value After Reset: 0x0

15.5.3.143 PD_07_IRQ_ENABLE

- Description: PD-07 IRQ enable register, enables individual IRQ sources from the PD.
- Offset: 0x0380
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_EN_ALARMB_PD_HHH	RW	Alarm B IRQ enable Volatile: No Value After Reset: 0x0
[3]	IRQ_EN_ALARMA_PD_HHH	RW	Alarm A IRQ enable Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_EN_DONE	RW	Sample done IRQ enable Volatile: No Value After Reset: 0x0

Bits	Field Name	Access	Description
[0]	IRQ_EN_FAULT	RW	Fault IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.144 PD_07_IRQ_STATUS

- Description: PD-07 IRQ status register, reports status of individual IRQ sources from the PD.
- Offset: 0x0384
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_STATUS_ALARMB_PD_HHH	RO	Alarm B IRQ status Volatile: Yes Value After Reset: 0x0
[3]	IRQ_STATUS_ALARMA_PD_HHH	RO	Alarm A IRQ status Volatile: Yes Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_STATUS_DONE	RO	Sample done IRQ status Volatile: Yes Value After Reset: 0x0
[0]	IRQ_STATUS_FAULT	RO	Fault IRQ status Volatile: Yes Value After Reset: 0x0

15.5.3.145 PD_07_IRQ_CLEAR

- Description: PD-07 IRQ clear register, clears individual IRQ sources from the PD.
- Offset: 0x0388
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	WO	Alarm B IRQ clear Volatile: No Value After Reset: 0x0

Bits	Field Name	Access	Description
[3]	IRQ_CLR_ALARMA_PD_HHH	WO	Alarm A IRQ clear Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	WO	Sample done IRQ clear Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	WO	Fault IRQ clear Volatile: No Value After Reset: 0x0

15.5.3.146 PD_07_IRQ_TEST

- Description: PD-07 IRQ test register. Write to register will trigger a PD IRQ if the IRQ enabled.
- Offset: 0x038c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	RW	Alarm B IRQ test Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	RW	Alarm A IRQ test Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	RW	Sample done IRQ test Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	RW	Fault IRQ test Volatile: No Value After Reset: 0x0

15.5.3.147 PD_07_SDIF_RDATA

- Description: PD-07 read data register

- Offset: 0x0390
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	SDIF_RDATA	RO	SDIF read data Volatile: Yes Value After Reset: 0x0

15.5.3.148 PD_07_SDIF_DONE

- Description: PD-07 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.
- Offset: 0x0394
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_SMPL_DONE	RO	Sample done flag (active high). The sample done flag is asserted when a new data sample is made available. The sample done flag is automatically cleared when the associated 'data' register is read. Volatile: Yes Value After Reset: 0x0

15.5.3.149 PD_07_SDIF_DATA

- Description: PD-07 SDIF sample data register
- Offset: 0x0398
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	SAMPLE_FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	SAMPLE_TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select

Bits	Field Name	Access	Description
			or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the [TS|PD]_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.150 PD_07_ALARMA_CFG

- Description: PD-07 Alarm A configuration
- Offset: 0x03a0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.151 PD_07_ALARMB_CFG

- Description: PD-07 Alarm B configuration
- Offset: 0x03a4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration.

Bits	Field Name	Access	Description
			Volatile: No Value After Reset: 0x0

15.5.3.152 PD_07_SMPL_HILO

- Description: PD-07 sample max/min high/low value
- Offset: 0x03a8
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.153 PD_07_HILO_RESET

- Description: PD-07 reset sample high/low register
- Offset: 0x03ac
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: No Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: No Value After Reset: 0x0

15.5.3.154 PD_08_IRQ_ENABLE

- Description: PD-08 IRQ enable register, enables individual IRQ sources from the PD.
- Offset: 0x03c0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_EN_ALARMB_PD_HHH	RW	Alarm B IRQ enable Volatile: No Value After Reset: 0x0
[3]	IRQ_EN_ALARMA_PD_HHH	RW	Alarm A IRQ enable Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_EN_DONE	RW	Sample done IRQ enable Volatile: No Value After Reset: 0x0
[0]	IRQ_EN_FAULT	RW	Fault IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.155 PD_08_IRQ_STATUS

- Description: PD-08 IRQ status register, reports status of individual IRQ sources from the PD.
- Offset: 0x03c4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_STATUS_ALARMB_PD_HHH	RO	Alarm B IRQ status Volatile: Yes Value After Reset: 0x0
[3]	IRQ_STATUS_ALARMA_PD_HHH	RO	Alarm A IRQ status Volatile: Yes Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_STATUS_DONE	RO	Sample done IRQ status Volatile: Yes Value After Reset: 0x0
[0]	IRQ_STATUS_FAULT	RO	Fault IRQ status

Bits	Field Name	Access	Description
			Volatile: Yes Value After Reset: 0x0

15.5.3.156 PD_08_IRQ_CLEAR

- Description: PD-08 IRQ clear register, clears individual IRQ sources from the PD.
- Offset: 0x03c8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	WO	Alarm B IRQ clear Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	WO	Alarm A IRQ clear Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	WO	Sample done IRQ clear Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	WO	Fault IRQ clear Volatile: No Value After Reset: 0x0

15.5.3.157 PD_08_IRQ_TEST

- Description: PD-08 IRQ test register. Write to register will trigger a PD IRQ if the IRQ enabled.
- Offset: 0x03cc
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	RW	Alarm B IRQ test Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	RW	Alarm A IRQ test

Bits	Field Name	Access	Description
			Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	RW	Sample done IRQ test Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	RW	Fault IRQ test Volatile: No Value After Reset: 0x0

15.5.3.158 PD_08_SDIF_RDATA

- Description: PD-08 read data register
- Offset: 0x03d0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	SDIF_RDATA	RO	SDIF read data Volatile: Yes Value After Reset: 0x0

15.5.3.159 PD_08_SDIF_DONE

- Description: PD-08 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.
- Offset: 0x03d4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_SMPL_DONE	RO	Sample done flag (active high). The sample done flag is asserted when a new data sample is made available. The sample done flag is automatically cleared when the associated 'data' register is read. Volatile: Yes Value After Reset: 0x0

15.5.3.160 PD_08_SDIF_DATA

- Description: PD-08 SDIF sample data register
- Offset: 0x03d8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	SAMPLE_FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	SAMPLE_TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the [TS|PD]_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.161 PD_08_ALARMA_CFG

- Description: PD-08 Alarm A configuration
- Offset: 0x03e0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.162 PD_08_ALARMB_CFG

- Description: PD-08 Alarm B configuration
- Offset: 0x03e4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.163 PD_08_SMPL_HILO

- Description: PD-08 sample max/min high/low value
- Offset: 0x03e8
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.164 PD_08_HILO_RESET

- Description: PD-08 reset sample high/low register
- Offset: 0x03ec
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written.

Bits	Field Name	Access	Description
			Volatile: No Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: No Value After Reset: 0x0

15.5.3.165 PD_09_IRQ_ENABLE

- Description: PD-09 IRQ enable register, enables individual IRQ sources from the PD.
- Offset: 0x0400
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_EN_ALARMB_PD_HHH	RW	Alarm B IRQ enable Volatile: No Value After Reset: 0x0
[3]	IRQ_EN_ALARMA_PD_HHH	RW	Alarm A IRQ enable Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_EN_DONE	RW	Sample done IRQ enable Volatile: No Value After Reset: 0x0
[0]	IRQ_EN_FAULT	RW	Fault IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.166 PD_09_IRQ_STATUS

- Description: PD-09 IRQ status register, reports status of individual IRQ sources from the PD.
- Offset: 0x0404
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	

Bits	Field Name	Access	Description
[4]	IRQ_STATUS_ALARMB_PD_HHH	RO	Alarm B IRQ status Volatile: Yes Value After Reset: 0x0
[3]	IRQ_STATUS_ALARMA_PD_HHH	RO	Alarm A IRQ status Volatile: Yes Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_STATUS_DONE	RO	Sample done IRQ status Volatile: Yes Value After Reset: 0x0
[0]	IRQ_STATUS_FAULT	RO	Fault IRQ status Volatile: Yes Value After Reset: 0x0

15.5.3.167 PD_09_IRQ_CLEAR

- Description: PD-09 IRQ clear register, clears individual IRQ sources from the PD.
- Offset: 0x0408
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	WO	Alarm B IRQ clear Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	WO	Alarm A IRQ clear Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	WO	Sample done IRQ clear Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	WO	Fault IRQ clear Volatile: No Value After Reset: 0x0

15.5.3.168 PD_09_IRQ_TEST

- Description: PD-09 IRQ test register. Write to register will trigger an PD IRQ if the IRQ enabled.
- Offset: 0x040c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	RW	Alarm B IRQ test Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	RW	Alarm A IRQ test Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	RW	Sample done IRQ test Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	RW	Fault IRQ test Volatile: No Value After Reset: 0x0

15.5.3.169 PD_09_SDIF_RDATA

- Description: PD-09 read data register
- Offset: 0x0410
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	SDIF_RDATA	RO	SDIF read data Volatile: Yes Value After Reset: 0x0

15.5.3.170 PD_09_SDIF_DONE

- Description: PD-09 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.
- Offset: 0x0414

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_SMPL_DONE	RO	Sample done flag (active high). The sample done flag is asserted when a new data sample is made available. The sample done flag is automatically cleared when the associated 'data' register is read. Volatile: Yes Value After Reset: 0x0

15.5.3.171 PD_09_SDIF_DATA

- Description: PD-09 SDIF sample data register
- Offset: 0x0418
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	SAMPLE_FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	SAMPLE_TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the [TS|PD]_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.172 PD_09_ALARMA_CFG

- Description: PD-09 Alarm A configuration
- Offset: 0x0420

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.173 PD_09_ALARMB_CFG

- Description: PD-09 Alarm B configuration
- Offset: 0x0424
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.174 PD_09_SMPL_HILO

- Description: PD-09 sample max/min high/low value
- Offset: 0x0428
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes

Bits	Field Name	Access	Description
			Value After Reset: 0xFFFF

15.5.3.175 PD_09_HILO_RESET

- Description: PD-09 reset sample high/low register
- Offset: 0x042c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: No Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: No Value After Reset: 0x0

15.5.3.176 PD_10_IRQ_ENABLE

- Description: PD-10 IRQ enable register, enables individual IRQ sources from the PD.
- Offset: 0x0440
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_EN_ALARMB_PD_HHH	RW	Alarm B IRQ enable Volatile: No Value After Reset: 0x0
[3]	IRQ_EN_ALARMA_PD_HHH	RW	Alarm A IRQ enable. Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_EN_DONE	RW	Sample done IRQ enable Volatile: No Value After Reset: 0x0

Bits	Field Name	Access	Description
[0]	IRQ_EN_FAULT	RW	Fault IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.177 PD_10_IRQ_STATUS

- Description: PD-10 IRQ status register, reports status of individual IRQ sources from the PD.
- Offset: 0x0444
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_STATUS_ALARMB_PD_HHH	RO	Alarm B IRQ status Volatile: Yes Value After Reset: 0x0
[3]	IRQ_STATUS_ALARMA_PD_HHH	RO	Alarm A IRQ status Volatile: Yes Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_STATUS_DONE	RO	Sample done IRQ status Volatile: Yes Value After Reset: 0x0
[0]	IRQ_STATUS_FAULT	RO	Fault IRQ status Volatile: Yes Value After Reset: 0x0

15.5.3.178 PD_10_IRQ_CLEAR

- Description: PD-10 IRQ clear register, clears individual IRQ sources from the PD.
- Offset: 0x0448
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	WO	Alarm B IRQ clear Volatile: No Value After Reset: 0x0

Bits	Field Name	Access	Description
[3]	IRQ_CLR_ALARMA_PD_HHH	WO	Alarm A IRQ clear Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	WO	Sample done IRQ clear Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	WO	Fault IRQ clear Volatile: No Value After Reset: 0x0

15.5.3.179 PD_10_IRQ_TEST

- Description: PD-10 IRQ test register. Write to register will trigger an PD IRQ if the IRQ enabled.
- Offset: 0x044c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_2	-	
[4]	IRQ_CLR_ALARMB_PD_HHH	RW	Alarm B IRQ test Volatile: No Value After Reset: 0x0
[3]	IRQ_CLR_ALARMA_PD_HHH	RW	Alarm A IRQ test Volatile: No Value After Reset: 0x0
[2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	RW	Sample done IRQ test Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	RW	Fault IRQ test Volatile: No Value After Reset: 0x0

15.5.3.180 PD_10_SDIF_RDATA

- Description: PD-10 read data register

- Offset: 0x0450
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	SDIF_RDATA	RO	SDIF read data Volatile: Yes Value After Reset: 0x0

15.5.3.181 PD_10_SDIF_DONE

- Description: PD-10 SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.
- Offset: 0x0454
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_SMPL_DONE	RO	Sample done flag (active high). The sample done flag is asserted when a new data sample is made available. The sample done flag is automatically cleared when the associated 'data' register is read. Volatile: Yes Value After Reset: 0x0

15.5.3.182 PD_10_SDIF_DATA

- Description: PD-10 SDIF sample data register
- Offset: 0x0458
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	SAMPLE_FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	SAMPLE_TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select

Bits	Field Name	Access	Description
			or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the [TS|PD]_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.183 PD_10_ALARMA_CFG

- Description: PD-10 Alarm A configuration
- Offset: 0x0460
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.184 PD_10_ALARMB_CFG

- Description: PD-10 Alarm B configuration
- Offset: 0x0464
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration.

Bits	Field Name	Access	Description
			Volatile: No Value After Reset: 0x0

15.5.3.185 PD_10_SMPL_HILO

- Description: PD-10 sample max/min high/low value
- Offset: 0x0468
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.186 PD_10_HILO_RESET

- Description: PD-10 Reset sample high/low register
- Offset: 0x046c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: No Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: No Value After Reset: 0x0

15.5.3.187 VM_CMN_CLK_SYNTH

- Description: VM Clock Synthesiser control register
- Offset: 0x0800
- Default Value: 0x10000

Bits	Field Name	Access	Description
[31:25]	RESERVED_2	-	
[24]	CLK_SYTH_EN	RW	Synthesized 'clk_ip' active high enable Volatile: No Value After Reset: 0x0
[23:20]	RESERVED_1	-	
[19:16]	CLK_SYNTH_HOLD	RW	SDA master to SDA slave output hold delay from posedge clk_ip and SDA slave to SDA master input setup delay from posedge 'clk_ip'. Expressed in units of 'clk_sys' cycles, the synth_strobe value must NOT exceed the synthesised clock period i.e. synth_setup <= synth_hi + synth_lo + 1. Volatile: No Value After Reset: 0x1
[15:8]	CLK_SYNTH_HI	RW	Synthesized 'clk_ip' high period zero indexed expressed in units of 'clk_sys' cycles. Volatile: No Value After Reset: 0x0
[7:0]	CLK_SYNTH_LO	RW	Synthesized 'clk_ip' low period zero indexed expressed in units of 'clk_sys' cycles. Volatile: No Value After Reset: 0x0

15.5.3.188 VM_CMN_SDIF_DISABLE

- Description: VM SDIF disable (active high). When asserted completely disables the selected VM instance(s), by forcing the VM macro clock and reset low.
- Offset: 0x0804
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_DISABLE	RW	SDIF disable (active high). When asserted completely disables the selected module instance(s), by forcing the module macro clock and reset low. Any disables should be applied before SDIF programming begins. E.g. setting sdif_disable = 8'b1000_1011 will disable module instances 0, 1, 3 & 7. Volatile: No

Bits	Field Name	Access	Description
			Value After Reset: 0x0

15.5.3.189 VM_CMN_SDIF_STATUS

- Description: VM SDIF status register
- Offset: 0x0808
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SDIF_LOCK	RO	SDIF Locked (active high). Set when slave auto mode is requested to indicate the SDIF is now a write only interface. Volatile: Yes Value After Reset: 0x0
[0]	SDIF_BUSY	RO	SDIF busy (active high). When asserted indicates the SDIF is busy so any SDIF programming requests will be ignored. Or the clock synthesiser/disable SDIF state is being updated. Volatile: Yes Value After Reset: 0x0

15.5.3.190 VM_CMN_SDIF

- Description: VM SDIF write data register
- Offset: 0x080c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	SDIF_PROG	WO	Serial I/F program request (active high). This self-clearing bit will be ignored if the sdif_busy flag is set or if the sdif_lock flag is set and the request is a read request (sdif_wrn = 0). Volatile: No Value After Reset: 0x0
[30:28]	RESERVED_1	-	
[27]	SDIF_WRN	RW	Serial I/F Write NOT Read control bit 1: Write 0: Read

Bits	Field Name	Access	Description
			Volatile: No Value After Reset: 0x0
[26:24]	SDIF_ADDR	RW	Serial I/F register address, SDIF_ADDR[1:0] Volatile: No Value After Reset: 0x0
[23:0]	SDIF_WDATA	RW	Serial I/F write data, SDIF_DATA[23:0] Volatile: No Value After Reset: 0x0

15.5.3.191 VM_CMN_SDIF_HALT

- Description: VM SDIF halt register. Halts all SDIF data transfer and resets SDIF slave.
- Offset: 0x0810
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_STOP	WO	Serial I/F write data. SDIF stop (active high) This self-clearing bit immediately stops all SDIF programming activity. The feature provides a means to terminate serial data interface activity in the unlikely event of it becoming locked, it should not be required during normal operation. Volatile: No Value After Reset: 0x0

15.5.3.192 VM_CMN_SDIF_CTRL

- Description: VM SDIF programming inhibit (active high). When asserted inhibits serial programming of the selected VM instance(s).
- Offset: 0x0814
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SDIF_INHIBIT	RW	SDIF programming inhibit (active high). When asserted inhibits serial programming of the selected module instance(s). Inhibits should be applied before SDIF programming begins. e.g. setting sdif_inhibit = 8'b1000_1011 will disable programing of module

Bits	Field Name	Access	Description
			instances 0, 1, 3 & 7. Volatile: No Value After Reset: 0x0

15.5.3.193 VM_CMN_SMPL_CTRL

- Description: VM SDIF sample counter control
- Offset: 0x0820
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	SMPL_DISCARD	RW	Sample discard (active high). This feature can be used to temporarily discard received data samples. When this bit is set data recovery is disabled but the external module may continue to run. Volatile: No Value After Reset: 0x0
[1]	SMPL_CTR_HOLD	RW	Sample counter hold (active high). When asserted the sample counter is prevented from rolling over when the maximum sample count is reached. Volatile: No Value After Reset: 0x0
[0]	SMPL_CTR_DISABLE	RW	Sample counter disable (active high) 0x0: Sample counter enabled. 0x1: Sample counter disabled. Volatile: No Value After Reset: 0x0

15.5.3.194 VM_CMN_SMPL_CLR

- Description: VM SDIF sample counter clear
- Offset: 0x0824
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SMPL_CTR_DISABLE	WO	Sample counter clear (active high write). The sample counter value is set to zero when this self-clearing bit

Bits	Field Name	Access	Description
			is written with 1. Volatile: No Value After Reset: 0x0

15.5.3.195 VM_CMN_SMPL_CNT

- Description: VM SDIF sample counter current value
- Offset: 0x0828
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	SMPL_COUNT	RO	Sample counter. The 16-bit counter increments each time a new data sample is made available. The counter is cleared by writing '1' to 'smpl_ctr_clr'. The sample counter over-flow operation is determined by 'smpl_ctr_hold'. Volatile: Yes Value After Reset: 0x0

15.5.3.196 VM_00_IRQ_ENABLE

- Description: VM-00 IRQ enable register, enables individual IRQ sources from the VM.
- Offset: 0x0a00
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	IRQ_EN_DONE	RW	Sample done IRQ enable Volatile: No Value After Reset: 0x0
[0]	IRQ_EN_FAULT	RW	Fault IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.197 VM_00_IRQ_STATUS

- Description: VM-00 IRQ status register, reports status of individual IRQ sources from the VM.
- Offset: 0x0a04
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	IRQ_STATUS_DONE	RO	Sample done IRQ status Volatile: Yes Value After Reset: 0x0
[0]	IRQ_STATUS_FAULT	RO	Fault IRQ status Volatile: Yes Value After Reset: 0x0

15.5.3.198 VM_00_IRQ_CLEAR

- Description: VM-00 IRQ clear register, clears individual IRQ sources from the VM.
- Offset: 0x0a08
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	WO	Sample done IRQ clear Volatile: Yes Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	WO	Fault IRQ clear Volatile: Yes Value After Reset: 0x0

15.5.3.199 VM_00_IRQ_TEST

- Description: VM-00 IRQ test register. Write to register will trigger a VM IRQ if the IRQ enabled.
- Offset: 0x0a0c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	IRQ_CLR_DONE	RW	Sample done IRQ test Volatile: No Value After Reset: 0x0
[0]	IRQ_CLR_FAULT	RW	Fault IRQ test Volatile: No Value After Reset: 0x0

15.5.3.200 VM_00_IRQ_ALARMA_ENABLE

- Description: VM-00 Alarm-A IRQ enable register, enables individual IRQ sources from the VM.
- Offset: 0x0a10
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	IRQ_EN_ALARMA	RW	Channel Alarm A IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.201 VM_00_IRQ_ALARMA_STATUS

- Description: VM-00 Alarm-A IRQ status register, reports status of individual IRQ sources from the VM.
- Offset: 0x0a14
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	IRQ_STATUS_ALARMA	RO	Channel Alarm A IRQ Status Volatile: Yes Value After Reset: 0x0

15.5.3.202 VM_00_IRQ_ALARMA_CLR

- Description: VM-00 Alarm-A IRQ clear register, clears individual IRQ sources from the VM.
- Offset: 0x0a18
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	IRQ_CLR_ALARMA	WO	Channel Alarm A IRQ clear Volatile: No Value After Reset: 0x0

15.5.3.203 VM_00_IRQ_ALARMA_TEST

- Description: VM-00 Alarm-A IRQ test register. Write to register will trigger a VM IRQ if the IRQ enabled.

- Offset: 0x0a1c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	IRQ_TEST_ALARMA	RW	Channel Alarm A IRQ test Volatile: No Value After Reset: 0x0

15.5.3.204 VM_00_IRQ_ALARMB_ENABLE

- Description: VM-00 Alarm-B IRQ enable register, enables individual IRQ sources from the VM.
- Offset: 0x0a20
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	IRQ_EN_ALARMB	RW	Channel Alarm B IRQ enable Volatile: No Value After Reset: 0x0

15.5.3.205 VM_00_IRQ_ALARMB_STATUS

- Description: VM-00 Alarm-B IRQ status register, reports status of individual IRQ sources from the VM.
- Offset: 0x0a24
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	IRQ_STATUS_ALARMB	RO	Channel Alarm B IRQ status Volatile: Yes Value After Reset: 0x0

15.5.3.206 VM_00_IRQ_ALARMB_CLR

- Description: VM-00 Alarm-B IRQ clear register, clears individual IRQ sources from the VM.
- Offset: 0x0a28
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	IRQ_CLR_ALARMB	WO	Channel Alarm B IRQ clear Volatile: No Value After Reset: 0x0

15.5.3.207 VM_00_IRQ_ALARMB_TEST

- Description: VM-00 Alarm-B IRQ test register. Write to register will trigger a VM IRQ if the IRQ enabled.
- Offset: 0x0a2c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	IRQ_TEST_ALARMB	RW	Channel Alarm B IRQ test Volatile: No Value After Reset: 0x0

15.5.3.208 VM_00_SDIF_RDATA

- Description: VM read data register
- Offset: 0x0a30
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	SDIF_RDATA	RO	SDIF read data Volatile: Yes Value After Reset: 0x0

15.5.3.209 VM_00_SDIF_DONE

- Description: VM SDIF sample done register. Indicates sample data is available, cleared by of SDIF sample data register.
- Offset: 0x0a34
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	

Bits	Field Name	Access	Description
[0]	SDIF_SMPL_DONE	RO	Sample done flag (active high). The sample done flag is asserted when a new data sample is made available. The sample done flag is automatically cleared when the associated 'data' register is read. Volatile: Yes Value After Reset: 0x0

15.5.3.210 VM_00_CH_00_SDIF_DATA

- Description: VM-00 SDIF channel 00 sample data register
- Offset: 0x0a40
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.211 VM_00_CH_01_SDIF_DATA

- Description: VM-00 SDIF channel 01 sample data register
- Offset: 0x0a44
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.212 VM_00_CH_02_SDIF_DATA

- Description: VM-00 SDIF channel 02 sample data register
- Offset: 0x0a48
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0

Bits	Field Name	Access	Description
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.213 VM_00_CH_03_SDIF_DATA

- Description: VM-00 SDIF channel 03 sample data register
- Offset: 0x0a4c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.214 VM_00_CH_04_SDIF_DATA

- Description: VM-00 SDIF channel 04 sample data register
- Offset: 0x0a50
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	

Bits	Field Name	Access	Description
[17]	FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.215 VM_00_CH_05_SDIF_DATA

- Description: VM-00 SDIF channel 05 sample data register
- Offset: 0x0a54
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of

Bits	Field Name	Access	Description
			the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.216 VM_00_CH_06_SDIF_DATA

- Description: VM-00 SDIF channel 06 sample data register
- Offset: 0x0a58
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.217 VM_00_CH_07_SDIF_DATA

- Description: VM-00 SDIF channel 07 sample data register
- Offset: 0x0a5c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	FAULT	RO	Sample fault. When set indicates that the module has

Bits	Field Name	Access	Description
			signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.218 VM_00_CH_08_SDIF_DATA

- Description: VM-00 SDIF channel 08 sample data register
- Offset: 0x0a60
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE

Bits	Field Name	Access	Description
			register. Volatile: Yes Value After Reset: 0x0

15.5.3.219 VM_00_CH_09_SDIF_DATA

- Description: VM-00 SDIF channel 09 sample data register
- Offset: 0x0a64
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.220 VM_00_CH_10_SDIF_DATA

- Description: VM-00 SDIF channel 10 sample data register
- Offset: 0x0a68
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded.

Bits	Field Name	Access	Description
			Volatile: Yes Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.221 VM_00_CH_11_SDIF_DATA

- Description: VM-00 SDIF channel 11 sample data register
- Offset: 0x0a6c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE register.

Bits	Field Name	Access	Description
			Volatile: Yes Value After Reset: 0x0

15.5.3.222 VM_00_CH_12_SDIF_DATA

- Description: VM-00 SDIF channel 12 sample data register
- Offset: 0x0a70
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.223 VM_00_CH_13_SDIF_DATA

- Description: VM-00 SDIF channel 13 sample data register
- Offset: 0x0a74
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.224 VM_00_CH_14_SDIF_DATA

- Description: VM-00 SDIF channel 14 sample data register
- Offset: 0x0a78
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE register. Volatile: Yes

Bits	Field Name	Access	Description
			Value After Reset: 0x0

15.5.3.225 VM_00_CH_15_SDIF_DATA

- Description: VM-00 SDIF channel 15 sample data register
- Offset: 0x0a7c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_1	-	
[17]	FAULT	RO	Sample fault. When set indicates that the module has signalled a fault, the sample data should be discarded. Volatile: Yes Value After Reset: 0x0
[16]	TYPE	RO	Module sample type 0x0: Indicates valid data. 0x1: Indicates either analogue access, signature select or fault debug mode. The ip_type flag is updated when new data is received. Volatile: Yes Value After Reset: 0x0
[15:0]	SAMPLE_DATA	RO	Sample data. Reading this register clears the state of the SDIF_SMPL_DONE flag in the VM_[n]_SDIF_DONE register. Volatile: Yes Value After Reset: 0x0

15.5.3.226 VM_00_CH_00_ALARMA_CFG

- Description: VM-00 channel 00 Alarm A configuration
- Offset: 0x0a80
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full

Bits	Field Name	Access	Description
			details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.227 VM_00_CH_00_ALARMB_CFG

- Description: VM-00 channel 00 Alarm B configuration
- Offset: 0x0a84
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.228 VM_00_CH_00_SMPL_HILO

- Description: VM-00 channel 00 sample max/min high/low value
- Offset: 0x0a88
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.229 VM_00_CH_00_HILO_RESET

- Description: VM-00 channel 00 reset sample high/low register
- Offset: 0x0a8c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

15.5.3.230 VM_00_CH_01_ALARMA_CFG

- Description: VM-00 channel 01 Alarm A configuration
- Offset: 0x0a90
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.231 VM_00_CH_01_ALARMB_CFG

- Description: VM-00 channel 01 Alarm B configuration
- Offset: 0x0a94
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full

Bits	Field Name	Access	Description
			details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.232 VM_00_CH_01_SMPL_HILO

- Description: VM-00 channel 01 sample max/min high/low value
- Offset: 0x0a98
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.233 VM_00_CH_01_HILO_RESET

- Description: VM-00 channel 01 reset sample high/low register
- Offset: 0x0a9c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

15.5.3.234 VM_00_CH_02_ALARMA_CFG

- Description: VM-00 channel 02 Alarm A configuration

- Offset: 0x0aa0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.235 VM_00_CH_02_ALARMB_CFG

- Description: VM-00 channel 02 Alarm B configuration
- Offset: 0x0aa4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.236 VM_00_CH_02_SMPL_HILO

- Description: VM-00 channel 02 sample max/min high/low value
- Offset: 0x0aa8
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received

Bits	Field Name	Access	Description
			Volatile: Yes Value After Reset: 0xFFFF

15.5.3.237 VM_00_CH_02_HILO_RESET

- Description: VM-00 channel 02 reset sample high/low register
- Offset: 0x0aac
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

15.5.3.238 VM_00_CH_03_ALARMA_CFG

- Description: VM-00 channel 03 Alarm A configuration
- Offset: 0x0ab0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.239 VM_00_CH_03_ALARMB_CFG

- Description: VM-00 channel 03 Alarm B configuration

- Offset: 0x0ab4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.240 VM_00_CH_03_SMPL_HILO

- Description: VM-00 channel 03 sample max/min high/low value
- Offset: 0x0ab8
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.241 VM_00_CH_03_HILO_RESET

- Description: VM-00 channel 03 reset sample high/low register
- Offset: 0x0abc
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0

Bits	Field Name	Access	Description
[0	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

15.5.3.242 VM_00_CH_04_ALARMA_CFG

- Description: VM-00 channel 04 Alarm A configuration
- Offset: 0x0ac0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.243 VM_00_CH_04_ALARMB_CFG

- Description: VM-00 channel 04 Alarm B configuration
- Offset: 0x0ac4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.244 VM_00_CH_04_SMPL_HILO

- Description: VM-00 channel 04 sample max/min high/low value

- Offset: 0x0ac8
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.245 VM_00_CH_04_HILO_RESET

- Description: VM-00 channel 04 reset sample high/low register
- Offset: 0x0acc
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

15.5.3.246 VM_00_CH_05_ALARMA_CFG

- Description: VM-00 channel 05 Alarm A configuration
- Offset: 0x0ad0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

Bits	Field Name	Access	Description
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.247 VM_00_CH_05_ALARMB_CFG

- Description: VM-00 channel 05 Alarm B configuration
- Offset: 0x0ad4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.248 VM_00_CH_05_SMPL_HILO

- Description: VM-00 channel 05 Sample max/min high/low value.
- Offset: 0x0ad8
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.249 VM_00_CH_05_HILO_RESET

- Description: VM-00 channel 05 reset sample high/low register
- Offset: 0x0adc
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

15.5.3.250 VM_00_CH_06_ALARMA_CFG

- Description: VM-00 channel 06 Alarm A configuration
- Offset: 0x0ae0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.251 VM_00_CH_06_ALARMB_CFG

- Description: VM-00 channel 06 Alarm B configuration
- Offset: 0x0ae4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full

Bits	Field Name	Access	Description
			details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.252 VM_00_CH_06_SMPL_HILO

- Description: VM-00 channel 06 sample max/min high/low value
- Offset: 0x0ae8
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.253 VM_00_CH_06_HILO_RESET

- Description: VM-00 channel 06 reset sample high/low register
- Offset: 0x0aec
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

15.5.3.254 VM_00_CH_07_ALARMA_CFG

- Description: VM-00 channel 07 Alarm A configuration

- Offset: 0x0af0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.255 VM_00_CH_07_ALARMB_CFG

- Description: VM-00 channel 07 Alarm B configuration
- Offset: 0x0af4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.256 VM_00_CH_07_SMPL_HILO

- Description: VM-00 channel 07 sample max/min high/low value
- Offset: 0x0af8
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received

Bits	Field Name	Access	Description
			Volatile: Yes Value After Reset: 0xFFFF

15.5.3.257 VM_00_CH_07_HILO_RESET

- Description: VM-00 channel 07 reset sample high/low register
- Offset: 0x0afc
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

15.5.3.258 VM_00_CH_08_ALARMA_CFG

- Description: VM-00 channel 08 Alarm A configuration
- Offset: 0x0b00
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.259 VM_00_CH_08_ALARMB_CFG

- Description: VM-00 channel 08 Alarm B configuration

- Offset: 0x0b04
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.260 VM_00_CH_08_SMPL_HILO

- Description: VM-00 channel 08 sample max/min high/low value
- Offset: 0x0b08
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.261 VM_00_CH_08_HILO_RESET

- Description: VM-00 channel 08 reset sample high/low register
- Offset: 0x0b0c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0

Bits	Field Name	Access	Description
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

15.5.3.262 VM_00_CH_09_ALARMA_CFG

- Description: VM-00 channel 09 Alarm A configuration
- Offset: 0x0b10
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.263 VM_00_CH_09_ALARMB_CFG

- Description: VM-00 channel 09 Alarm B configuration
- Offset: 0x0b14
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.264 VM_00_CH_09_SMPL_HILO

- Description: VM-00 channel 09 sample max/min high/low value

- Offset: 0x0b18
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.265 VM_00_CH_09_HILO_RESET

- Description: VM-00 channel 09 reset sample high/low register
- Offset: 0x0b1c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

15.5.3.266 VM_00_CH_10_ALARMA_CFG

- Description: VM-00 channel 10 Alarm A configuration
- Offset: 0x0b20
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

Bits	Field Name	Access	Description
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.267 VM_00_CH_10_ALARMB_CFG

- Description: VM-00 channel 10 Alarm B configuration
- Offset: 0x0b24
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.268 VM_00_CH_10_SMPL_HILO

- Description: VM-00 channel 10 sample max/min high/low value
- Offset: 0x0b28
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.269 VM_00_CH_10_HILO_RESET

- Description: VM-00 channel 10 reset sample high/low register
- Offset: 0x0b2c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

15.5.3.270 VM_00_CH_11_ALARMA_CFG

- Description: VM-00 channel 11 Alarm A configuration
- Offset: 0x0b30
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.271 VM_00_CH_11_ALARMB_CFG

- Description: VM-00 channel 11 Alarm B configuration
- Offset: 0x0b34
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full

Bits	Field Name	Access	Description
			details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.272 VM_00_CH_11_SMPL_HILO

- Description: VM-00 channel 11 sample max/min high/low value
- Offset: 0x0b38
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.273 VM_00_CH_11_HILO_RESET

- Description: VM-00 channel 11 reset sample high/low register
- Offset: 0x0b3c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

15.5.3.274 VM_00_CH_12_ALARMA_CFG

- Description: VM-00 channel 12 Alarm A configuration

- Offset: 0x0b40
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.275 VM_00_CH_12_ALARMB_CFG

- Description: VM-00 channel 12 Alarm B configuration
- Offset: 0x0b44
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.276 VM_00_CH_12_SMPL_HILO

- Description: VM-00 channel 12 sample max/min high/low value
- Offset: 0x0b48
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received

Bits	Field Name	Access	Description
			Volatile: Yes Value After Reset: 0xFFFF

15.5.3.277 VM_00_CH_12_HILO_RESET

- Description: VM-00 channel 12 reset sample high/low register
- Offset: 0x0b4c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

15.5.3.278 VM_00_CH_13_ALARMA_CFG

- Description: VM-00 channel 13 Alarm A configuration
- Offset: 0x0b50
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.279 VM_00_CH_13_ALARMB_CFG

- Description: VM-00 channel 13 Alarm B configuration

- Offset: 0x0b54
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.280 VM_00_CH_13_SMPL_HILO

- Description: VM-00 channel 13 sample max/min high/low value
- Offset: 0x0b58
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.281 VM_00_CH_13_HILO_RESET

- Description: VM-00 channel 13 reset sample high/low register
- Offset: 0x0b5c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0

Bits	Field Name	Access	Description
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

15.5.3.282 VM_00_CH_14_ALARMA_CFG

- Description: VM-00 channel 14 Alarm A configuration
- Offset: 0x0b60
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.283 VM_00_CH_14_ALARMB_CFG

- Description: VM-00 channel 14 Alarm B configuration
- Offset: 0x0b64
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.284 VM_00_CH_14_SMPL_HILO

- Description: VM-00 channel 14 sample max/min high/low value

- Offset: 0x0b68
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.285 VM_00_CH_14_HILO_RESET

- Description: VM-00 channel 14 reset sample high/low register
- Offset: 0x0b6c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

15.5.3.286 VM_00_CH_15_ALARMA_CFG

- Description: VM-00 channel 15 Alarm A configuration
- Offset: 0x0b70
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

Bits	Field Name	Access	Description
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.287 VM_00_CH_15_ALARMB_CFG

- Description: VM-00 channel 15 Alarm B configuration
- Offset: 0x0b74
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	ALARM_THRESH	RW	Alarm threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0
[15:0]	HYST_THRESH	RW	Alarm hysteresis threshold. Refer to section 14 for full details of the alarm configuration. Volatile: No Value After Reset: 0x0

15.5.3.288 VM_00_CH_15_SMPL_HILO

- Description: VM-00 channel 15 sample max/min high/low value
- Offset: 0x0b78
- Default Value: 0xffff

Bits	Field Name	Access	Description
[31:16]	SMPL_HI	RO	Highest valid data sample value received Volatile: Yes Value After Reset: 0x0
[15:0]	SMPL_LO	RO	Lowest valid data sample value received Volatile: Yes Value After Reset: 0xFFFF

15.5.3.289 VM_00_CH_15_HILO_RESET

- Description: VM-00 channel 15 reset sample high/low register
- Offset: 0x0b7c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	SMPL_HI_CLR	WO	Sample high clear 0 (active high write). The stored sample high value is initialized to all zeros when written. Volatile: Yes Value After Reset: 0x0
[0]	SMPL_LO_SET	WO	Sample low set (active high write). The stored sample low value is initialized to all ones when written. Volatile: Yes Value After Reset: 0x0

16 System Configuration

16.1 Overview

The system configuration module mainly manages bus configuration, system startup and control between subsystems in the chip. It only contains registers that are divided into the TEE region and the REE region. Each control register corresponds to a TEE address and a REE address. In addition, some registers in the TEE region can control access authority of the registers in the REE region. The system configuration module also includes the SOC_ID register, which describes the SoC chip version.

16.2 Main Features

- Top and subsystem bus configuration, including bus master and salve ports arbitration priority and QoS configuration
- General purpose register for software use
- Boot media select register
- Software interrupt source register
- C910 CPU startup address configuration register
- SoC chip version register

16.3 Register Description

16.3.1 TEE and REE Address Space Description

Each register in the system configuration module corresponds to two addresses, one is the REE space address, and the other is the TEE space address. In addition, there are some registers in the TEE address space that can control access authority of the REE address segment. The address space distribution is described as follows:

	C910 Access Space		E902 Access Space	
	REE Start Address	**TEE Start Address**	**REE Start Address**	**TEE Start Address**
System control registers	0xFFEF018000	0xFFFF018000	0xBF018000	0xFF018000
AON_SUBSYS registers	Not accessible	0xFFFFF48000	Not accessible	0xFFF48000
DDR_SUBSYS control registers	Not accessible	0xFFFF004000	Not accessible	0xFF004000
DSP_SUBSYS control registers	0xFFEF040000	0xFFFF040000	0xBF040000	0xFF040000

	C910 Access Space		E902 Access Space	
	REE Start Address	TEE Start Address	REE Start Address	TEE Start Address
PERI_SUBSYS control registers	0xFFEC02C000	0xFFFC02C000	0xBC02C000	0xFC02C000
VI_SUBSYS control registers	0xFFE4040000	0xFFF4040000	0xB4040000	0xF4040000
VO_SUBYS control registers	0xFFEF528000	0xFFFF528000	0xBF528000	0xFF528000
VP_SUBSYS control registers	0xFFECC30000	0xFFFCC30000	0xBCC30000	0xFCC30000

16.3.2 Register Memory Map

16.3.2.1 System Control Registers

Register	Offset	Description	Section/Page
BOOT_REG0	0x0	General purpose register for bootloader	16.3.3.1.1/1037
BOOT_REG1	0x4	General purpose register for bootloader	16.3.3.1.2/1037
BOOT_REG2	0x8	General purpose register for bootloader	16.3.3.1.3/1037
BOOT_REG3	0xC	General purpose register for bootloader	16.3.3.1.4/1037
BOOT_SEL	0x10	Boot media selection	16.3.3.1.5/1038
C910_CTRL0	0x14	C910 CPU system control	16.3.3.1.6/1038
SOC_VER	0x20	SoC chip version register	16.3.3.1.7/1038
SW_REG0	0x40	General purpose register for software use	16.3.3.1.8/1039
SW_REG1	0x44	General purpose register for software use	16.3.3.1.9/1039
SW_REG2	0x48	General purpose register for software use	16.3.3.1.10/1039
SW_REG3	0x4C	General purpose register for software use	16.3.3.1.11/1040
C910_CORE0_RVBA_L	0x50	C910 core0 reset entry address lower bits	16.3.3.1.12/1040
C910_CORE0_RVBA_H	0x54	C910 core0 reset entry address upper bits	16.3.3.1.13/1040
C910_CORE1_RVBA_L	0x58	C910 core1 reset entry address lower bits	16.3.3.1.14/1040
C910_CORE1_RVBA_H	0x5C	C910 core1 reset entry address upper bits	16.3.3.1.15/1041
C910_CORE2_RVBA_L	0x60	C910 core2 reset entry address lower bits	16.3.3.1.16/1041
C910_CORE2_RVBA_H	0x64	C910 core2 reset entry address upper bits	16.3.3.1.17/1041
C910_CORE3_RVBA_L	0x68	C910 core3 reset entry address lower bits	16.3.3.1.18/1041

Register	Offset	Description	Section/Page
C910_CORE3_RVBA_H	0x6C	C910 core3 reset entry address upper bits	16.3.3.1.19/1042
C910_TIMER_LINK	0x74	Timer in CPU_SUBSYS configuration register	16.3.3.1.20/1042
C910_REE_INT_SRC_0	0x78	C910 REE core software interrupt source 0	16.3.3.1.21/1042
C910_REE_INT_SRC_1	0x7C	C910 REE core software interrupt source 1	16.3.3.1.22/1043
C910_REE_INT_SRC_2	0x80	C910 REE core software interrupt source 2	16.3.3.1.23/1043
C910_REE_INT_SRC_3	0x84	C910 REE core software interrupt source 3	16.3.3.1.24/1043
C910_REE_INT_SRC_4	0x88	C910 REE core software interrupt source 4	16.3.3.1.25/1044
C910_REE_INT_SRC_5	0x8C	C910 REE core software interrupt source 5	16.3.3.1.26/1044
C910_REE_INT_SRC_6	0x90	C910 REE core software interrupt source 6	16.3.3.1.27/1044
C910_REE_INT_SRC_7	0x94	C910 REE core software interrupt source 7	16.3.3.1.28/1045
CPUSYS1_AXI_CFG	0xC0	AXI_CPUSYS1 AXI master and slave ports arbitration priority configuration	16.3.3.1.29/1045
CPUSYS2_AXI_CFG	0xC4	AXI_CPUSYS2 AXI master and slave ports arbitration priority configuration	16.3.3.1.30/1046
CPUSYS_QOS_CFG	0xC8	Master Quality of Service (QoS) identifier register of AXI bus in CPU_SUBSYS	16.3.3.1.31/1047
PERISYS_SEL_ADDR_L	0xD0	GMAC AXI bus address configuration register	16.3.3.1.32/1048
NPUSYS_AXI_CFG	0xD4	NPU2MEM AXI master and slave ports arbitration priority configuration	16.3.3.1.33/1048
AXI4_CFG_BUS_CFG_M	0xD8	CFG AXI master ports arbitration priority configuration	16.3.3.1.34/1049
AXI4_CFG_BUS_CFG_S	0xDC	CFG AXI slave ports arbitration priority configuration	16.3.3.1.35/1049
AP_BUS_CFG	0xE0	Master QoS identifier register of AXI bus in CPU_SUBSYS	16.3.3.1.36/1050
VOBUS_AXI_CFG	0xE4	CFG AXI master and slave ports arbitration priority configuration	16.3.3.1.37/1051
QSPI_XIP_CTRL	0x134	SPI eXecute-In-Place (XIP) support control register	16.3.3.1.38/1051
AP_I2S_CTRL	0x138	I2S configuration and status register	16.3.3.1.39/1052
NNA_INT_MASK	0x13c	NNA interrupt mask register	16.3.3.1.40/1052

Register	Offset	Description	Section/Page
BOOT_REG0_TEE	0x1000	General purpose register for bootloader	16.3.3.1.41/1052
BOOT_REG1_TEE	0x1004	General purpose register for bootloader	16.3.3.1.42/1053
BOOT_REG2_TEE	0x1008	General purpose register for bootloader	16.3.3.1.43/1053
BOOT_REG3_TEE	0x100C	General purpose register for bootloader	16.3.3.1.44/1053
BOOT_SEL_TEE	0x1010	Boot media selection	16.3.3.1.45/1053
C910_CTRL0_TEE	0x1014	C910 CPU system control	16.3.3.1.46/1054
SOC_VER_TEE	0x1020	SoC chip version register	16.3.3.1.47/1054
SW_REG0_TEE	0x1040	General purpose register for software use	16.3.3.1.48/1055
SW_REG1_TEE	0x1044	General purpose register for software use	16.3.3.1.49/1055
SW_REG2_TEE	0x1048	General purpose register for software use	16.3.3.1.50/1055
SW_REG3_TEE	0x104C	General purpose register for software use	16.3.3.1.51/1056
C910_CORE0_RVBA_L_TEE	0x1050	C910 core0 reset entry address lower bits	16.3.3.1.52/1056
C910_CORE0_RVBA_H_TEE	0x1054	C910 core0 reset entry address upper bits	16.3.3.1.53/1056
C910_CORE1_RVBA_L_TEE	0x1058	C910 core1 reset entry address lower bits	16.3.3.1.54/1056
C910_CORE1_RVBA_H_TEE	0x105C	C910 core1 reset entry address upper bits	16.3.3.1.55/1056
C910_CORE2_RVBA_L_TEE	0x1060	C910 core2 reset entry address lower bits	16.3.3.1.56/1057
C910_CORE2_RVBA_H_TEE	0x1064	C910 core2 reset entry address upper bits	16.3.3.1.57/1057
C910_CORE3_RVBA_L_TEE	0x1068	C910 core3 reset entry address lower bits	16.3.3.1.58/1057
C910_CORE3_RVBA_H_TEE	0x106C	C910 core3 reset entry address upper bits	16.3.3.1.59/1057
C910_TIMER_LINK_TEE	0x1074	TIMER in CPU_SUBSYS configuration register	16.3.3.1.60/1058
C910_REE_INT_SRC_0_TEE	0x1078	C910 TEE core software interrupt source 0	16.3.3.1.61/1058
C910_REE_INT_SRC_1_TEE	0x107C	C910 TEE core software interrupt source 1	16.3.3.1.62/1059
C910_REE_INT_SRC_2_TEE	0x1080	C910 TEE core software interrupt source 2	16.3.3.1.63/1059
C910_REE_INT_SRC_3_TEE	0x1084	C910 TEE core software interrupt source 3	16.3.3.1.64/1059
C910_REE_INT_SRC_4_TEE	0x1088	C910 TEE core software interrupt source 4	16.3.3.1.65/1060
C910_REE_INT_SRC_5_TEE	0x108C	C910 TEE core software interrupt source 5	16.3.3.1.66/1060
C910_REE_INT_SRC_6_TEE	0x1090	C910 TEE core software interrupt source 6	16.3.3.1.67/1060
C910_REE_INT_SRC_7_TEE	0x1094	C910 TEE core software interrupt source 7	16.3.3.1.68/1060

Register	Offset	Description	Section/Page
CPUSYS1_AXI_CFG_TEE	0x10C0	AXI_CPUSYS1 AXI master and slave ports arbitration priority configuration	16.3.3.1.69/1061
CPUSYS2_AXI_CFG_TEE	0x10C4	AXI_CPUSYS2 AXI master and slave ports arbitration priority configuration	16.3.3.1.70/1062
CPUSYS_QOS_CFG_TEE	0x10C8	Master QoS identifier register of AXI bus in CPU_SUBSYS	16.3.3.1.71/1063
PERISYS_SEL_ADDR_L_TEE	0x10D0	GMAC AXI bus address configuration register	16.3.3.1.72/1064
NPUSYS_AXI_CFG_TEE	0x10D4	NPU2MEM AXI master and slave ports arbitration priority configuration	16.3.3.1.73/1064
AXI4_CFG_BUS_CFG_M_TEE	0x10D8	CFG AXI master ports arbitration priority configuration	16.3.3.1.74/1065
AXI4_CFG_BUS_CFG_S_TEE	0x10DC	CFG AXI slave ports arbitration priority configuration	16.3.3.1.75/1065
AP_BUS_CFG_TEE	0x10E0	Master QoS identifier register of AXI bus in CPU_SUBSYS	16.3.3.1.76/1066
VOBUS_AXI_CFG_TEE	0x10E4	CFG AXI master and slave ports arbitration priority configuration	16.3.3.1.77/1066
QSPI_XIP_CTRL_TEE	0x1134	SPI XIP support control register	16.3.3.1.78/1067
AP_I2S_CTRL_TEE	0x1138	I2S configuration and status register	16.3.3.1.79/1067
NNA_INT_MASK_TEE	0x113C	NNA interrupt mask register	16.3.3.1.80/1068
SYSREG_LOCK_0	0x1800	REE region registers' lock control register	16.3.3.1.81/1068

16.3.2.2 AON_SUBSYS Control Registers

Register	Offset	Description	Section/Page
CPU_LP_MODE	0x00	CPU low power mode register	16.3.3.2.1/1070
CHIP_LP_MODE	0x04	SoC low power mode register	16.3.3.2.2/1071
AO_SERAM_TRN	0x10	AO_SERAM scrambler register	16.3.3.2.3/1071
AO_SERAM_INT	0x14	AO_SRAM interrupt register	16.3.3.2.4/1072
STR_SERAM_TRN	0x18	STR_SERAM scrambler register	16.3.3.2.5/1072
STR_SERAM_INT	0x1c	STR_SRAM interrupt register	16.3.3.2.6/1072
STR_INDICATOR_0	0x20	Low power startup marker register 0	16.3.3.2.7/1072

Register	Offset	Description	Section/Page
STR_INDICATOR_1	0x24	Low power startup marker register 1	16.3.3.2.8/1073
STR_INDICATOR_2	0x28	Low power startup marker register 2	16.3.3.2.9/1073
STR_INDICATOR_3	0x2c	Low power startup marker register 3	16.3.3.2.10/1073
PVTC_WR_LOCK	0x30	Pvtc write lock	16.3.3.2.11/1073
PVTC_TS_ALARM	0x34	Temperature sensor alarm register	16.3.3.2.12/1074
PVTC_VM_ALARM	0x38	Voltage monitor alarm register	16.3.3.2.13/1074
PVTC_PD_ALARM	0x3c	Process detector alarm register	16.3.3.2.14/1074
E902_CNT_CLR	0x40	E902 timer counter clear register	16.3.3.2.15/1075
E902_RST_ADDR	0x44	E902 reset start address register	16.3.3.2.16/1075
C906_RST_ADDR_L	0x48	C906 reset start address register, lower 32 bits	16.3.3.2.17/1075
C906_RST_ADDR_H	0x4c	C906 reset start address register, upper 32 bits	16.3.3.2.18/1075
RESERVED_REG_0	0x50	General purpose register	16.3.3.2.19/1076
RESERVED_REG_1	0x54	General purpose register	16.3.3.2.20/1076
RESERVED_REG_2	0x58	General purpose register	16.3.3.2.21/1076
RESERVED_REG_3	0x5c	General purpose register	16.3.3.2.22/1076
AON_AHB_ADEXT	0x60	AON_SUBSYS AHB bus address extension register	16.3.3.2.23/1077
RC_EN	0x70	RC enable control register	16.3.3.2.24/1077
RC_FCAL	0x74	RC trim register	16.3.3.2.25/1077
RC_MODE	0x78	RC mode control register	16.3.3.2.26/1078
RC_READY	0x7c	RC status register	16.3.3.2.27/1078
ISO_CFG	0x80	Isolation cells control register for low power mode	16.3.3.2.28/1078
OCRAM_ERR	0x90	OCRAM check error register	16.3.3.2.29/1079
TIMER_LINK	0x100	Timer link register	16.3.3.2.30/1079
PD_REQ	0x110	Power domain power on/off control register	16.3.3.2.31/1080
PD_ISO_EN_SET	0x114	Power domain isolation cells enable control register	16.3.3.2.32/1081

Register	Offset	Description	Section/Page
PD_ISO_EN_CLR	0x118	Power domain isolation cells disable control register	16.3.3.2.33/1081
PD_SW_EN_SET	0x11c	Power domain power switch cells off control register. Used for low power control in software mode.	16.3.3.2.34/1082
PD_SW_EN_CLR	0x120	Power domain power switch cells on control register. Used for low power control in software mode.	16.3.3.2.35/1083
PD_SW_ACK	0x124	Power domain power switch cells acknowledgement register	16.3.3.2.36/1083
PD_SW_CNT_EN	0x128	Power domain power on/off feedback wait time control register, used in low power control hardware mode.	16.3.3.2.37/1084
PD_FSM_RST	0x12c	Reset control register for all PMUs in every power domain	16.3.3.2.38/1085
PD_INT_MASK	0x130	PMU interrupt mask control register	16.3.3.2.39/1085
PD_FSM_STS_L	0x134	PMU FSM status register of every power domain	16.3.3.2.40/1086
PD_FSM_STS_H	0x138	PMU FSM status register of every power domain	16.3.3.2.41/1086
PD_INT_STS	0x13c	PMU interrupt status register	16.3.3.2.42/1087
PD_INT_CLR	0x140	PMU interrupt clear register	16.3.3.2.43/1087
PD_BLK0_SW_CNT	0x144	AUDIO_SUBSYS power domain power on/off feedback wait time counter register	16.3.3.2.44/1088
PD_BLK1_SW_CNT	0x148	VDEC power domain power on/off feedback wait time counter register	16.3.3.2.45/1088
PD_BLK2_SW_CNT	0x14c	NPU power domain power on/off feedback wait time counter register	16.3.3.2.46/1089
PD_BLK3_SW_CNT	0x150	VENC power domain power on/off feedback wait time counter register	16.3.3.2.47/1089
PD_BLK4_SW_CNT	0x154	GPU power domain power on/off feedback wait time counter register	16.3.3.2.48/1089
PD_BLK5_SW_CNT	0x158	DSP0 power domain power on/off feedback wait time counter register	16.3.3.2.49/1090
PD_BLK6_SW_CNT	0x15c	DSP1 power domain power on/off	16.3.3.2.50/1090

Register	Offset	Description	Section/Page
		feedback wait time counter register	
PD_BLK7_SW_CNT	0x160	C910 core0 power domain power on/off feedback wait time counter register	16.3.3.2.51/1090
PD_BLK8_SW_CNT	0x164	C910 core1 power domain power on/off feedback wait time counter register	16.3.3.2.52/1091
PD_BLK9_SW_CNT	0x168	C910 core2 power domain power on/off feedback wait time counter register	16.3.3.2.53/1091
PD_BLK10_SW_CNT	0x16c	C910 core3 power domain power on/off feedback wait time counter register	16.3.3.2.54/1092
PD_BLK0_INTV_CNT	0x180	AUDIO_SUBSYS PMU state transition wait time counter register	16.3.3.2.55/1092
PD_BLK1_INTV_CNT	0x184	VDEC PMU state transition wait time counter register	16.3.3.2.56/1092
PD_BLK2_INTV_CNT	0x188	NPU PMU state transition wait time counter register	16.3.3.2.57/1093
PD_BLK3_INTV_CNT	0x18c	VENC PMU state transition wait time counter register	16.3.3.2.58/1093
PD_BLK4_INTV_CNT	0x190	GPU PMU state transition wait time counter register	16.3.3.2.59/1094
PD_BLK5_INTV_CNT	0x194	DSP0 PMU state transition wait time counter register	16.3.3.2.60/1094
PD_BLK6_INTV_CNT	0x198	DSP1 PMU state transition wait time counter register	16.3.3.2.61/1094
PD_BLK7_INTV_CNT	0x19c	C910 core0 PMU state transition wait time counter register	16.3.3.2.62/1095
PD_BLK8_INTV_CNT	0x1a0	C910 core1 PMU state transition wait time counter register	16.3.3.2.63/1095
PD_BLK9_INTV_CNT	0x1a4	C910 core2 PMU state transition wait time counter register	16.3.3.2.64/1096
PD_BLK10_INTV_CNT	0x1a8	C910 core3 PMU state transition wait time counter register	16.3.3.2.65/1096
AUDIO_PMU_REQ	0x1f8	AUDIO_SUBSYS low power request register	16.3.3.2.66/1097
AUDIO_PMU_STS	0x1fc	AUDIO_SUBSYS low power status register	16.3.3.2.67/1097
AUDIO_PMU_INTR	0x204	AUDIO_SUBSYS low power interrupt control and status register	16.3.3.2.68/1097

Register	Offset	Description	Section/Page
PMU_AUDIO_REQ	0x208	Low power request from AON_SUBSYS to AUDIO_SUBSYS	16.3.3.2.69/1098
PMU_AUDIO_STS	0x20c	Low power status data from AON_SUBSYS to AUDIO_SUBSYS	16.3.3.2.70/1098
MEM_LP_MODE	0x210	Memory low power mode control register	16.3.3.2.71/1098
C910_DBG_MASK	0x214	C910 debug enable control register	16.3.3.2.72/1100
C910_L2CACHE	0x218	C910 L2CACHE flush control and status register	16.3.3.2.73/1100
EFUSE_PRELOAD_DONE	0x224	eFuse preload completion status register	16.3.3.2.74/1101
PLL_DSKEW_LOCK	0x22c	PLL calibration control register	16.3.3.2.75/1101
SRAM_AXI_CFG	0x230	SRAMC configuration register	16.3.3.2.76/1101
SRAM_AXI_ST	0x234	SRAMC status register	16.3.3.2.77/1102
SRAM_AXI_ERR_STS_0	0x238	SRAMC error status register 0	16.3.3.2.78/1102
SRAM_AXI_ERR_STS_1	0x23c	SRAMC error status register 1	16.3.3.2.79/1103
SRAM_AXI_ERR_STS_2	0x240	SRAMC error status register 2	16.3.3.2.80/1103
SRAM_AXI_ERR_STS_3	0x244	SRAMC error status register 3	16.3.3.2.81/1103
SRAM_AXI_ERR_STS_4	0x248	SRAMC error status register 4	16.3.3.2.82/1103
SE_MUX_LOCK	0x24c	Secure IO PADMUX registers' lock register	16.3.3.2.83/1103
CPU_DBG_DIS_LOCK	0x270	Lock signal for CPU_DBG_DIS signal in MPJTAG	16.3.3.2.84/1104

16.3.2.3 DDR_SUBSYS Control Registers

Register	Offset	Description	Section/Page
DDR_STS0	0x1c	DDR SYS status	16.3.3.3.1/1104
MRR_STS_CH0	0x2c	ch0 MRR value	16.3.3.3.2/1105
MRR_STS_CH1	0x30	ch1 MRR value	16.3.3.3.3/1105
DDR_STS1	0x34	DDR monitor configuration	16.3.3.3.4/1105
DDR_STS2	0x38	DDR Monitor configuration	16.3.3.3.5/1106
DFI0_INFO	0x3c	Debug status0	16.3.3.3.6/1106
DDR_SRAM_CFG	0x40	DDR SDRAM LP mode configuration	16.3.3.3.7/1107

Register	Offset	Description	Section/Page
DFI1_INFO	0x44	Error status of DFI1	16.3.3.3.8/1109
BPAC_CFG0	0x48	PHY bypass mode configuration	16.3.3.3.9/1109
BPAC_CFG1	0x4c	PHY bypass mode configuration	16.3.3.3.10/1110
BPAC_STS	0x50	PHY bypass mode configuration	16.3.3.3.11/1110
BPDA_CFG0	0x54	PHY bypass mode configuration	16.3.3.3.12/1110
BPDA_CFG1	0x58	PHY bypass mode configuration	16.3.3.3.13/1110
BPDA_CFG2	0x5c	PHY bypass mode configuration	16.3.3.3.14/1111
BPDA_CFG3	0x60	PHY bypass mode configuration	16.3.3.3.15/1111
BPDA_STS0	0x64	PHY bypass mode configuration	16.3.3.3.16/1111
BPDA_STS1	0x68	PHY bypass mode configuration	16.3.3.3.17/1112
BPMA_CFG	0x6c	PHY bypass mode configuration	16.3.3.3.18/1112
BPAC_DCH_CFG0	0x70	PHY bypass mode configuration	16.3.3.3.19/1112
BPAC_DCH_CFG1	0x74	PHY bypass mode configuration	16.3.3.3.20/1113
BPAC_DCH_STS	0x78	PHY bypass mode configuration	16.3.3.3.21/1113
BPDA_DCH_CFG0	0x7c	PHY bypass mode configuration	16.3.3.3.22/1113
BPDA_DCH_CFG1	0x80	PHY bypass mode configuration	16.3.3.3.23/1114
BPDA_DCH_CFG2	0x84	PHY bypass mode configuration	16.3.3.3.24/1114
BPDA_DCH_CFG3	0x88	PHY bypass mode configuration	16.3.3.3.25/1114
BPDA_DCH_STS0	0x8c	PHY bypass mode configuration	16.3.3.3.26/1115
BPDA_DCH_STS1	0x90	PHY bypass mode configuration	16.3.3.3.27/1115
BPMA_DCH_CFG	0x94	PHY bypass mode configuration	16.3.3.3.28/1115

16.3.2.4 DSP_SUBSYS Control Registers

Register	Offset	Description	Section/Page
TEST_CLK_FREQ_STAT	0x2c	Clock frequency status register	16.3.3.4.1/1116
TEST_CLK_CFG	0x30	Test clock configuration register	16.3.3.4.2/1116
AXI4_DSPSYS_PRI	0x34	AXI4 bus priority configuration register	16.3.3.4.3/1117
AXI4_DSPSYS_PRI_SLV	0x38	AXI4 slave bus priority configuration register	16.3.3.4.4/1118

Register	Offset	Description	Section/Page
DSP0_BUS_ADDR	0x90	DSP0 MSB8 address register	16.3.3.4.5/1118
DSP1_BUS_ADDR	0x94	DSP1 MSB8 address register	16.3.3.4.6/1119
DSP_REMAP	0x98	DSP address remap enable register	16.3.3.4.7/1119
DSP_DDR_CH_SEL	0x9c	DSP access DDR bus select register	16.3.3.4.8/1120
TEST_CLK_FREQ_STAT_TEE	0x102c	Clock frequency status TEE register	16.3.3.4.9/1120
TEST_CLK_CFG_TEE	0x1030	Test clock configuration TEE register	16.3.3.4.10/1120
AXI4_DSPSYS_PRI_TEE	0x1034	AXI4 bus priority configuration TEE register	16.3.3.4.11/1121
AXI4_DSPSYS_PRI_SLV_TEE	0x1038	AXI4 slave bus priority configuration TEE register	16.3.3.4.12/1122
DSP0_BUS_ADDR_TEE	0x1090	DSP0 MSB8 address TEE register	16.3.3.4.13/1122
DSP1_BUS_ADDR_TEE	0x1094	DSP1 MSB8 address TEE register	16.3.3.4.14/1122
DSP_REMAP_TEE	0x1098	DSP address remap enable TEE register	16.3.3.4.15/1123
DSP_DDR_CH_SEL_TEE	0x109c	DSP access DDR bus select TEE register	16.3.3.4.16/1123
CFG_CLK_LOCK_TEE	0x1140	Clock lock TEE register	16.3.3.4.17/1124
CFG_RST_LOCK_TEE	0x1144	Reset lock TEE register	16.3.3.4.18/1124
CFG_DSPSYS_LOCK_TEE	0x1148	DSP subsystem lock TEE register	16.3.3.4.19/1125

16.3.2.5 PERI_SUBSYS Control Registers

Register	Offset	Description	Section/Page
USB3_AXI_QOS_PRIORITY	0x200	USB AXI bus configuration register	16.3.3.5.1/1126
GMAC_AXI_QOS_PRIORITY	0x204	GMAC AXI bus configuration register	16.3.3.5.2/1126
EMMC_AXI_QOS_PRIORITY	0x208	eMMC AXI bus configuration register	16.3.3.5.3/1126
SDIO0_AXI_QOS_PRIORITY	0x20c	SDIO0 AXI bus configuration register	16.3.3.5.4/1127
SDIO1_AXI_QOS_PRIORITY	0x210	SDIO1 AXI bus configuration register	16.3.3.5.5/1127
EMMC_TEST_CTRL	0x220	eMMC test register 0	16.3.3.5.6/1128
EMMC_TEST_PAD_O	0x224	eMMC test signal output	16.3.3.5.7/1128
EMMC_TEST_PAD_OEN	0x228	eMMC test signal output enable	16.3.3.5.8/1128
EMMC_TEST_PAD_I	0x22c	eMMC test signal input	16.3.3.5.9/1129
SDIO0_TEST_CTRL	0x230	SDIO0 test register 0	16.3.3.5.10/1129

Register	Offset	Description	Section/Page
SDIO0_TEST_PAD_O	0x234	SDIO0 test signal output	16.3.3.5.11/1129
SDIO0_TEST_PAD_OEN	0x238	SDIO0 test signal output enable	16.3.3.5.12/1130
SDIO0_TEST_PAD_I	0x23c	SDIO0 test signal input	16.3.3.5.13/1130
SDIO1_TEST_CTRL	0x240	SDIO1 test register 0	16.3.3.5.14/1130
SDIO1_TEST_PAD_O	0x244	SDIO1 test signal output	16.3.3.5.15/1131
SDIO1_TEST_PAD_OEN	0x248	SDIO1 test signal output enable	16.3.3.5.16/1131
SDIO1_TEST_PAD_I	0x24c	SDIO1 test signal input	16.3.3.5.17/1131
SW_REG0	0x300	Software register 0	16.3.3.5.18/1131
SW_REG1	0x304	Software register 1	16.3.3.5.19/1132
SW_REG2	0x308	Software register 2	16.3.3.5.20/1132
SW_REG3	0x30C	Software register 3	16.3.3.5.21/1132
USB3_AXI_QOS_PRIORITY_TEE	0x1200	USB AXI bus configuration register	16.3.3.5.22/1132
GMAC_AXI_QOS_PRIORITY_TEE	0x1204	GMAC AXI bus configuration register	16.3.3.5.23/1133
EMMC_AXI_QOS_PRIORITY_TEE	0x1208	eMMC AXI bus configuration register	16.3.3.5.24/1133
SDIO0_AXI_QOS_PRIORITY_TEE	0x120c	SDIO0 AXI bus configuration register	16.3.3.5.25/1133
SDIO1_AXI_QOS_PRIORITY_TEE	0x1210	SDIO1 AXI bus configuration register	16.3.3.5.26/1134
TEE_AXI_QOS_PRIORITY_TEE	0x1214	TEE AXI bus configuration register	16.3.3.5.27/1134
MISCSYS_AXI_QOS_PRIORITY_TEE	0x1218	MISC AXI bus configuration register	16.3.3.5.28/1135
EMMC_TEST_CTRL_TEE	0x1220	eMMC test register 0	16.3.3.5.29/1135
EMMC_TEST_PAD_O_TEE	0x1224	eMMC test signal output	16.3.3.5.30/1135
EMMC_TEST_PAD_OEN_TEE	0x1228	eMMC test signal output enable	16.3.3.5.31/1136
EMMC_TEST_PAD_I_TEE	0x122c	eMMC test signal input	16.3.3.5.32/1136
SDIO0_TEST_CTRL_TEE	0x1230	SDIO0 test register 0	16.3.3.5.33/1136
SDIO0_TEST_PAD_O_TEE	0x1234	SDIO0 test signal output	16.3.3.5.34/1137
SDIO0_TEST_PAD_OEN_TEE	0x1238	SDIO0 test signal output enable	16.3.3.5.35/1137
SDIO0_TEST_PAD_I_TEE	0x123c	SDIO0 test signal input	16.3.3.5.36/1137
SDIO1_TEST_CTRL_TEE	0x1240	SDIO1 test register 0	16.3.3.5.37/1137
SDIO1_TEST_PAD_O_TEE	0x1244	SDIO1 test signal output	16.3.3.5.38/1138

Register	Offset	Description	Section/Page
SDIO1_TEST_PAD_OEN_TEE	0x1248	SDIO1 test signal output enable	16.3.3.5.39/1138
SDIO1_TEST_PAD_I_TEE	0x124c	SDIO1 test signal input	16.3.3.5.40/1138
SW_REG0_TEE	0x1300	Software register 0	16.3.3.5.41/1139
SW_REG1_TEE	0x1304	Software register 1	16.3.3.5.42/1139
SW_REG2_TEE	0x1308	Software register 2	16.3.3.5.43/1139
SW_REG3_TEE	0x130C	Software register 3	16.3.3.5.44/1139
SYSREG_LOCK_0_TEE	0x1800	MISC_SUBSYS sysreg lock registers	16.3.3.5.45/1140

16.3.2.6 VI_SUBSYS Control Registers

Register	Offset	Description	Section/Page
VISYS_CONTROL	0x120	VISYS_CONTROL	16.3.3.6.1/1141
MIPI_CSI0_CTRL	0x140	MIPI_CSI0_CTRL	16.3.3.6.2/1143
MIPI_CSI1_CTRL	0x144	MIPI_CSI1_CTRL	16.3.3.6.3/1144
MIPI_CSI2_CTRL	0x148	MIPI_CSI2_CTRL	16.3.3.6.4/1145
MIPI_CSI_FIFO_CTRL	0x14C	MIPI_CSI_FIFO_CTRL	16.3.3.6.5/1146
AXI4_VISYS1_PRI	0x150	AXI4_VISYS1_PRI	16.3.3.6.6/1147
AXI4_VISYS2_PRI	0x154	AXI4_VISYS2_PRI	16.3.3.6.7/1148
AXI4_VISYS3_PRI	0x158	AXI4_VISYS3_PRI	16.3.3.6.8/1148
AXI4_VISYS_PRI	0x160	AXI4_VISYS_PRI	16.3.3.6.9/1149
VI_MMU_QOS	0x164	VI_MMU_QOS	16.3.3.6.10/1150
DEC400_STATUS	0x16c	DEC400 idle status	16.3.3.6.11/1151
VI_RSV_REG_0	0x170	Reserved register	16.3.3.6.12/1151
VI_VERSION_REG_0	0x174	Version register	16.3.3.6.13/1152
MIPI_CSI2_FPGA	0x180	MIPI_CSI2_FPGA	16.3.3.6.14/1152
MIPI_CSI2X2_FPGA	0x184	MIPI_CSI2X2_FPGA	16.3.3.6.15/1152
DSP0_CPU_INT_MASK	0x190	DSP0_CPU_INT_MASK	16.3.3.6.16/1153
DSP0_CPU_INT_CLR	0x194	DSP0_CPU_INT_CLR	16.3.3.6.17/1154
DSP0_CPU_INT_STA	0x198	DSP0_CPU_INT_STA	16.3.3.6.18/1154
DSP1_CPU_INT_MASK	0x1a0	DSP1_CPU_INT_MASK	16.3.3.6.19/1155

Register	Offset	Description	Section/Page
DSP1_CPU_INT_CLR	0x1a4	DSP1_CPU_INT_CLR	16.3.3.6.20/1155
DSP1_CPU_INT_STA	0x1a8	DSP1_CPU_INT_STA	16.3.3.6.21/1155
CPU_DSP0_INT_MASK	0x1b0	CPU_DSP0_INT_MASK	16.3.3.6.22/1156
CPU_DSP0_INT_CLR	0x1b4	CPU_DSP0_INT_CLR	16.3.3.6.23/1156
CPU_DSP0_INT_STA	0x1b8	CPU_DSP0_INT_STA	16.3.3.6.24/1157
CPU_DSP1_INT_MASK	0x1c0	CPU_DSP1_INT_MASK	16.3.3.6.25/1157
CPU_DSP1_INT_CLR	0x1c4	CPU_DSP1_INT_CLR	16.3.3.6.26/1158
CPU_DSP1_INT_STA	0x1c8	CPU_DSP1_INT_STA	16.3.3.6.27/1158
DSP0_DSP1_INT_MASK	0x1d0	DSP0_DSP1_INT_MASK	16.3.3.6.28/1159
DSP0_DSP1_INT_CLR	0x1d4	DSP0_DSP1_INT_CLR	16.3.3.6.29/1159
DSP0_DSP1_INT_STA	0x1d8	DSP0_DSP1_INT_STA	16.3.3.6.30/1159
DSP1_DSP0_INT_MASK	0x1e0	DSP1_DSP0_INT_MASK	16.3.3.6.31/1160
DSP1_DSP0_INT_CLR	0x1e4	DSP1_DSP0_INT_CLR	16.3.3.6.32/1160
DSP1_DSP0_INT_STA	0x1e8	DSP1_DSP0_INT_STA	16.3.3.6.33/1161
DSP0_INT_STA	0x1f0	DSP0_INT_STA	16.3.3.6.34/1161
DSP1_INT_STA	0x1f4	DSP1_INT_STA	16.3.3.6.35/1161
VISYS_CONTROL_TEE	0x1120	VISYS_CONTROL	16.3.3.6.36/1162
MIPI_CSI0_CTRL_TEE	0x1140	MIPI_CSI0_CTRL	16.3.3.6.37/1163
MIPI_CSI1_CTRL_TEE	0x1144	MIPI_CSI1_CTRL	16.3.3.6.38/1164
MIPI_CSI2_CTRL_TEE	0x1148	MIPI_CSI2_CTRL	16.3.3.6.39/1165
MIPI_CSI_FIFO_CTRL_TEE	0x114C	MIPI_CSI_FIFO_CTRL	16.3.3.6.40/1166
AXI4_VISYS1_PRI_TEE	0x1150	AXI4_VISYS1_PRI	16.3.3.6.41/1167
AXI4_VISYS2_PRI_TEE	0x1154	AXI4_VISYS2_PRI	16.3.3.6.42/1168
AXI4_VISYS3_PRI_TEE	0x1158	AXI4_VISYS3_PRI	16.3.3.6.43/1169
AXI4_VISYS_PRI_TEE	0x1160	AXI4_VISYS_PRI	16.3.3.6.44/1170
VI_MMU_QOS_TEE	0x1164	VI_MMU_QOS	16.3.3.6.45/1170
VI_RSV_REG_0_TEE	0x1170	Reserved register	16.3.3.6.46/1171
DSP0_CPU_INT_MASK_TEE	0x1190	DSP0_CPU_INT_MASK	16.3.3.6.47/1171
DSP0_CPU_INT_CLR_TEE	0x1194	DSP0_CPU_INT_CLR	16.3.3.6.48/1172

Register	Offset	Description	Section/Page
DSP0_CPU_INT_STA_TEE	0x1198	DSP0_CPU_INT_STA	16.3.3.6.49/1172
DSP1_CPU_INT_MASK_TEE	0x11a0	DSP1_CPU_INT_MASK	16.3.3.6.50/1173
DSP1_CPU_INT_CLR_TEE	0x11a4	DSP1_CPU_INT_CLR	16.3.3.6.51/1173
DSP1_CPU_INT_STA_TEE	0x11a8	DSP1_CPU_INT_STA	16.3.3.6.52/1173
CPU_DSP0_INT_MASK_TEE	0x11b0	CPU_DSP0_INT_MASK	16.3.3.6.53/1174
CPU_DSP0_INT_CLR_TEE	0x11b4	CPU_DSP0_INT_CLR	16.3.3.6.54/1174
CPU_DSP0_INT_STA_TEE	0x11b8	CPU_DSP0_INT_STA	16.3.3.6.55/1175
CPU_DSP1_INT_MASK_TEE	0x11c0	CPU_DSP1_INT_MASK	16.3.3.6.56/1175
CPU_DSP1_INT_CLR_TEE	0x11c4	CPU_DSP1_INT_CLR	16.3.3.6.57/1176
CPU_DSP1_INT_STA_TEE	0x11c8	CPU_DSP1_INT_STA	16.3.3.6.58/1176
DSP0_DSP1_INT_MASK_TEE	0x11d0	DSP0_DSP1_INT_MASK	16.3.3.6.59/1177
DSP0_DSP1_INT_CLR_TEE	0x11d4	DSP0_DSP1_INT_CLR	16.3.3.6.60/1177
DSP0_DSP1_INT_STA_TEE	0x11d8	DSP0_DSP1_INT_STA	16.3.3.6.61/1177
DSP1_DSP0_INT_MASK_TEE	0x11e0	DSP1_DSP0_INT_MASK	16.3.3.6.62/1178
DSP1_DSP0_INT_CLR_TEE	0x11e4	DSP1_DSP0_INT_CLR	16.3.3.6.63/1178
DSP1_DSP0_INT_STA_TEE	0x11e8	DSP1_DSP0_INT_STA	16.3.3.6.64/1179
CFG_FUNC_LOCK_TEE	0x1220	VI function registers TEE lock	16.3.3.6.65/1179

16.3.2.7 VO_SUBSYS Control Registers

Register	Offset	Description	Section/Page
VOSYS_GPU_SYSREG	0x6c	GPU dxt bc enable register	16.3.3.7.1/1181
VOSYS_GPU_SYSREG1	0x70	GPU idle indicate register	16.3.3.7.2/1181
VOSYS_MIPIDSI0_SYSREG	0x74	DSI0 control register	16.3.3.7.3/1181
VOSYS_MIPIDSI1_SYSREG	0x78	DSI1 control register	16.3.3.7.4/1182
AXI4_VO_BUS_CFG	0xa0	AXI4_VO bus priority register	16.3.3.7.5/1182
IOPMP_VOSYS_GPU_QOS	0xa4	GPU IOPMP QoS register	16.3.3.7.6/1183
DPU1_SELECT	0xa8	DPU1 pixel clock mux register	16.3.3.7.7/1183
DSI0_VSYNC_CFG	0xac	DSI0 polarity register for FPGA	16.3.3.7.8/1184
DSI0_HALT_MASK	0xb4	DSI0 halt error mask register for FPGA	16.3.3.7.9/1184

Register	Offset	Description	Section/Page
DSI1_VSYNC_CFG	0xb8	DSI1 polarity register for FPGA	16.3.3.7.10/1185
DSI1_HALT_ERR	0xbc	DSI1 halt error register	16.3.3.7.11/1185
DSI1_HALT_MASK	0xc0	DSI1 halt error mask register for FPGA	16.3.3.7.12/1185
TEST_CLK_FREQ_STAT	0xc4	Clock frequency register	16.3.3.7.13/1186
TEST_CLK_CFG	0xc8	Clock sample control register	16.3.3.7.14/1186
GPU_GPIO	0xcc	GPU GPIO register	16.3.3.7.15/1186
HDMI_COLOR_BAR_CFG	0xd0	HDMI color bar control register	16.3.3.7.16/1187
GPU_CNT_CLR	0xd4	GPU timer counter clean register	16.3.3.7.17/1188
GPU_CNT_VALUE	0xd8	GPU timer counter value register	16.3.3.7.18/1188
DPU_ADDR_REMAP	0xe0	DPU address remap register	16.3.3.7.19/1188
MIPI_DSI0_ZCAL_RSTZ_SYSREG	0x100	mipi_dsi0_zcal_rstz register	16.3.3.7.20/1189
MIPI_DSI0_ZCAL_DONE_SYSREG	0x104	mipi_dsi0_zcal_done register for FPGA	16.3.3.7.21/1189
MIPI_DSI0_GLUEIFTESTER_SYSREG	0x108	mipi_dsi0_glueiftester register for FPGA	16.3.3.7.22/1189
MIPI_DSI0_CLKEXT_SYSREG	0x10c	mipi_dsi0_clkext register for FPGA	16.3.3.7.23/1189
MIPI_DSI0_DIV_EN_IN_TX_SYSREG	0x110	mipi_dsi0_div_en_in_tx register for FPGA	16.3.3.7.24/1190
MIPI_DSI0_CLOCKUNGATING_IN_TX_SYSREG	0x114	mipi_dsi0_clockungating_in_tx register for FPGA	16.3.3.7.25/1190
MIPI_DSI0_CLOCK8SENT_IN_TX_SYSREG	0x118	mipi_dsi0_clock8sent_in_tx register for FPGA	16.3.3.7.26/1190
MIPI_DSI0_CLK_KILL_IN_TX_SYSREG	0x11c	mipi_dsi0_clk_kill_in_tx register for FPGA	16.3.3.7.27/1190
MIPI_DSI0_CLK_EN_IN_TX_SYSREG	0x120	mipi_dsi0_clk_en_in_tx register for FPGA	16.3.3.7.28/1191
MIPI_DSI0_HSTRAILDONE_IN_TX_SYSREG	0x124	mipi_dsi0_hstraildone_in_tx register for FPGA	16.3.3.7.29/1191
MIPI_DSI1_ZCAL_RSTZ_SYSREG	0x130	mipi_dsi1_zcal_rstz register for FPGA	16.3.3.7.30/1191
MIPI_DSI1_ZCAL_DONE_SYSREG	0x134	mipi_dsi1_zcal_done register for FPGA	16.3.3.7.31/1192
MIPI_DSI1_GLUEIFTESTER_SYSREG	0x138	mipi_dsi1_glueiftester register for FPGA	16.3.3.7.32/1192
MIPI_DSI1_CLKEXT_SYSREG	0x13c	mipi_dsi1_clkext register for FPGA	16.3.3.7.33/1192

Register	Offset	Description	Section/Page
MIPI_DSI1_DIV_EN_IN_TX_SYSREG	0x140	mipi_dsi1_div_en_in_tx register for FPGA	16.3.3.7.34/1192
MIPI_DSI1_CLOCKUNGATING_IN_TX_SYSREG	0x144	mipi_dsi1_clockungating_in_tx register for FPGA	16.3.3.7.35/1193
MIPI_DSI1_CLOCK8SENT_IN_TX_SYSREG	0x148	mipi_dsi1_clock8sent_in_tx register for FPGA	16.3.3.7.36/1193
MIPI_DSI1_CLK_KILL_IN_TX_SYSREG	0x14c	mipi_dsi1_clk_kill_in_tx register for FPGA	16.3.3.7.37/1193
MIPI_DSI1_CLK_EN_IN_TX_SYSREG	0x150	mipi_dsi1_clk_en_in_tx register for FPGA	16.3.3.7.38/1193
MIPI_DSI1_HSTRAILDONE_IN_TX_SYSREG	0x154	mipi_dsi1_hstraildone_in_tx register for FPGA	16.3.3.7.39/1194
HDMI_ZCAL_RSTZ_SYSREG	0x160	hdmi_zcal_rstz register for FPGA	16.3.3.7.40/1194
HDMI_ZCAL_DONE_SYSREG	0x164	hdmi_zcal_done register for FPGA	16.3.3.7.41/1194
HDMI_CONTINUITY_SYSREG	0x168	hdmi_cont_en register for FPGA	16.3.3.7.42/1194
HDMI_BIST_SYSREG	0x16c	hdmi_bisten register for FPGA	16.3.3.7.43/1195
RESERVED_REG_0	0x200	Reserved register	16.3.3.7.44/1195
RESERVED_REG_1	0x204	Reserved register	16.3.3.7.45/1195
RESERVED_REG_2	0x208	Reserved register	16.3.3.7.46/1196
RESERVED_REG_3	0x20c	Reserved register	16.3.3.7.47/1196
VOSYS_GPU_SYSREG_TEE	0x106c	GPU dxt_bc TEE register	16.3.3.7.48/1196
VOSYS_GPU_SYSREG1_TEE	0x1070	GPU idle TEE register	16.3.3.7.49/1196
VOSYS_MIPIDSI0_SYSREG_TEE	0x1074	DSI0 control TEE register	16.3.3.7.50/1197
VOSYS_MIPIDSI1_SYSREG_TEE	0x1078	DSI1 control TEE register	16.3.3.7.51/1197
AXI4_VO_BUS_CFG_TEE	0x10a0	AXI4_VO bus priority TEE register	16.3.3.7.52/1198
IOPMP_VOSYS_GPU_QOS_TEE	0x10a4	GPU IOPMP QoS TEE register	16.3.3.7.53/1198
DPU1_SELECT_TEE	0x10a8	DPU1 pixel clock mux TEE register	16.3.3.7.54/1199
DSI0_VSYNC_CFG_TEE	0x10ac	DSI0 polarity TEE register for FPGA	16.3.3.7.55/1199
DSI0_HALT_ERR_TEE	0x10b0	DSI0 halt error mask TEE register	16.3.3.7.56/1200
DSI0_HALT_MASK_TEE	0x10b4	DSI0 halt mask TEE register	16.3.3.7.57/1200
DSI1_VSYNC_CFG_TEE	0x10b8	DSI1 polarity TEE register for FPGA	16.3.3.7.58/1200

Register	Offset	Description	Section/Page
DSI1_HALT_ERR_TEE	0x10bc	DSI1 halt error TEE register	16.3.3.7.59/1201
DSI1_HALT_MASK_TEE	0x10c0	DSI1 halt mask TEE register	16.3.3.7.60/1201
TEST_CLK_FREQ_STAT_TEE	0x10c4	Test clock frequency TEE register	16.3.3.7.61/1201
TEST_CLK_CFG_TEE	0x10c8	Test clock configuration TEE register	16.3.3.7.62/1202
GPU_GPIO_TEE	0x10cc	GPU GPIO TEE register	16.3.3.7.63/1202
HDMI_COLOR_BAR_CFG_TEE	0x10d0	HDMI color bar configuration TEE register	16.3.3.7.64/1203
GPU_CNT_CLR_TEE	0x10d4	GPU timer counter clean TEE register	16.3.3.7.65/1203
GPU_CNT_VALUE_TEE	0x10d8	GPU timer counter value TEE register	16.3.3.7.66/1204
DPU_ADDR_REMAP_TEE	0x10e0	DPU address remap TEE register	16.3.3.7.67/1204
HDMI_CONTINUITY_SYSREG_TEE	0x1168	HDMI continuity TEE register	16.3.3.7.68/1204
HDMI_BIST_SYSREG_TEE	0x116c	HDMI bist TEE register	16.3.3.7.69/1205
RESERVED_REG_0_TEE	0x1200	Reserved TEE register	16.3.3.7.70/1205
RESERVED_REG_1_TEE	0x1204	Reserved TEE register	16.3.3.7.71/1205
RESERVED_REG_2_TEE	0x1208	Reserved TEE register	16.3.3.7.72/1205
RESERVED_REG_3_TEE	0x120c	Reserved TEE register	16.3.3.7.73/1206
CFG_LOCK_TEE	0x1a00	Configuration lock TEE register	16.3.3.7.74/1206

16.3.2.8 VP_SUBSYS Control Registers

Register	Offset	Description	Section/Page
VPSYS_DBG_STS	0x40	VPSYS_DBG_STS	16.3.3.8.1/1207
VPSYS_VDEC_FUSE_CFG	0x44	VPSYS_VDEC_FUSE_CFG	16.3.3.8.2/1207
VPSYS_VENC_FUSE_CFG	0x48	VPSYS_VENC_FUSE_CFG	16.3.3.8.3/1207
VPSYS_ADDR_SEL	0x60	VPSYS_ADDR_SEL	16.3.3.8.4/1207
VPSYS_DBG_TEESTS	0x1040	VPSYS_DBG_TEESTS	16.3.3.8.5/1208
VPSYS_VDEC_FUSE_TEECFG	0x1044	VPSYS_VDEC_FUSE_TEECFG	16.3.3.8.6/1208
VPSYS_VENC_FUSE_TEECFG	0x1048	VPSYS_VENC_FUSE_TEECFG	16.3.3.8.7/1209
LOCK_CFG	0x1800	LOCK_CFG	16.3.3.8.8/1209
VPSYS_ADDR_TEESEL	0x1060	VPSYS_ADDR_TEESEL	16.3.3.8.9/1210

16.3.3 Register and Field Description

16.3.3.1 System Control Registers

16.3.3.1.1 BOOT_REG0

- Description: General purpose register for bootloader
- Offset: 0x0
- Default Value: 0xff810010

Bits	Field Name	Access	Description
[31:0]	BOOT_REG0	RW	General purpose register for bootloader Value After Reset: 0xFF810010

16.3.3.1.2 BOOT_REG1

- Description: General purpose register for bootloader
- Offset: 0x4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	BOOT_REG1	RW	General purpose register for bootloader Value After Reset: 0x0

16.3.3.1.3 BOOT_REG2

- Description: General purpose register for bootloader
- Offset: 0x8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	BOOT_REG2	RW	General purpose register for bootloader Value After Reset: 0x0

16.3.3.1.4 BOOT_REG3

- Description: General purpose register for bootloader
- Offset: 0xC
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	BOOT_REG3	RW	General purpose register for bootloader Value After Reset: 0x0

16.3.3.1.5 BOOT_SEL

- Description: Boot media selection
- Offset: 0x10
- Default Value: 0x10

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	BOOT_SEL_UPDT	W1S	bootsel update, write any non-zero value to current register will set this bit, and then will lock input pad to boot_sel[3:0]. Value After Reset: 0x1
[3:0]	BOOT_SEL	RO	BOOT media selection Value After Reset: 0x0

16.3.3.1.6 C910_CTRL0

- Description: C910 CPU system control
- Offset: 0x14
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	C910_COUNTER_CLR	RW	C910 CPU timer counter clear Value After Reset: 0x0
[3:1]	C910_CORE_ASYNC_MODE	RW	Set C910 core1/2/3 and bus in asynchronous mode. One bit represents one core. 1: core[i] and bus are in asynchronous mode. 0: core[i] and bus are in synchronous mode. Value After Reset: 0x0
[0]	C910_CORE0_ASYNC_MODE	RO	Set C910 core0 and bus in asynchronous mode. 1: core0 and bus are in asynchronous mode. 0: core0 and bus are in synchronous mode. Value After Reset: 0x0

16.3.3.1.7 SOC_VER

- Description: SoC chip version register
- Offset: 0x20
- Default Value: 0x10001018

Bits	Field Name	Access	Description
[31:28]	ID_VER	RO	Current ID register version. Different ID version has different register field definition. Value After Reset: 0x1
[27:24]	SOC_IMPL	RO	SoC implementation form. 0x0 for ASIC. Value After Reset: 0x0
[23:16]	RESERVED_1	-	
[15:6]	SOC_ID	RO	SoC ID, different project has a different ID. Value After Reset: 0x40
[5:0]	RELEASE_VER	RO	Release version Value After Reset: 0x18

16.3.3.1.8 SW_REG0

- Description: General purpose register for software use
- Offset: 0x40
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG0	RW	General purpose register for software use Value After Reset: 0x0

16.3.3.1.9 SW_REG1

- Description: General purpose register for software use
- Offset: 0x44
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG1	RW	General purpose register for software use Value After Reset: 0x0

16.3.3.1.10 SW_REG2

- Description: General purpose register for software use
- Offset: 0x48
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG2	RW	General purpose register for software use

Bits	Field Name	Access	Description
			Value After Reset: 0x0

16.3.3.1.11 SW_REG3

- Description: General purpose register for software use
- Offset: 0x4C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG3	RW	General purpose register for software use Value After Reset: 0x0

16.3.3.1.12 C910_CORE0_RVBA_L

- Description: C910 core0 reset entry address lower bits
- Offset: 0x50
- Default Value: 0xffd00000

Bits	Field Name	Access	Description
[31:0]	C910_CORE0_RVBA_31_0	RW	C910 core0 reset entry address lower bits Value After Reset: 0xFFD00000

16.3.3.1.13 C910_CORE0_RVBA_H

- Description: C910 core0 reset entry address upper bits
- Offset: 0x54
- Default Value: 0xff

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	C910_CORE0_RVBA_39_32	RW	C910 core0 reset entry address upper bits Value After Reset: 0xFF

16.3.3.1.14 C910_CORE1_RVBA_L

- Description: C910 core1 reset entry address lower bits
- Offset: 0x58
- Default Value: 0xffd00000

Bits	Field Name	Access	Description
[31:0]	C910_CORE1_RVBA_31_0	RW	C910 core1 reset entry address lower bits

Bits	Field Name	Access	Description
			Value After Reset: 0xFFD00000

16.3.3.1.15 C910_CORE1_RVBA_H

- Description: C910 core1 reset entry address upper bits
- Offset: 0x5C
- Default Value: 0xff

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	C910_CORE1_RVBA_39_32	RW	C910 core1 reset entry address upper bits Value After Reset: 0xFF

16.3.3.1.16 C910_CORE2_RVBA_L

- Description: C910 core2 reset entry address lower bits
- Offset: 0x60
- Default Value: 0xffd00000

Bits	Field Name	Access	Description
[31:0]	C910_CORE2_RVBA_31_0	RW	C910 core2 reset entry address lower bits Value After Reset: 0xFFD00000

16.3.3.1.17 C910_CORE2_RVBA_H

- Description: C910 core2 reset entry address upper bits
- Offset: 0x64
- Default Value: 0xff

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	C910_CORE2_RVBA_39_32	RW	C910 core2 reset entry address upper bits Value After Reset: 0xFF

16.3.3.1.18 C910_CORE3_RVBA_L

- Description: C910 core3 reset entry address lower bits
- Offset: 0x68
- Default Value: 0xffd00000

Bits	Field Name	Access	Description
[31:0]	C910_CORE3_RVBA_31_0	RW	C910 core3 reset entry address lower bits Value After Reset: 0xFFD00000

16.3.3.1.19 C910_CORE3_RVBA_H

- Description: C910 core3 reset entry address upper bits
- Offset: 0x6C
- Default Value: 0xff

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	C910_CORE3_RVBA_39_32	RW	C910 core3 reset entry address upper bits Value After Reset: 0xFF

16.3.3.1.20 C910_TIMER_LINK

- Description: Timer in CPU_SUBSYS configuration register
- Offset: 0x74
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	TIMER1_3_4_LINK	RW	Timer1 counter3 and counter4 link enable Value After Reset: 0x0
[4]	TIMER1_2_3_LINK	RW	Timer1 counter2 and counter3 link enable Value After Reset: 0x0
[3]	TIMER1_1_2_LINK	RW	Timer1 counter1 and counter2 link enable Value After Reset: 0x0
[2]	TIMER0_3_4_LINK	RW	Timer0 counter3 and counter4 link enable Value After Reset: 0x0
[1]	TIMER0_2_3_LINK	RW	Timer0 counter2 and counter3 link enable Value After Reset: 0x0
[0]	TIMER0_1_2_LINK	RW	Timer0 counter1 and counter2 link enable Value After Reset: 0x0

16.3.3.1.21 C910_REE_INT_SRC_0

- Description: C910 REE core software interrupt source 0

- Offset: 0x78
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_C910_REE_SW[0]	RW	C910 REE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 REE cores. Value After Reset: 0x0

16.3.3.1.22 C910_REE_INT_SRC_1

- Description: C910 REE core software interrupt source 1
- Offset: 0x7C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_C910_REE_SW[1]	RW	C910 REE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 REE cores. Value After Reset: 0x0

16.3.3.1.23 C910_REE_INT_SRC_2

- Description: C910 REE core software interrupt source 2
- Offset: 0x80
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_C910_REE_SW[2]	RW	C910 REE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 REE cores. Value After Reset: 0x0

16.3.3.1.24 C910_REE_INT_SRC_3

- Description: C910 REE core software interrupt source 3
- Offset: 0x84
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_C910_REE_SW[3]	RW	C910 REE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 REE cores. Value After Reset: 0x0

16.3.3.1.25 C910_REE_INT_SRC_4

- Description: C910 REE core software interrupt source 4
- Offset: 0x88
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_C910_REE_SW[4]	RW	C910 REE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 REE cores. Value After Reset: 0x0

16.3.3.1.26 C910_REE_INT_SRC_5

- Description: C910 REE core software interrupt source 5
- Offset: 0x8C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_C910_REE_SW[5]	RW	C910 REE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 REE cores. Value After Reset: 0x0

16.3.3.1.27 C910_REE_INT_SRC_6

- Description: C910 REE core software interrupt source 6
- Offset: 0x90
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	

Bits	Field Name	Access	Description
[0]	INT_C910_REE_SW[6]	RW	C910 REE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 REE cores. Value After Reset: 0x0

16.3.3.1.28 C910_REE_INT_SRC_7

- Description: C910 REE core software interrupt source 7
- Offset: 0x94
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_C910_REE_SW[7]	RW	C910 REE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 REE cores. Value After Reset: 0x0

16.3.3.1.29 CPUSYS1_AXI_CFG

- Description: AXI_CPUSYS1 AXI master and slave ports arbitration priority configuration
- Offset: 0xC0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:23]	RESERVED_2	-	
[22:20]	AXI4_CPUSYS1_PRIORITY_S5	RW	Slave arbitration priority associated with slave port 5 (VI_SUBSYS) of AXI_CPUSYS1 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[19:17]	AXI4_CPUSYS1_PRIORITY_S4	RW	Slave arbitration priority associated with slave port 4 (SRAM) of AXI_CPUSYS1 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[16:14]	AXI4_CPUSYS1_PRIORITY_S3	RW	Slave arbitration priority associated with slave port 3 (PERI_SUBSYS) of AXI_CPUSYS1 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[13:11]	AXI4_CPUSYS1_PRIORITY_S2	RW	Slave arbitration priority associated with slave port 2 (CFG_AXI_BUS) of AXI_CPUSYS1 AXI bus in CPU_SUBSYS.

Bits	Field Name	Access	Description
			Larger value represents higher priority. Value After Reset: 0x0
[10:8]	AXI4_CPUSYS1_PRIORITY_S1	RW	Slave arbitration priority associated with slave port 1 (DDR) of AXI_CPUSYS1 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[7:6]	RESERVED_1	-	
[5:4]	AXI4_CPUSYS1_PRIORITY_M3	RW	Master arbitration priority associated with master port 3 (AUD_SUBSYS) of AXI_CPUSYS1 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[3:2]	AXI4_CPUSYS1_PRIORITY_M2	RW	Master arbitration priority associated with master port 2 (AON_SUBSYS/DMA/CHIP_DBG) of AXI_CPUSYS1 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[1:0]	AXI4_CPUSYS1_PRIORITY_M1	RW	Master arbitration priority associated with master port 1 (C910 CPU) of AXI_CPUSYS1 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0

16.3.3.1.30 CPUSYS2_AXI_CFG

- Description: AXI_CPUSYS2 AXI master and slave ports arbitration priority configuration
- Offset: 0xC4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_2	-	
[8]	AXI4_CPUSYS2_PRIORITY_S1	RW	Slave arbitration priority associated with slave port 1 of AXI_CPUSYS2 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[7:6]	RESERVED_1	-	
[5:4]	AXI4_CPUSYS2_PRIORITY_M3	RW	Master arbitration priority associated with master port 3 (AON_SUBSYS) of AXI_CPUSYS2 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0

Bits	Field Name	Access	Description
[3:2]	AXI4_CPUSYS2_PRIORITY_M2	RW	Master arbitration priority associated with master port 2 (DMA) of AXI_CPUSYS2 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[1:0]	AXI4_CPUSYS2_PRIORITY_M1	RW	Master arbitration priority associated with master port 1 (CHIP_DBG) of AXI_CPUSYS2 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0

16.3.3.1.31 CPUSYS_QOS_CFG

- Description: Master QoS identifier register of AXI bus in CPU_SUBSYS
- Offset: 0xC8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	CHIP_DBG_AXI4M_AXI_AWQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at write address channel of CHIP_DBG AXI master port. Value After Reset: 0x0
[27:24]	CHIP_DBG_AXI4M_AXI_ARQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at read address channel of CHIP_DBG AXI master port. Value After Reset: 0x0
[23:20]	C910_AXI4M_AXI_AWQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at write address channel of C910 CPU AXI master port. Value After Reset: 0x0
[19:16]	C910_AXI4M_AXI_ARQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at read address channel of C910 CPU AXI master port. Value After Reset: 0x0
[15:12]	AUD_AXI_AWQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at write address channel of AUD_SUBSYS AXI master port. Value After Reset: 0x0
[11:8]	AUD_AXI_ARQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at read address channel of AUD_SUBSYS AXI master port.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[7:4]	AON_AXI_AWQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at write address channel of AON_SUBSYS AXI master port. Value After Reset: 0x0
[3:0]	AON_AXI_ARQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at read address channel of AON_SUBSYS AXI master port. Value After Reset: 0x0

16.3.3.1.32 PERISYS_SEL_ADDR_L

- Description: GMAC AXI bus address configuration register
- Offset: 0xD0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	PERI_BUS_SEL_ADDR	RW	AXI master bus address upper bits ([39:32]) for GMAC0 and GMAC1. The AXI address bus width of GMAC is 32-bits, this register is used to extend the AXI address bus width to 40-bits. [7:0]: GMAC0 AXI bus upper bits [15:8]: GMAC1 AXI bus upper bits Value After Reset: 0x0

16.3.3.1.33 NPUSYS_AXI_CFG

- Description: NPU2MEM AXI master and slave ports arbitration priority configuration
- Offset: 0xD4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:4]	NPUSYS_AXI_PRIORITY_S2	RW	Slave arbitration priority associated with slave port 2 (SRAM) of NPU2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[3:2]	NPUSYS_AXI_PRIORITY_S1	RW	Slave arbitration priority associated with slave port 1 (DDR) of NPU2MEM AXI bus. Larger value represents

Bits	Field Name	Access	Description
			higher priority. Value After Reset: 0x0
[1]	NPUSYS_AXI_PRIORITY_M2	RW	Master arbitration priority associated with master port 2 (VO_SUBSYS/DSP_SUBSYS) of NPU2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[0]	NPUSYS_AXI_PRIORITY_M1	RW	Master arbitration priority associated with master port 1 (NPU_SUBSYS) of NPU2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0

16.3.3.1.34 AXI4_CFG_BUS_CFG_M

- Description: CFG AXI master ports arbitration priority configuration
- Offset: 0xD8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	AXI4_CFG_BUS_PRIORITY_M1	RW	Master arbitration priority associated with master port 1 (CPU_SUBSYS) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0

16.3.3.1.35 AXI4_CFG_BUS_CFG_S

- Description: CFG AXI slave ports arbitration priority configuration
- Offset: 0xDC
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	AXI4_CFG_BUS_PRIORITY_S8	RW	Slave arbitration priority associated with slave port 2 (SRAM) of NPU2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[27:24]	AXI4_CFG_BUS_PRIORITY_S7	RW	Slave arbitration priority associated with slave port 7 (AUD_SUBSYS) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[23:20]	AXI4_CFG_BUS_PRIORITY_S6	RW	Slave arbitration priority associated with slave port 6

Bits	Field Name	Access	Description
			(MISC_SUBSYS) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[19:16]	AXI4_CFG_BUS_PRIORITY_S5	RW	Slave arbitration priority associated with slave port 5 (VO_SUBSYS) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[15:12]	AXI4_CFG_BUS_PRIORITY_S4	RW	Slave arbitration priority associated with slave port 4 (CLK/RST/SYSREG) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[11:8]	AXI4_CFG_BUS_PRIORITY_S3	RW	Slave arbitration priority associated with slave port 3 (VP_SUBSYS) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[7:4]	AXI4_CFG_BUS_PRIORITY_S2	RW	Slave arbitration priority associated with slave port 2 (NPU_SUBSYS) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[3:0]	AXI4_CFG_BUS_PRIORITY_S1	RW	Slave arbitration priority associated with slave port 1 (CPU_SUBSYS) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0

16.3.3.1.36 AP_BUS_CFG

- Description: Master QoS identifier register of AXI bus in CPU_SUBSYS
- Offset: 0xE0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:4]	SRAM2DSPSYS_AWQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at write address channel of DSP_SUBSYS AXI slave port. Value After Reset: 0x0
[3:0]	SRAM2DSPSYS_ARQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at read address channel of DSP_SUBSYS AXI slave port.

Bits	Field Name	Access	Description
			Value After Reset: 0x0

16.3.3.1.37 VOBUS_AXI_CFG

- Description: CFG AXI master and slave ports arbitration priority configuration
- Offset: 0xE4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:4]	VOSYS_AXI_PRIORITY_S2	RW	Slave arbitration priority associated with slave port 2 (DDR) of VO2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[3:2]	VOSYS_AXI_PRIORITY_S1	RW	Slave arbitration priority associated with slave port 1 (NPU2MEM bus) of VO2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[1]	VOSYS_AXI_PRIORITY_M2	RW	Master arbitration priority associated with master port 1 (DSP_SUBSYS) of VO2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[0]	VOSYS_AXI_PRIORITY_M1	RW	Master arbitration priority associated with master port 1 (VO_SUBSYS) of VO2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0

16.3.3.1.38 QSPI_XIP_CTRL

- Description: SPI XIP support control register
- Offset: 0x134
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	SPI_XIP_EN	RW	SPI XIP enable control. Write 1 to enable the SPI master to behave as a memory mapped I/O and fetch the data from the device based on the APB read request. Value After Reset: 0x0

Bits	Field Name	Access	Description
[1]	QSPI1_XIP_EN	RW	QSPI1 XIP enable control. Write 1 to enable the QSPI1 master to behave as a memory mapped I/O and fetch the data from the device based on the APB read request. Value After Reset: 0x0
[0]	QSPI0_XIP_EN	RW	QSPI0 XIP enable control. Write 1 to enable the QSPI0 master to behave as a memory mapped I/O and fetch the data from the device based on the APB read request. Value After Reset: 0x0

16.3.3.1.39 AP_I2S_CTRL

- Description: I2S configuration and status register
- Offset: 0x138
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	AP_I2S_ERROR	RO	I2S error status bit. This bit indicates FIFO errors or register address errors. Value After Reset: 0x0
[0]	AP_I2S_EN	RW	I2S enable bit. Write 1 to enable the I2S in AP_SUBSYS. Value After Reset: 0x1

16.3.3.1.40 NNA_INT_MASK

- Description: NNA interrupt mask register
- Offset: 0x13c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	INT_IMG_NNA_MASK	RW	NNA interrupt mask bits. Set to mask the interrupt from NNA to AUD_SUBSYS. Value After Reset: 0x0

16.3.3.1.41 BOOT_REG0_TEE

- Description: General purpose register for bootloader
- Offset: 0x1000

- Default Value: 0xff810010

Bits	Field Name	Access	Description
[31:0]	BOOT_REG0	RW	General purpose register for bootloader Value After Reset: 0xFF810010

16.3.3.1.42 BOOT_REG1_TEE

- Description: General purpose register for bootloader
- Offset: 0x1004
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	BOOT_REG1	RW	General purpose register for bootloader Value After Reset: 0x0

16.3.3.1.43 BOOT_REG2_TEE

- Description: General purpose register for bootloader
- Offset: 0x1008
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	BOOT_REG2	RW	General purpose register for bootloader Value After Reset: 0x0

16.3.3.1.44 BOOT_REG3_TEE

- Description: General purpose register for bootloader
- Offset: 0x100C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	BOOT_REG3	RW	General purpose register for bootloader Value After Reset: 0x0

16.3.3.1.45 BOOT_SEL_TEE

- Description: Boot media selection
- Offset: 0x1010
- Default Value: 0x10

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	BOOT_SEL_UPDT	W1S	bootsel update, write any non-zero value to current register will set this bit, and then will lock input pad to boot_sel[3:0]. Value After Reset: 0x1
[3:0]	BOOT_SEL	RO	BOOT media selection Value After Reset: 0x0

16.3.3.1.46 C910_CTRL0_TEE

- Description: C910 CPU system control
- Offset: 0x1014
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	C910_COUNTER_CLR	RW	C910 CPU timer counter clear Value After Reset: 0x0
[3:1]	C910_CORE_ASYNC_MODE	RW	Set C910 core1/2/3 and bus in asynchronous mode. One bit represents one core. 1: core[i] and bus are in asynchronous mode. 0: core[i] and bus are in synchronous mode. Value After Reset: 0x0
[0]	C910_CORE0_ASYNC_MODE	RO	Set C910 core0 and bus in asynchronous mode. 1: core0 and bus are in asynchronous mode. 0: core0 and bus are in synchronous mode. Value After Reset: 0x0

16.3.3.1.47 SOC_VER_TEE

- Description: SoC chip version register
- Offset: 0x1020
- Default Value: 0x10001018

Bits	Field Name	Access	Description
[31:28]	ID_VER	RO	Current ID register version. Different ID version has different register field definition. Value After Reset: 0x1

Bits	Field Name	Access	Description
[27:24]	SOC_IMPL	RO	SoC implementation form. 0x0 for ASIC. Value After Reset: 0x0
[23:16]	RESERVED_1	-	
[15:6]	SOC_ID	RO	SoC ID, different project has a different ID. Value After Reset: 0x40
[5:0]	RELEASE_VER	RO	Release version Value After Reset: 0x18

16.3.3.1.48 SW_REG0_TEE

- Description: General purpose register for software use
- Offset: 0x1040
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG0	RW	General purpose register for software use Value After Reset: 0x0

16.3.3.1.49 SW_REG1_TEE

- Description: General purpose register for software use
- Offset: 0x1044
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG1	RW	General purpose register for software use Value After Reset: 0x0

16.3.3.1.50 SW_REG2_TEE

- Description: General purpose register for software use
- Offset: 0x1048
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG2	RW	General purpose register for software use Value After Reset: 0x0

16.3.3.1.51 SW_REG3_TEE

- Description: General purpose register for software use
- Offset: 0x104C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG3	RW	General purpose register for software use Value After Reset: 0x0

16.3.3.1.52 C910_CORE0_RVBA_L_TEE

- Description: C910 core0 reset entry address lower bits
- Offset: 0x1050
- Default Value: 0xffd00000

Bits	Field Name	Access	Description
[31:0]	C910_CORE0_RVBA_31_0	RW	C910 core0 reset entry address lower bits Value After Reset: 0xFFD00000

16.3.3.1.53 C910_CORE0_RVBA_H_TEE

- Description: C910 core0 reset entry address upper bits
- Offset: 0x1054
- Default Value: 0xff

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	C910_CORE0_RVBA_39_32	RW	C910 core0 reset entry address upper bits Value After Reset: 0xFF

16.3.3.1.54 C910_CORE1_RVBA_L_TEE

- Description: C910 core1 reset entry address lower bits
- Offset: 0x1058
- Default Value: 0xffd00000

Bits	Field Name	Access	Description
[31:0]	C910_CORE1_RVBA_31_0	RW	C910 core1 reset entry address lower bits Value After Reset: 0xFFD00000

16.3.3.1.55 C910_CORE1_RVBA_H_TEE

- Description: C910 core1 reset entry address upper bits

- Offset: 0x105C
- Default Value: 0xff

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	C910_CORE1_RVBA_39_32	RW	C910 core1 reset entry address upper bits Value After Reset: 0xFF

16.3.3.1.56 C910_CORE2_RVBA_L_TEE

- Description: C910 core2 reset entry address lower bits
- Offset: 0x1060
- Default Value: 0xffd00000

Bits	Field Name	Access	Description
[31:0]	C910_CORE2_RVBA_31_0	RW	C910 core2 reset entry address lower bits Value After Reset: 0xFFD00000

16.3.3.1.57 C910_CORE2_RVBA_H_TEE

- Description: C910 core2 reset entry address upper bits
- Offset: 0x1064
- Default Value: 0xff

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	C910_CORE2_RVBA_39_32	RW	C910 core2 reset entry address upper bits Value After Reset: 0xFF

16.3.3.1.58 C910_CORE3_RVBA_L_TEE

- Description: C910 core3 reset entry address lower bits
- Offset: 0x1068
- Default Value: 0xffd00000

Bits	Field Name	Access	Description
[31:0]	C910_CORE3_RVBA_31_0	RW	C910 core3 reset entry address lower bits Value After Reset: 0xFFD00000

16.3.3.1.59 C910_CORE3_RVBA_H_TEE

- Description: C910 core3 reset entry address upper bits
- Offset: 0x106C

- Default Value: 0xff

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	C910_CORE3_RVBA_39_32	RW	C910 core3 reset entry address upper bits Value After Reset: 0xFF

16.3.3.1.60 C910_TIMER_LINK_TEE

- Description: Timer in CPU_SUBSYS configuration register
- Offset: 0x1074
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	TIMER1_3_4_LINK	RW	Timer1 counter3 and counter4 link enable Value After Reset: 0x0
[4]	TIMER1_2_3_LINK	RW	Timer1 counter2 and counter3 link enable Value After Reset: 0x0
[3]	TIMER1_1_2_LINK	RW	Timer1 counter1 and counter2 link enable Value After Reset: 0x0
[2]	TIMER0_3_4_LINK	RW	Timer0 counter3 and counter4 link enable Value After Reset: 0x0
[1]	TIMER0_2_3_LINK	RW	Timer0 counter2 and counter3 link enable Value After Reset: 0x0
[0]	TIMER0_1_2_LINK	RW	Timer0 counter1 and counter2 link enable Value After Reset: 0x0

16.3.3.1.61 C910_REE_INT_SRC_0_TEE

- Description: C910 TEE core software interrupt source 0
- Offset: 0x1078
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_C910_TEE_SW[0]	RW	C910 TEE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 TEE cores.

Bits	Field Name	Access	Description
			Value After Reset: 0x0

16.3.3.1.62 C910_REE_INT_SRC_1_TEE

- Description: C910 TEE core software interrupt source 1
- Offset: 0x107C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_C910_TEE_SW[1]	RW	C910 TEE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 TEE cores. Value After Reset: 0x0

16.3.3.1.63 C910_REE_INT_SRC_2_TEE

- Description: C910 TEE core software interrupt source 2
- Offset: 0x1080
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_C910_TEE_SW[2]	RW	C910 TEE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 TEE cores. Value After Reset: 0x0

16.3.3.1.64 C910_REE_INT_SRC_3_TEE

- Description: C910 TEE core software interrupt source 3
- Offset: 0x1084
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_C910_TEE_SW[3]	RW	C910 TEE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 TEE cores. Value After Reset: 0x0

16.3.3.1.65 C910_REE_INT_SRC_4_TEE

- Description: C910 TEE core software interrupt source 4
- Offset: 0x1088
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_C910_TEE_SW[4]	RW	C910 TEE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 TEE cores. Value After Reset: 0x0

16.3.3.1.66 C910_REE_INT_SRC_5_TEE

- Description: C910 TEE core software interrupt source 5
- Offset: 0x108C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_C910_TEE_SW[5]	RW	C910 TEE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 TEE cores. Value After Reset: 0x0

16.3.3.1.67 C910_REE_INT_SRC_6_TEE

- Description: C910 TEE core software interrupt source 6
- Offset: 0x1090
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_C910_TEE_SW[6]	RW	C910 TEE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 TEE cores. Value After Reset: 0x0

16.3.3.1.68 C910_REE_INT_SRC_7_TEE

- Description: C910 TEE core software interrupt source 7
- Offset: 0x1094

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_C910_TEE_SW[7]	RW	C910 TEE core software interrupt source. Write 1 to this bit will generate an external interrupt request to C910 TEE cores. Value After Reset: 0x0

16.3.3.1.69 CPUSYS1_AXI_CFG_TEE

- Description: AXI_CPUSYS1 AXI master and slave ports arbitration priority configuration
- Offset: 0x10C0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:23]	RESERVED_2	-	
[22:20]	AXI4_CPUSYS1_PRIORITY_S5	RW	Slave arbitration priority associated with slave port 5 (VI_SUBSYS) of AXI_CPUSYS1 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[19:17]	AXI4_CPUSYS1_PRIORITY_S4	RW	Slave arbitration priority associated with slave port 4 (SRAM) of AXI_CPUSYS1 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[16:14]	AXI4_CPUSYS1_PRIORITY_S3	RW	Slave arbitration priority associated with slave port 3 (PERI_SUBSYS) of AXI_CPUSYS1 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[13:11]	AXI4_CPUSYS1_PRIORITY_S2	RW	Slave arbitration priority associated with slave port 2 (CFG_AXI_BUS) of AXI_CPUSYS1 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[10:8]	AXI4_CPUSYS1_PRIORITY_S1	RW	Slave arbitration priority associated with slave port 1 (DDR) of AXI_CPUSYS1 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[7:6]	RESERVED_1	-	
[5:4]	AXI4_CPUSYS1_PRIORITY_M3	RW	Master arbitration priority associated with master port 3 (AUD_SUBSYS) of AXI_CPUSYS1 AXI bus in

Bits	Field Name	Access	Description
			CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[3:2]	AXI4_CPUSYS1_PRIORITY_M2	RW	Master arbitration priority associated with master port 2 (AON_SUBSYS/DMA/CHIP_DBG) of AXI_CPUSYS1 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[1:0]	AXI4_CPUSYS1_PRIORITY_M1	RW	Master arbitration priority associated with master port 1 (C910 CPU) of AXI_CPUSYS1 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0

16.3.3.1.70 CPUSYS2_AXI_CFG_TEE

- Description: AXI_CPUSYS2 AXI master and slave ports arbitration priority configuration
- Offset: 0x10C4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_2	-	
[8]	AXI4_CPUSYS2_PRIORITY_S1	RW	Slave arbitration priority associated with slave port 1 of AXI_CPUSYS2 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[7:6]	RESERVED_1	-	
[5:4]	AXI4_CPUSYS2_PRIORITY_M3	RW	Master arbitration priority associated with master port 3 (AON_SUBSYS) of AXI_CPUSYS2 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[3:2]	AXI4_CPUSYS2_PRIORITY_M2	RW	Master arbitration priority associated with master port 2 (DMA) of AXI_CPUSYS2 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[1:0]	AXI4_CPUSYS2_PRIORITY_M1	RW	Master arbitration priority associated with master port 1 (CHIP_DBG) of AXI_CPUSYS2 AXI bus in CPU_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0

16.3.3.1.71 CPUSYS_QOS_CFG_TEE

- Description: Master QoS identifier register of AXI bus in CPU_SUBSYS
- Offset: 0x10C8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	CHIP_DBG_AXI4M_AXI_AWQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at write address channel of CHIP_DBG AXI master port. Value After Reset: 0x0
[27:24]	CHIP_DBG_AXI4M_AXI_ARQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at read address channel of CHIP_DBG AXI master port. Value After Reset: 0x0
[23:20]	C910_AXI4M_AXI_AWQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at write address channel of C910 CPU AXI master port. Value After Reset: 0x0
[19:16]	C910_AXI4M_AXI_ARQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at read address channel of C910 CPU AXI master port. Value After Reset: 0x0
[15:12]	AUD_AXI_AWQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at write address channel of AUD_SUBSYS AXI master port. Value After Reset: 0x0
[11:8]	AUD_AXI_ARQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at read address channel of AUD_SUBSYS AXI master port. Value After Reset: 0x0
[7:4]	AON_AXI_AWQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at write address channel of AON_SUBSYS AXI master port. Value After Reset: 0x0
[3:0]	AON_AXI_ARQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at read address channel of AON_SUBSYS AXI master port. Value After Reset: 0x0

16.3.3.1.72 PERISYS_SEL_ADDR_L_TEE

- Description: GMAC AXI bus address configuration register
- Offset: 0x10D0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	PERI_BUS_SEL_ADDR	RW	AXI master bus address upper bits ([39:32]) for GMAC0 and GMAC1. The AXI address bus width of GMAC is 32-bits, this register is used to extend the AXI address bus width to 40-bits. [7:0]: GMAC0 AXI bus upper bits [15:8]: GMAC1 AXI bus upper bits Value After Reset: 0x0

16.3.3.1.73 NPUSYS_AXI_CFG_TEE

- Description: NPU2MEM AXI master and slave ports arbitration priority configuration
- Offset: 0x10D4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:4]	NPUSYS_AXI_PRIORITY_S2	RW	Slave arbitration priority associated with slave port 2 (SRAM) of NPU2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[3:2]	NPUSYS_AXI_PRIORITY_S1	RW	Slave arbitration priority associated with slave port 1 (DDR) of NPU2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[1]	NPUSYS_AXI_PRIORITY_M2	RW	Master arbitration priority associated with master port 2 (VO_SUBSYS/DSP_SUBSYS) of NPU2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[0]	NPUSYS_AXI_PRIORITY_M1	RW	Master arbitration priority associated with master port 1 (NPU_SUBSYS) of NPU2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0

16.3.3.1.74 AXI4_CFG_BUS_CFG_M_TEE

- Description: CFG AXI master ports arbitration priority configuration
- Offset: 0x10D8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	AXI4_CFG_BUS_PRIORITY_M1	RW	Master arbitration priority associated with master port 1 (CPU_SUBSYS) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0

16.3.3.1.75 AXI4_CFG_BUS_CFG_S_TEE

- Description: CFG AXI slave ports arbitration priority configuration
- Offset: 0x10DC
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	AXI4_CFG_BUS_PRIORITY_S8	RW	Slave arbitration priority associated with slave port 2 (SRAM) of NPU2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[27:24]	AXI4_CFG_BUS_PRIORITY_S7	RW	Slave arbitration priority associated with slave port 7 (AUD_SUBSYS) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[23:20]	AXI4_CFG_BUS_PRIORITY_S6	RW	Slave arbitration priority associated with slave port 6 (MISC_SUBSYS) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[19:16]	AXI4_CFG_BUS_PRIORITY_S5	RW	Slave arbitration priority associated with slave port 5 (VO_SUBSYS) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[15:12]	AXI4_CFG_BUS_PRIORITY_S4	RW	Slave arbitration priority associated with slave port 4 (CLK/RST/SYSREG) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[11:8]	AXI4_CFG_BUS_PRIORITY_S3	RW	Slave arbitration priority associated with slave port 3

Bits	Field Name	Access	Description
			(VP_SUBSYS) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[7:4]	AXI4_CFG_BUS_PRIORITY_S2	RW	Slave arbitration priority associated with slave port 2 (NPU_SUBSYS) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[3:0]	AXI4_CFG_BUS_PRIORITY_S1	RW	Slave arbitration priority associated with slave port 1 (CPU_SUBSYS) of CFG AXI bus. Larger value represents higher priority. Value After Reset: 0x0

16.3.3.1.76 AP_BUS_CFG_TEE

- Description: Master QoS identifier register of AXI bus in CPU_SUBSYS
- Offset: 0x10E0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:4]	SRAM2DSPSYS_AWQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at write address channel of DSP_SUBSYS AXI slave port. Value After Reset: 0x0
[3:0]	SRAM2DSPSYS_ARQOS	RW	Master QoS identifier, conveying priority information associated with each transaction at read address channel of DSP_SUBSYS AXI slave port. Value After Reset: 0x0

16.3.3.1.77 VOBUS_AXI_CFG_TEE

- Description: CFG AXI master and slave ports arbitration priority configuration
- Offset: 0x10E4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:4]	VOSYS_AXI_PRIORITY_S2	RW	Slave arbitration priority associated with slave port 2 (DDR) of VO2MEM AXI bus. Larger value represents higher priority.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[3:2]	VOSYS_AXI_PRIORITY_S1	RW	Slave arbitration priority associated with slave port 1 (NPU2MEM bus) of VO2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[1]	VOSYS_AXI_PRIORITY_M2	RW	Master arbitration priority associated with master port 1 (DSP_SUBSYS) of VO2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0
[0]	VOSYS_AXI_PRIORITY_M1	RW	Master arbitration priority associated with master port 1 (VO_SUBSYS) of VO2MEM AXI bus. Larger value represents higher priority. Value After Reset: 0x0

16.3.3.1.78 QSPI_XIP_CTRL_TEE

- Description: SPI XIP support control register
- Offset: 0x1134
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	SPI_XIP_EN	RW	SPI XIP enable control. Write 1 to enable the SPI master to behave as a memory mapped I/O and fetch the data from the device based on the APB read request. Value After Reset: 0x0
[1]	QSPI1_XIP_EN	RW	QSPI1 XIP enable control. Write 1 to enable the QSPI1 master to behave as a memory mapped I/O and fetch the data from the device based on the APB read request. Value After Reset: 0x0
[0]	QSPI0_XIP_EN	RW	QSPI0 XIP enable control. Write 1 to enable the QSPI0 master to behave as a memory mapped I/O and fetch the data from the device based on the APB read request. Value After Reset: 0x0

16.3.3.1.79 AP_I2S_CTRL_TEE

- Description: I2S configuration and status register

- Offset: 0x1138
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	AP_I2S_ERROR	RO	I2S error status bit. This bit indicates FIFO errors or register address errors. Value After Reset: 0x0
[0]	AP_I2S_EN	RW	I2S enable bit. Write 1 to enable the I2S in AP_SUBSYS. Value After Reset: 0x1

16.3.3.1.80 NNA_INT_MASK_TEE

- Description: NNA interrupt mask register
- Offset: 0x113C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	INT_IMG_NNA_MASK	RW	NNA interrupt mask bits. Set to mask the interrupt from NNA to AUD_SUBSYS. Value After Reset: 0x0

16.3.3.1.81 SYSREG_LOCK_0

- Description: REE region registers' lock control register
- Offset: 0x1800
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:19]	RESERVED_1	-	
[18]	NNA_INT_MASK_LOCK	RW	Write lock bit for NNA interrupt mask register. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[17]	AP_I2S_CTRL_LOCK	RW	Write lock bit for I2S configuration register. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[16]	QSPI_XIP_CTRL_LOCK	RW	Write lock bit for QSPI/SPI XIP configuration register. Write 1 to this bit to disable the write authority of REE region.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[15]	VOBUS_AXI_CFG_LOCK	RW	Write lock bit for VO2MEM AXI bus configuration register. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[14]	AP_QOS_CFG_LOCK	RW	Write lock bit for WRAM2DSP AXI bus QoS configuration register. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[13]	AXI4_CFG_BUS_CFG_S_LOCK	RW	Write lock bit for CFG AXI bus slave configuration register. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[12]	AXI4_CFG_BUS_CFG_M_LOCK	RW	Write lock bit for CFG AXI bus master configuration register. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[11]	NPUSYS_AXI_CFG_LOCK	RW	Write lock bit for NPU2MEM AXI bus configuration register. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[10]	PERISYS_SEL_ADDR_LOCK	RW	Write lock bit for GMAC AXI bus configuration register. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[9]	CPUSYS_QOS_CFG_LOCK	RW	Write lock bit for CPU_SUBSYS AXI bus configuration register. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[8]	CPUSYS2_AXI_CFG_LOCK	RW	Write lock bit for AXI_CPUSYS2 AXI bus configuration register. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[7]	CPUSYS1_AXI_CFG_LOCK	RW	Write lock bit for AXI_CPUSYS1 AXI bus configuration register. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0

Bits	Field Name	Access	Description
[6]	C910_TIMER_LINK_LOCK	RW	Write lock bit for timer configuration register. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[5]	C910_REE_INT_SRC_LOCK	RW	Write lock bit for C910 REE core software interrupt source registers. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[4]	C910_RVBA_LOCK	RW	Write lock bit for C910 CPU reset entry address registers. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[3]	SW_REG_LOCK	RW	Write lock bit for general purpose registers for software use. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[2]	C910_CTRL0_LOCK	RW	Write lock bit for C910 CPU system control register. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[1]	BOOT_SEL_LOCK	RW	Write lock bit for boot media selection register. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0
[0]	BOOT_REG_LOCK	RW	Write lock bit for general purpose registers for bootloader. Write 1 to this bit to disable the write authority of REE region. Value After Reset: 0x0

16.3.3.2 AON_SUBSYS Control Registers

16.3.3.2.1 CPU_LP_MODE

- Description: CPU low power mode register
- Offset: 0x00
- Default Value: 0x3ff

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9:8]	C906_CORE_LPMD_B	RO	C906 low power mode register

Bits	Field Name	Access	Description
			00/01/10: Low power mode 11: Normal mode Value After Reset: 0x3
[7:6]	C910_CORE3_LPMD_B	RO	C910 core3 low power mode register 00/01/10: Low power mode 11: Normal mode Value After Reset: 0x3
[5:4]	C910_CORE2_LPMD_B	RO	C910 core2 low power mode register 00/01/10: Low power mode 11: Normal mode Value After Reset: 0x3
[3:2]	C910_CORE1_LPMD_B	RO	C910 core1 low power mode register 00/01/10: Low power mode 11: Normal mode Value After Reset: 0x3
[1:0]	C910_CORE0_LPMD_B	RO	C910 core0 low power mode register 00/01/10: Low power mode 11: Normal mode Value After Reset: 0x3

16.3.3.2.2 CHIP_LP_MODE

- Description: SoC low power mode register
- Offset: 0x04
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	CHIP_LP_MODE	RW	SoC low power mode register, used by software to mark the user defined low power state of the chip. Value After Reset: 0x0

16.3.3.2.3 AO_SERAM_TRN

- Description: AO_SERAM scrambler register
- Offset: 0x10
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	AO_SERAM_TRN	RW	AO_SERAM scrambling key Value After Reset: 0x0

16.3.3.2.4 AO_SERAM_INT

- Description: AO_SRAM interrupt register
- Offset: 0x14
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	AO_SRAM_INIT	RW	AO_SERAM interrupt Value After Reset: 0x0

16.3.3.2.5 STR_SERAM_TRN

- Description: STR_SERAM scrambler register
- Offset: 0x18
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	STR_SERAM_TRN	RW	STR_SERAM scrambling key Value After Reset: 0x0

16.3.3.2.6 STR_SERAM_INT

- Description: STR_SRAM interrupt register
- Offset: 0x1c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	STR_SRAM_INIT	RW	STR_SERAM interrupt Value After Reset: 0x0

16.3.3.2.7 STR_INDICATOR_0

- Description: Low power startup marker register 0
- Offset: 0x20
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	STR_INDICATOR_0	RW	Low power start tag Value After Reset: 0x0

16.3.3.2.8 STR_INDICATOR_1

- Description: Low power startup marker register 1
- Offset: 0x24
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	STR_INDICATOR_1	RW	Low power start tag Value After Reset: 0x0

16.3.3.2.9 STR_INDICATOR_2

- Description: Low power startup marker register 2
- Offset: 0x28
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	STR_INDICATOR_2	RW	Low power start tag Value After Reset: 0x0

16.3.3.2.10 STR_INDICATOR_3

- Description: Low power startup marker register 3
- Offset: 0x2c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	STR_INDICATOR_3	RW	Low power start tag Value After Reset: 0x0

16.3.3.2.11 PVTC_WR_LOCK

- Description: PVTC write lock
- Offset: 0x30
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	

Bits	Field Name	Access	Description
[0]	PVTC_WR_LOCK	RW	PVTC write lock Value After Reset: 0x0

16.3.3.2.12 PVTC_TS_ALARM

- Description: Temperature sensor alarm register
- Offset: 0x34
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3:2]	PVTC_TS_ALARMA	RO	Temperature sensor alarm A, active high Value After Reset: 0x0
[1:0]	PVTC_TS_ALARMB	RO	Temperature sensor alarm B, active high Value After Reset: 0x0

16.3.3.2.13 PVTC_VM_ALARM

- Description: Voltage monitor alarm register
- Offset: 0x38
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	PVTC_VM_ALARMA	RO	Voltage monitor alarm A, active high Value After Reset: 0x0
[15:0]	PVTC_VM_ALARMB	RO	Voltage monitor alarm B, active high Value After Reset: 0x0

16.3.3.2.14 PVTC_PD_ALARM

- Description: Process detector alarm register
- Offset: 0x3c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:23]	RESERVED_2	-	
[22:12]	PVTC_PD_ALARMA	RO	Process detector alarm A, active high Value After Reset: 0x0
[11]	RESERVED_1	-	

Bits	Field Name	Access	Description
[10:0]	PVTC_PD_ALARMB	RO	Process detector alarm B, active high Value After Reset: 0x0

16.3.3.2.15 E902_CNT_CLR

- Description: E902 timer counter clear register
- Offset: 0x40
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	E902_CNT_CLR	RW	E902 timer counter clear register, write 1 to clear the counter value of the timer in E902 Value After Reset: 0x0

16.3.3.2.16 E902_RST_ADDR

- Description: E902 reset start address register
- Offset: 0x44
- Default Value: 0xffef8000

Bits	Field Name	Access	Description
[31:0]	E902_CPU_RST_ADDR	RW	E902 reset start address Value After Reset: 0xFFEF8000

16.3.3.2.17 C906_RST_ADDR_L

- Description: C906 reset start address register, lower 32 bits
- Offset: 0x48
- Default Value: 0xc0000000

Bits	Field Name	Access	Description
[31:0]	C906_CPU_RST_ADDR_L	RW	C906 reset start address, lower 32 bits Value After Reset: 0xC0000000

16.3.3.2.18 C906_RST_ADDR_H

- Description: C906 reset start address register, upper 32 bits
- Offset: 0x4c
- Default Value: 0xff

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	C906_CPU_RST_ADDR_H	RW	C906 reset start address, upper 32 bits Value After Reset: 0xFF

16.3.3.2.19 RESERVED_REG_0

- Description: General purpose register
- Offset: 0x50
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_0	RW	General purpose register used by software Value After Reset: 0x0

16.3.3.2.20 RESERVED_REG_1

- Description: General purpose register
- Offset: 0x54
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_1	RW	General purpose register used by software Value After Reset: 0x0

16.3.3.2.21 RESERVED_REG_2

- Description: General purpose register
- Offset: 0x58
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_2	RW	General purpose register used by software Value After Reset: 0x0

16.3.3.2.22 RESERVED_REG_3

- Description: General purpose register
- Offset: 0x5c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_3	RW	General purpose register used by software Value After Reset: 0x0

16.3.3.2.23 AON_AHB_ADEXT

- Description: AON_SUBSYS AHB bus address extension register
- Offset: 0x60
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9:0]	AONSYS_AHB_SPACE_SEL	RW	AON_SUBSYS AHB bus address extension register

16.3.3.2.24 RC_EN

- Description: RC enable control register
- Offset: 0x70
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	RC_EN	RW	Internal RC oscillator enable control 0: Oscillator is powered down. 1: Oscillator is enabled. Value After Reset: 0x1

16.3.3.2.25 RC_FCAL

- Description: RC trim register
- Offset: 0x74
- Default Value: 0x77f

Bits	Field Name	Access	Description
[31:12]	RESERVED_1	-	
[11:0]	RC_FCAL	RW	Trim to set nominal oscillator frequency to adjust for process variations. Provides between a 0.05% (low-end) to 0.02% (high-end) step. Ensures that frequency will remain within ±2% of target over PVT after calibration (MODE==1). Trim can be changed asynchronously. The output frequency will immediately begin to slew to the new

Bits	Field Name	Access	Description
			value when the FCAL value is updated. The upper 4 bits of FCAL are for coarse frequency tuning. The lower 8 bits of FCAL are for fine frequency tuning. Value After Reset: 0x77F

16.3.3.2.26 RC_MODE

- Description: RC mode control register
- Offset: 0x78
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	RC_MODE	RW	RC mode control register 0: Low frequency mode: FOSC = 0.9MHz to 2.0MHz 1: High frequency mode: FOSC = 24MHz to 26MHz Value After Reset: 0x1

16.3.3.2.27 RC_READY

- Description: RC status Register
- Offset: 0x7c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	RC_READY	RO	RC status register 0: Oscillator internal frequency is not settled, output is gated low. 1: Oscillator internal frequency is settled, output is valid. Value After Reset: 0x0

16.3.3.2.28 ISO_CFG

- Description: Isolation cells control register for low power mode
- Offset: 0x80
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	USB3_ISOLATION_EN	RW	USB3 PHY input isolation enable register Value After Reset: 0x0
[2]	DDR_ISOLATION_EN	RW	DDR input isolation enable register Value After Reset: 0x0
[1]	C910_ISOLATION_EN	RW	C910 input isolation enable register Value After Reset: 0x0
[0]	AON_ISOLATION_EN	RW	AON_SUBSYS input isolation enable register Value After Reset: 0x0

16.3.3.2.29 OCRAM_ERR

- Description: OCRAM check error register
- Offset: 0x90
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	INT_SERAM_ERR	RO	OCRAM check error register Value After Reset: 0x0

16.3.3.2.30 TIMER_LINK

- Description: Timer link register
- Offset: 0x100
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	TIMER_3_4_LINK	RW	The timer in AON_SUBSYS counter 3 and counter 4 link control Value After Reset: 0x0
[1]	TIMER_2_3_LINK	RW	The timer in AON_SUBSYS counter 2 and counter 3 link control Value After Reset: 0x0
[0]	TIMER_1_2_LINK	RW	The timer in AON_SUBSYS counter 1 and counter 2 link control

Bits	Field Name	Access	Description
			Value After Reset: 0x0

16.3.3.2.31 PD_REQ

- Description: Power domain power on/off control register
- Offset: 0x110
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:27]	RESERVED_2	-	
[26:16]	PU_REQ	W1S	Power domain power-on request signals, PU_REQ is set by software and auto cleared in the next cycle. [0]: AUDIO [1]: VDEC [2]: NPU [3]: VENC [4]: GPU [5]: DSP0 [6]: DSP1 [7]: C910 CORE0 [8]: C910 CORE1 [9]: C910 CORE2 [10]: C910 CORE3 Value After Reset: 0x0
[15:11]	RESERVED_1	-	
[10:0]	PD_REQ	W1S	Power domain power-off request signals, PD_REQ is set by software and auto cleared in the next cycle. [0]: AUDIO [1]: VDEC [2]: NPU [3]: VENC [4]: GPU [5]: DSP0 [6]: DSP1 [7]: C910 CORE0 [8]: C910 CORE1 [9]: C910 CORE2

Bits	Field Name	Access	Description
			[10]: C910 CORE3 Value After Reset: 0x0

16.3.3.2.32 PD_ISO_EN_SET

- Description: Power domain isolation cells enable control register
- Offset: 0x114
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:0]	PD_ISO_EN_SET	W1S	Power domain isolation cells enable request signals, PD_ISO_EN_SET is set by software and auto cleared in the next cycle. [0]: AUDIO [1]: VDEC [2]: NPU [3]: VENC [4]: GPU [5]: DSP0 [6]: DSP1 [7]: C910 CORE0 [8]: C910 CORE1 [9]: C910 CORE2 [10]: C910 CORE3 Value After Reset: 0x0

16.3.3.2.33 PD_ISO_EN_CLR

- Description: Power domain isolation cells disable control register
- Offset: 0x118
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:0]	PD_ISO_EN_CLR	W1S	Power domain isolation cells disable request signals, PD_ISO_EN_SET is set by software and auto cleared in the next cycle. [0]: AUDIO

Bits	Field Name	Access	Description
			[1]: VDEC [2]: NPU [3]: VENC [4]: GPU [5]: DSP0 [6]: DSP1 [7]: C910 CORE0 [8]: C910 CORE1 [9]: C910 CORE2 [10]: C910 CORE3 Value After Reset: 0x0

16.3.3.2.34 PD_SW_EN_SET

- Description: Power domain power switch cells off control register. Used for low power control in software mode.
- Offset: 0x11c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:22]	RESERVED_1	-	
[21:0]	PD_SW_EN_SET	W1S	Power domain power switch cells off control signals, each power domain needs 2-bits. PD_SW_EN_SET is set by software only when 2'b11 is written, and auto cleared in the next cycle. [1:0]: AUDIO [3:2]: VDEC [5:4]: NPU [7:6]: VENC [9:8]: GPU [11:10]: DSP0 [13:12]: DSP1 [15:14]: C910 CORE0 [17:16]: C910 CORE1 [19:18]: C910 CORE2 [21:20]: C910 CORE3 Value After Reset: 0x0

16.3.3.2.35 PD_SW_EN_CLR

- Description: Power domain power switch cells on control register. Used for low power control in software mode.
- Offset: 0x120
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:22]	RESERVED_1	-	
[21:0]	PD_SW_EN_CLR	W1S	Power domain power switch cells on control signals, each power domain needs 2-bits. PD_SW_EN_CLR is set by software only when 2'b11 is written, and auto cleared in the next cycle. [1:0]: AUDIO [3:2]: VDEC [5:4]: NPU [7:6]: VENC [9:8]: GPU [11:10]: DSP0 [13:12]: DSP1 [15:14]: C910 CORE0 [17:16]: C910 CORE1 [19:18]: C910 CORE2 [21:20]: C910 CORE3 Value After Reset: 0x0

16.3.3.2.36 PD_SW_ACK

- Description: Power domain power switch cells acknowledgement register
- Offset: 0x124
- Default Value: 0x3fffff

Bits	Field Name	Access	Description
[31:22]	RESERVED_1	-	
[21:0]	PD_SW_ACK	RO	Power domain power switch cells on/off feedback status, every 2bits represent one power domain. 2'b00: power off state; 2'b11: power on state [1:0]: AUDIO [3:2]: VDEC [5:4]: NPU

Bits	Field Name	Access	Description
			[7:6]: VENC [9:8]: GPU [11:10]: DSP0 [13:12]: DSP1 [15:14]: C910 CORE0 [17:16]: C910 CORE1 [19:18]: C910 CORE2 [21:20]: C910 CORE3 Value After Reset: 0x3FFFFF

16.3.3.2.37 PD_SW_CNT_EN

- Description: Power domain power on/off feedback wait time control register, used in low power control hardware mode.
- Offset: 0x128
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:22]	RESERVED_1	-	
[21:0]	PD_SW_CNT_EN	RW	Power domain power on/off feedback wait counter enable signals. Every 2bits represent one power domain. The PD_SW_CNT_EN is used only in low power control hardware mode. If PD_SW_CNT_EN is set, PMU will ignore the feedback signal from power switch and use the overflow signal of internal counter. [1:0]: AUDIO [3:2]: VDEC [5:4]: NPU [7:6]: VENC [9:8]: GPU [11:10]: DSP0 [13:12]: DSP1 [15:14]: C910 CORE0 [17:16]: C910 CORE1 [19:18]: C910 CORE2 [21:20]: C910 CORE3 Value After Reset: 0x0

16.3.3.2.38 PD_FSM_RST

- Description: Reset control register for all PMUs in every power domain
- Offset: 0x12c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:0]	PD_FSM_RST	W1S	PMU state machine reset signal. Write 1 to reset the PMU, and auto cleared in next cycle. [0]: AUDIO [1]: VDEC [2]: NPU [3]: VENC [4]: GPU [5]: DSP0 [6]: DSP1 [7]: C910 CORE0 [8]: C910 CORE1 [9]: C910 CORE2 [10]: C910 CORE3 Value After Reset: 0x0

16.3.3.2.39 PD_INT_MASK

- Description: PMU interrupt mask control register
- Offset: 0x130
- Default Value: 0x3fffff

Bits	Field Name	Access	Description
[31:22]	RESERVED_1	-	
[21:0]	PD_INT_MASK	RW	PMU interrupt mask signals for every power domain 0: Unmasked 1: Masked [1:0]: AUDIO [3:2]: VDEC [5:4]: NPU [7:6]: VENC [9:8]: GPU

Bits	Field Name	Access	Description
			[11:10]: DSP0 [13:12]: DSP1 [15:14]: C910 CORE0 [17:16]: C910 CORE1 [19:18]: C910 CORE2 [21:20]: C910 CORE3 Value After Reset: 0x3FFFFF

16.3.3.2.40 PD_FSM_STS_L

- Description: PMU FSM status register of every power domain
- Offset: 0x134
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PD_FSM_ST_L	RO	FSM state in PMU of every power domain [3:0]: AUDIO [7:4]: VDEC [11:8]: NPU [15:12]: VENC [19:16]: GPU [23:20]: DSP0 [27:24]: DSP1 [31:28]: C910 CORE0 Value After Reset: 0x0

16.3.3.2.41 PD_FSM_STS_H

- Description: PMU FSM status register of every power domain
- Offset: 0x138
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:12]	RESERVED_1	-	
[11:0]	PD_FSM_ST_H	RO	FSM state in PMU of every power domain [3:0]: C910 CORE1 [7:4]: C910 CORE2 [11:8]: C910 CORE3

Bits	Field Name	Access	Description
			Value After Reset: 0x0

16.3.3.2.42 PD_INT_STS

- Description: PMU interrupt status register
- Offset: 0x13c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:22]	RESERVED_1	-	
[21:0]	PD_INT_ST	RO	PMU interrupt status signals for every power domain [1:0]: AUDIO [3:2]: VDEC [5:4]: NPU [7:6]: VENC [9:8]: GPU [11:10]: DSP0 [13:12]: DSP1 [15:14]: C910 CORE0 [17:16]: C910 CORE1 [19:18]: C910 CORE2 [21:20]: C910 CORE3 Value After Reset: 0x0

16.3.3.2.43 PD_INT_CLR

- Description: PMU interrupt clear register
- Offset: 0x140
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:22]	RESERVED_1	-	
[21:0]	PD_INT_CLR	RW	PMU interrupt clear signals for every power domain [1:0]: AUDIO [3:2]: VDEC [5:4]: NPU [7:6]: VENC [9:8]: GPU

Bits	Field Name	Access	Description
			[11:10]: DSP0 [13:12]: DSP1 [15:14]: C910 CORE0 [17:16]: C910 CORE1 [19:18]: C910 CORE2 [21:20]: C910 CORE3 Value After Reset: 0x0

16.3.3.2.44 PD_BLK0_SW_CNT

- Description: AUDIO_SUBSYS power domain power on/off feedback wait time counter register
- Offset: 0x144
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_0	RW	AUDIO_SUBSYS power domain power on/off phase 2 feedback wait counter register, enabled when PD_SW_CNT_EN[1] is set. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_0	RW	AUDIO_SUBSYS power domain power on/off phase 1 feedback wait counter register, enabled when PD_SW_CNT_EN[0] is set. Value After Reset: 0xFF

16.3.3.2.45 PD_BLK1_SW_CNT

- Description: VDEC power domain power on/off feedback wait time counter register
- Offset: 0x148
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_1	RW	VDEC power domain power on/off phase 2 feedback wait counter register, enabled when PD_SW_CNT_EN[3] is set. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_1	RW	VDEC power domain power on/off phase 1 feedback wait counter register, enabled when PD_SW_CNT_EN[2] is set. Value After Reset: 0xFF

16.3.3.2.46 PD_BLK2_SW_CNT

- Description: NPU power domain power on/off feedback wait time counter register
- Offset: 0x14c
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_2	RW	NPU power domain power on/off phase 2 feedback wait counter register, enabled when PD_SW_CNT_EN[5] is set. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_2	RW	NPU power domain power on/off phase 1 feedback wait counter register, enabled when PD_SW_CNT_EN[4] is set. Value After Reset: 0xFF

16.3.3.2.47 PD_BLK3_SW_CNT

- Description: VENC power domain power on/off feedback wait time counter register
- Offset: 0x150
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_3	RW	VENC power domain power on/off phase 2 feedback wait counter register, enabled when PD_SW_CNT_EN[7] is set. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_3	RW	VENC power domain power on/off phase 1 feedback wait counter register, enabled when PD_SW_CNT_EN[6] is set. Value After Reset: 0xFF

16.3.3.2.48 PD_BLK4_SW_CNT

- Description: GPU power domain power on/off feedback wait time counter register
- Offset: 0x154
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_4	RW	GPU power domain power on/off phase 2 feedback wait counter register, enabled when PD_SW_CNT_EN[9] is set. Value After Reset: 0xFF

Bits	Field Name	Access	Description
[15:0]	SW0_WAIT_CNT_4	RW	GPU power domain power on/off phase 1 feedback wait counter register, enabled when PD_SW_CNT_EN[8] is set. Value After Reset: 0xFF

16.3.3.2.49 PD_BLK5_SW_CNT

- Description: DSP0 power domain power on/off feedback wait time counter register
- Offset: 0x158
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_5	RW	DSP0 power domain power on/off phase 2 feedback wait counter register, enabled when PD_SW_CNT_EN[11] is set. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_5	RW	DSP0 power domain power on/off phase 1 feedback wait counter register, enabled when PD_SW_CNT_EN[10] is set. Value After Reset: 0xFF

16.3.3.2.50 PD_BLK6_SW_CNT

- Description: DSP1 power domain power on/off feedback wait time counter register
- Offset: 0x15c
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_6	RW	DSP1 power domain power on/off phase 2 feedback wait counter register, enabled when PD_SW_CNT_EN[13] is set. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_6	RW	DSP1 power domain power on/off phase 1 feedback wait counter register, enabled when PD_SW_CNT_EN[12] is set. Value After Reset: 0xFF

16.3.3.2.51 PD_BLK7_SW_CNT

- Description: C910 core0 power domain power on/off feedback wait time counter register
- Offset: 0x160
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_7	RW	C910 core0 power domain power on/off phase 2 feedback wait counter register, enabled when PD_SW_CNT_EN[15] is set. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_7	RW	C910 core0 power domain power on/off phase 1 feedback wait counter register, enabled when PD_SW_CNT_EN[14] is set. Value After Reset: 0xFF

16.3.3.2.52 PD_BLK8_SW_CNT

- Description: C910 core1 power domain power on/off feedback wait time counter register
- Offset: 0x164
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_8	RW	C910 core1 power domain power on/off phase 2 feedback wait counter register, enabled when PD_SW_CNT_EN[17] is set. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_8	RW	C910 core1 power domain power on/off phase 1 feedback wait counter register, enabled when PD_SW_CNT_EN[16] is set. Value After Reset: 0xFF

16.3.3.2.53 PD_BLK9_SW_CNT

- Description: C910 core2 power domain power on/off feedback wait time counter register
- Offset: 0x168
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_9	RW	C910 core2 power domain power on/off phase 2 feedback wait counter register, enabled when PD_SW_CNT_EN[19] is set. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_9	RW	C910 core2 power domain power on/off phase 1 feedback wait counter register, enabled when PD_SW_CNT_EN[18] is set. Value After Reset: 0xFF

16.3.3.2.54 PD_BLK10_SW_CNT

- Description: C910 core3 power domain power on/off feedback wait time counter register
- Offset: 0x16c
- Default Value: 0xff00ff

Bits	Field Name	Access	Description
[31:16]	SW1_WAIT_CNT_10	RW	C910 core3 power domain power on/off phase 2 feedback wait counter register, enabled when PD_SW_CNT_EN[21] is set. Value After Reset: 0xFF
[15:0]	SW0_WAIT_CNT_10	RW	C910 core3 power domain power on/off phase 1 feedback wait counter register, enabled when PD_SW_CNT_EN[20] is set. Value After Reset: 0xFF

16.3.3.2.55 PD_BLK0_INTV_CNT

- Description: AUDIO_SUBSYS PMU state transition wait time counter register
- Offset: 0x180
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_0	RW	AUDIO_SUBSYS low power transition time counter between isolation cells releasing and clock enabling Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_0	RW	AUDIO_SUBSYS low power transition time counter between isolation cells enabling and power on/off Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_0	RW	AUDIO_SUBSYS low power transition time counter between power on/off phase 1 and phase 2 Value After Reset: 0xFF

16.3.3.2.56 PD_BLK1_INTV_CNT

- Description: VDEC PMU state transition wait time counter register
- Offset: 0x184
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_1	RW	VDEC low power transition time counter between isolation cells releasing and clock enabling

Bits	Field Name	Access	Description
			Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_1	RW	VDEC low power transition time counter between isolation cells enabling and power on/off Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_1	RW	VDEC low power transition time counter between power on/off phase 1 and phase 2 Value After Reset: 0xFF

16.3.3.2.57 PD_BLK2_INTV_CNT

- Description: NPU PMU state transition wait time counter register
- Offset: 0x188
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_2	RW	NPU low power transition time counter between isolation cells releasing and clock enabling Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_2	RW	NPU low power transition time counter between isolation cells enabling and power on/off Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_2	RW	NPU low power transition time counter between power on/off phase 1 and phase 2 Value After Reset: 0xFF

16.3.3.2.58 D_BLK3_INTV_CNT

- Description: VENC PMU state transition wait time counter register
- Offset: 0x18c
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_3	RW	VENC low power transition time counter between isolation cells releasing and clock enabling Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_3	RW	VENC low power transition time counter between isolation cells enabling and power on/off Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_3	RW	VENC low power transition time counter between

Bits	Field Name	Access	Description
			power on/off phase 1 and phase 2 Value After Reset: 0xFF

16.3.3.2.59 PD_BLK4_INTV_CNT

- Description: GPU PMU state transition wait time counter register
- Offset: 0x190
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_4	RW	GPU low power transition time counter between isolation cells releasing and clock enabling Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_4	RW	GPU low power transition time counter between isolation cells enabling and power on/off Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_4	RW	GPU low power transition time counter between power on/off phase 1 and phase 2 Value After Reset: 0xFF

16.3.3.2.60 PD_BLK5_INTV_CNT

- Description: DSP0 PMU state transition wait time counter register
- Offset: 0x194
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_5	RW	DSP0 low power transition time counter between isolation cells releasing and clock enabling Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_5	RW	DSP0 low power transition time counter between isolation cells enabling and power on/off Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_5	RW	DSP0 low power transition time counter between power on/off phase 1 and phase 2 Value After Reset: 0xFF

16.3.3.2.61 PD_BLK6_INTV_CNT

- Description: DSP1 PMU state transition wait time counter register

- Offset: 0x198
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_6	RW	DSP1 low power transition time counter between isolation cells releasing and clock enabling Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_6	RW	DSP1 low power transition time counter between isolation cells enabling and power on/off Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_6	RW	DSP1 low power transition time counter between power on/off phase 1 and phase 2 Value After Reset: 0xFF

16.3.3.2.62 PD_BLK7_INTV_CNT

- Description: C910 core0 PMU state transition wait time counter register
- Offset: 0x19c
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_7	RW	C910 core0 low power transition time counter between isolation cells releasing and clock enabling Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_7	RW	C910 core0 low power transition time counter between isolation cells enabling and power on/off Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_7	RW	C910 core0 low power transition time counter between power on/off phase 1 and phase 2 Value After Reset: 0xFF

16.3.3.2.63 PD_BLK8_INTV_CNT

- Description: C910 core1 PMU state transition wait time counter register
- Offset: 0x1a0
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_8	RW	C910 core1 low power transition time counter between isolation cells releasing and clock enabling Value After Reset: 0xFF

Bits	Field Name	Access	Description
[19:8]	ISO_SW_WAIT_CNT_8	RW	C910 core1 low power transition time counter between isolation cells enabling and power on/off Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_8	RW	C910 core1 low power transition time counter between power on/off phase 1 and phase 2 Value After Reset: 0xFF

16.3.3.2.64 PD_BLK9_INTV_CNT

- Description: C910 core2 PMU state transition wait time counter register
- Offset: 0x1a4
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_9	RW	C910 core2 low power transition time counter between isolation cells releasing and clock enabling Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_9	RW	C910 core2 low power transition time counter between isolation cells enabling and power on/off Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_9	RW	C910 core2 low power transition time counter between power on/off phase 1 and phase 2 Value After Reset: 0xFF

16.3.3.2.65 PD_BLK10_INTV_CNT

- Description: C910 core3 PMU state transition wait time counter register
- Offset: 0x1a8
- Default Value: 0xff0ffff

Bits	Field Name	Access	Description
[31:20]	ISO_WAIT_CNT_10	RW	C910 core3 low power transition time counter between isolation cells releasing and clock enabling Value After Reset: 0xFF
[19:8]	ISO_SW_WAIT_CNT_10	RW	C910 core3 low power transition time counter between isolation cells enabling and power on/off Value After Reset: 0xFF
[7:0]	SW0_SW1_WAIT_CNT_10	RW	C910 core3 low power transition time counter between power on/off phase 1 and phase 2

Bits	Field Name	Access	Description
			Value After Reset: 0xFF

16.3.3.2.66 AUDIO_PMU_REQ

- Description: AUDIO_SUBSYS low power request register
- Offset: 0x1f8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	AUDIO_PMU_REQ	RO	Low power request signal from AUDIO_SUBSYS Value After Reset: 0x0

16.3.3.2.67 AUDIO_PMU_STS

- Description: AUDIO_SUBSYS low power status register
- Offset: 0x1fc
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	AUDIO_PMU_STS	RO	Low power status signal from AUDIO_SUBSYS Value After Reset: 0x0

16.3.3.2.68 AUDIO_PMU_INTR

- Description: AUDIO_SUBSYS low power interrupt control and status register
- Offset: 0x204
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	AUDIO_PMU_INTR_MSK	RW	AUDIO_SUBSYS PMU interrupt mask control 0: Unmasked 1: Masked Value After Reset: 0x0
[2]	AUDIO_PMU_INTR_CLR	W1S	AUDIO_SUBSYS PMU interrupt clear signal Value After Reset: 0x0
[1]	AUDIO_PMU_INTR_STS	RO	AUDIO_SUBSYS PMU interrupt status Value After Reset: 0x0

Bits	Field Name	Access	Description
[0]	AUDIO_PMU_INTR_STS_RAW	RO	AUDIO_SUBSYS PMU interrupt raw status Value After Reset: 0x0

16.3.3.2.69 PMU_AUDIO_REQ

- Description: Low power request from AON_SUBSYS to AUDIO_SUBSYS
- Offset: 0x208
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	PMU_AUDIO_REQ	RW	Low power request signal to AUDIO_SUBSYS Value After Reset: 0x0

16.3.3.2.70 PMU_AUDIO_STS

- Description: Low power status data from AON_SUBSYS to AUDIO_SUBSYS
- Offset: 0x20c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PMU_AUDIO_STS	RW	Low power status data to AUDIO_SUBSYS Value After Reset: 0x0

16.3.3.2.71 MEM_LP_MODE

- Description: Memory low power mode control register
- Offset: 0x210
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:23]	RESERVED_6	-	
[22]	SRAM_AXI_AXI_SRAM_SD	RW	SRAM_AXI memory shut down mode control Value After Reset: 0x0
[21]	SRAM_AXI_AXI_SRAM_SLP	RW	SRAM_AXI memory sleep mode control Value After Reset: 0x0
[20]	SRAM_AXI_AXI_SRAM_DSLP	RW	SRAM_AXI memory deep sleep mode control Value After Reset: 0x0
[19]	RESERVED_5	-	

Bits	Field Name	Access	Description
[18]	C910_CPU_MEM_SD	RW	C910 top memory shut down mode control Value After Reset: 0x0
[17]	C910_CPU_MEM_SLP	RW	C910 top memory sleep mode control Value After Reset: 0x0
[16]	C910_CPU_MEM_DSLP	RW	C910 top memory deep sleep mode control Value After Reset: 0x0
[15]	RESERVED_4	-	
[14]	C910_CORE3_MEM_SD	RW	C910 core3 memory shut down mode control Value After Reset: 0x0
[13]	C910_CORE3_MEM_SLP	RW	C910 core3 memory sleep mode control Value After Reset: 0x0
[12]	C910_CORE3_MEM_DSLP	RW	C910 core3 memory deep sleep mode control Value After Reset: 0x0
[11]	RESERVED_3	-	
[10]	C910_CORE2_MEM_SD	RW	C910 core2 memory shut down mode control Value After Reset: 0x0
[9]	C910_CORE2_MEM_SLP	RW	C910 core2 memory sleep mode control Value After Reset: 0x0
[8]	C910_CORE2_MEM_DSLP	RW	C910 core2 memory deep sleep mode control Value After Reset: 0x0
[7]	RESERVED_2	-	
[6]	C910_CORE1_MEM_SD	RW	C910 core1 memory shut down mode control Value After Reset: 0x0
[5]	C910_CORE1_MEM_SLP	RW	C910 core1 memory sleep mode control Value After Reset: 0x0
[4]	C910_CORE1_MEM_DSLP	RW	C910 core1 memory deep sleep mode control Value After Reset: 0x0
[3]	RESERVED_1	-	
[2]	C910_CORE0_MEM_SD	RW	C910 core0 memory shut down mode control Value After Reset: 0x0
[1]	C910_CORE0_MEM_SLP	RW	C910 core0 memory sleep mode control

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[0]	C910_CORE0_MEM_DSLP	RW	C910 core0 memory deep sleep mode control Value After Reset: 0x0

16.3.3.2.72 C910_DBG_MASK

- Description: C910 debug enable control register
- Offset: 0x214
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	C910_CORE3_DBG_MASK	RW	C910 Core3 debug mask. Write 1 to this bit to disable C910 core3 debug mode. Value After Reset: 0x0
[2]	C910_CORE2_DBG_MASK	RW	C910 Core2 debug mask. Write 1 to this bit to disable C910 core2 debug mode. Value After Reset: 0x0
[1]	C910_CORE1_DBG_MASK	RW	C910 Core1 debug mask. Write 1 to this bit to disable C910 core1 debug mode. Value After Reset: 0x0
[0]	C910_CORE0_DBG_MASK	RW	C910 Core0 debug mask. Write 1 to this bit to disable C910 core0 debug mode. Value After Reset: 0x0

16.3.3.2.73 C910_L2CACHE

- Description: C910 L2CACHE flush control and status register
- Offset: 0x218
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	C910_CPU_NO_OP	RO	C910 idle state signal 0: C910 CPU is busy. 1: C910 CPU is in idle state. Value After Reset: 0x0
[1]	C910_CPU_L2CACHE_FLUSH_DO	RO	C910 L2Cache flush operation completion signal

Bits	Field Name	Access	Description
	NE		Value After Reset: 0x0
[0]	C910_CPU_L2CACHE_FLUSH_REQ	RW	C910 L2 cache flush request signal. Write 1 to this bit to flush all data in the C910 L2 cache. Value After Reset: 0x0

16.3.3.2.74 EFUSE_PRELOAD_DONE

- Description: eFuse preload completion status register
- Offset: 0x224
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	EFUSE_PRELOAD_DONE_REG	RO	eFuse preload completion register Value After Reset: 0x0

16.3.3.2.75 PLL_DSKEW_LOCK

- Description: PLL calibration control register
- Offset: 0x22c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	PLL_DSKEWCAL_BYPASS_REG	RW	PLL calibration bypass register, stores the PAD_PLL_DSKEWCAL_BYPASS value from PAD by software. Value After Reset: 0x0
[1]	PAD_PLL_DSKEWCAL_BYPASS	RO	PLL calibration bypass signal from PAD Value After Reset: 0x0
[0]	PLL_DSKEWCAL_BYPASS_LOCK	RW	Select the source of PLL deskewcal bypass signal. 0: Use PAD_PLL_DSKEWCAL_BYPASS as the PLL deskew bypass signal. 1: Use PLL_DSKEWCAL_BYPASS_REG as the PLL deskew bypass signal. Value After Reset: 0x0

16.3.3.2.76 SRAM_AXI_CFG

- Description: SRAMC configuration register

- Offset: 0x230
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_2	-	
[15:8]	SRAMC_PCHK_MODE	W1S	Memory access parity checking enable. Write any non-zero to enable parity check. Value After Reset: 0x0
[7:3]	RESERVED_1	-	
[2]	SRAMC_ACG_EN	RW	SRAMC auto clock gating enable Value After Reset: 0x0
[1]	SRAMC_OVCAP_DET	RW	Memory access boundary crossing detection enable control. Write 1 to this bit to enable boundary crossing detection. Value After Reset: 0x0
[0]	SRAMC_INIT	RW	Soft reset signal of SRAM controller, controlled by software Value After Reset: 0x0

16.3.3.2.77 SRAM_AXI_ST

- Description: SRAMC status register
- Offset: 0x234
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	SRAMC_OVCAP_ALARM	RO	Memory access boundary crossing detected. Value After Reset: 0x0

16.3.3.2.78 SRAM_AXI_ERR_STS_0

- Description: SRAMC error status register 0
- Offset: 0x238
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SRAMC_ERR_STS_0	RO	SRAMC error status signal, debug purpose only. Value After Reset: 0x0

16.3.3.2.79 SRAM_AXI_ERR_STS_1

- Description: SRAMC error status register 1
- Offset: 0x23c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SRAMC_ERR_STS_1	RO	SRAMC error status signal, debug purpose only. Value After Reset: 0x0

16.3.3.2.80 SRAM_AXI_ERR_STS_2

- Description: SRAMC error status register 2
- Offset: 0x240
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SRAMC_ERR_STS_2	RO	SRAMC error status signal, debug purpose only. Value After Reset: 0x0

16.3.3.2.81 SRAM_AXI_ERR_STS_3

- Description: SRAMC error status register 3
- Offset: 0x244
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SRAMC_ERR_STS_3	RO	SRAMC error status signal, debug purpose only. Value After Reset: 0x0

16.3.3.2.82 SRAM_AXI_ERR_STS_4

- Description: SRAMC error status register 4
- Offset: 0x248
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SRAMC_ERR_STS_4	RO	SRAMC error status signal, debug purpose only. Value After Reset: 0x0

16.3.3.2.83 SE_MUX_LOCK

- Description: Secure IO PADMUX registers' lock register
- Offset: 0x24c

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:7]	RESERVED_1	-	
[6:1]	SE_IO_MUX_LOCK	RW	Secure IO padmux register lock signal. When this bit is set, the PADMUX registers of secure IO pads are locked, and cannot changed by software. Value After Reset: 0x0
[0]	SE_RST_MUX_LOCK	RW	SE_RSTN padmux register lock signal. When this bit is set, the PADMUX registers of SE_RSTN pad is locked, and cannot changed by software. Value After Reset: 0x0

16.3.3.2.84 CPU_DBG_DIS_LOCK

- Description: Lock signal for CPU_DBG_DIS signal in MPJTAG
- Offset: 0x270
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	CPU_DBG_DIS_LOCK	RW	Lock signal for CPU_DBG_DIS signal in MPJTAG. When this bit is set, the MPJTAG will lock the CPU_DBG_DIS signal and ignore the external control signals. [0]: Lock signal for E902_DBG_DIS [1]: Lock signal for C906_DBG_DIS [2]: Lock signal for C910_DBG_DIS Value After Reset: 0x0

16.3.3.3 DDR_SUBSYS Control Registers

16.3.3.3.1 DDR_STS0

- Description: DDR system status
- Offset: 0x1c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:4]	DDR_CTL_IDLE	RO	DDR idle indicator Value After Reset: 0x0

Bits	Field Name	Access	Description
[3:2]	DDR_DFI_INIT_COMPLETE	RO	DDR DFI initialization finish indicator Value After Reset: 0x0
[1:0]	DDR_DFI_INIT_START	RO	DDR DFI initialization start indicator Value After Reset: 0x0

16.3.3.3.2 MRR_STS_CH0

- Description: ch0 MRR value
- Offset: 0x2c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	HIF_MRR_DATA	RO	ch0 MRR value Value After Reset: 0x0

16.3.3.3.3 MRR_STS_CH1

- Description: ch1 MRR value
- Offset: 0x30
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	HIF_MRR_DATA_DCH1	RO	ch1 MRR value Value After Reset: 0x0

16.3.3.3.4 DDR_STS1

- Description: DDR monitor configuration
- Offset: 0x34
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	MON_CLR	RW	Clear MRR_STS and DDR_STS1/STS2 Value After Reset: 0x0
[30:23]	RESERVED_3	-	
[22:16]	HPR_CREDIT_CNT	RO	Indicates the number of available high priority read CAM slots in every 8192 cycles. Value After Reset: 0x0
[15]	RESERVED_2	-	

Bits	Field Name	Access	Description
[14:8]	LPR_CREDIT_CNT	RO	Indicates the number of available low priority read CAM slots in every 8192 cycles. Value After Reset: 0x0
[7]	RESERVED_1	-	
[6:0]	WR_CREDIT_CNT	RO	Indicates the number of available write CAM slots in every 8192 cycles. Value After Reset: 0x0

16.3.3.3.5 DDR_STS2

- Description:
- Offset: 0x38
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:23]	RESERVED_3	-	
[22:16]	HPR_CREDIT_CNT_DCH1	RO	Indicates the number of available high priority ch1 read CAM slots in every 8192 cycles. Value After Reset: 0x0
[15]	RESERVED_2	-	
[14:8]	LPR_CREDIT_CNT_DCH1	RO	Indicates the number of available low priority ch1 read CAM slots in every 8192 cycles. Value After Reset: 0x0
[7]	RESERVED_1	-	
[6:0]	WR_CREDIT_CNT_DCH1	RO	Indicates the number of available write CAM ch1 slots in every 8192 cycles. Value After Reset: 0x0

16.3.3.3.6 DFI0_INFO

- Description: Debug status 0
- Offset: 0x3c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:20]	RESERVED_3	-	
[19]	DERATE_TEMP_LIMIT_INTR	RO	ch0 derate status 0 Value After Reset: 0x0

Bits	Field Name	Access	Description
[18]	DERATE_TEMP_LIMIT_INTR_FAULT	RO	ch0 derate status 1 Value After Reset: 0x0
[17]	DERATE_TEMP_LIMIT_INTR_DCH1	RO	ch1 derate status 0 Value After Reset: 0x0
[16]	DERATE_TEMP_LIMIT_INTR_FAULT_DCH1	RO	ch1 derate status 1 Value After Reset: 0x0
[15:13]	RESERVED_2	-	
[12]	DFI0_ERROR	RO	ch0 dfi0 error flag Value After Reset: 0x0
[11:8]	DFI0_ERROR_INFO	RO	ch0 dfi0 error information Value After Reset: 0x0
[7:5]	RESERVED_1	-	
[4]	DFI0_ERROR_DCH1	RO	ch1 dfi0 error flag Value After Reset: 0x0
[3:0]	DFI0_ERROR_INFO_DCH1	RO	ch1 dfi0 error information Value After Reset: 0x0

16.3.3.3.7 DDR_SRAM_CFG

- Description: DDR SDRAM LP mode configuration
- Offset: 0x40
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:28]	RESERVED_3	-	
[27]	O_DCCM_PUDELAY_U3_DCB	RO	SRAM PD status Value After Reset: 0x0
[26]	O_DCCM_PUDELAY_U2_DCB	RO	Value After Reset: 0x0
[25]	O_DCCM_PUDELAY_U1_DCB	RO	Value After Reset: 0x0
[24]	O_DCCM_PUDELAY_U0_DCB	RO	Value After Reset: 0x0
[23]	O_ICCM_PUDELAY_U1_DCB	RO	

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[22]	O_ICCM_PUDELAY_U0_DCB	RO	Value After Reset: 0x0
[21]	O_DCCM_PUDELAY_U3	RO	Value After Reset: 0x0
[20]	O_DCCM_PUDELAY_U2	RO	Value After Reset: 0x0
[19]	O_DCCM_PUDELAY_U1	RO	Value After Reset: 0x0
[18]	O_DCCM_PUDELAY_U0	RO	Value After Reset: 0x0
[17]	O_ICCM_PUDELAY_U1	RO	Value After Reset: 0x0
[16]	O_ICCM_PUDELAY_U0	RO	Value After Reset: 0x0
[15:7]	RESERVED_2	-	
[6]	I_SD_DCB	RW	1: ch1 ICCM/DCCM shut down mode 0: ch1 SRAM active mode Value After Reset: 0x0
[5]	I_DSLP_DCB	RW	1: ch1 enters ICCM/DCCM deep sleep mode 0: ch1 SRAM active mode Value After Reset: 0x0
[4]	I_SLP_DCB	RW	1: ch1 ICCM/DCCM in sleep mode 0: ch1 SRAM active mode Value After Reset: 0x0
[3]	RESERVED_1	-	
[2]	I_SD	RW	1: ch0 ICCM/DCCM shut down mode 0: ch0 SRAM active mode Value After Reset: 0x0
[1]	I_DSLP	RW	1: ch0 enters ICCM/DCCM deep sleep mode 0: ch0 SRAM active mode Value After Reset: 0x0

Bits	Field Name	Access	Description
[0]	I_SLP	RW	1: ch0 ICCM/DCCM in sleep mode 0: ch0 SRAM active mode Value After Reset: 0x0

16.3.3.3.8 DFI1_INFO

- Description: Error status of dfi1
- Offset: 0x44
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:13]	RESERVED_2	-	
[12]	DFI1_ERROR	RO	ch0 dfi1 error flag Value After Reset: 0x0
[11:8]	DFI1_ERROR_INFO	RO	ch0 dfi1 error information Value After Reset: 0x0
[7:5]	RESERVED_1	-	
[4]	DFI1_ERROR_DCH1	RO	ch1 dfi1 error flag Value After Reset: 0x0
[3:0]	DFI1_ERROR_INFO_DCH1	RO	ch1 dfi1 error information Value After Reset: 0x0

16.3.3.3.9 BPAC_CFG0

- Description: PHY bypass mode configuration
- Offset: 0x48
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	BYPASSMODEENAC	RW	Asynchronous bypass mode enable for ACX4 Value After Reset: 0x0
[30:24]	RESERVED_1	-	
[23:0]	BYPASSOUTENAC	RW	Per lane asynchronous input enable for bypass mode for ACX4 Value After Reset: 0x0

16.3.3.3.10 BPAC_CFG1

- Description:
- Offset: 0x4c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	BYPASSOUTDATAAC	RW	Per lane asynchronous input data for bypass mode for ACX4 Value After Reset: 0x0

16.3.3.3.11 BPAC_STS

- Description:
- Offset: 0x50
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	BYPASSINDATAAC	RO	Per lane asynchronous output data for bypass mode for ACX4 Value After Reset: 0x0

16.3.3.3.12 BPDA_CFG0

- Description:
- Offset: 0x54
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	BYPASSMODEENDAT	RW	Asynchronous bypass mode enable for DBYTE Value After Reset: 0x0
[30:24]	RESERVED_1	-	
[23:0]	BYPASSOUTENDAT_L	RW	Per lane asynchronous input enable for bypass mode for DBYTE Value After Reset: 0x0

16.3.3.3.13 BPDA_CFG1

- Description:
- Offset: 0x58

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	BYPASSOUTENDAT_H	RW	Per lane asynchronous input enable for bypass mode for DBYTE Value After Reset: 0x0

16.3.3.3.14 BPDA_CFG2

- Description:
- Offset: 0x5c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	BYPASSOUTDATADAT_L	RW	Per lane asynchronous input data for bypass mode for DBYTE Value After Reset: 0x0

16.3.3.3.15 BPDA_CFG3

- Description:
- Offset: 0x60
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	BYPASSOUTDATADAT_H	RW	Per lane asynchronous input data for bypass mode for DBYTE Value After Reset: 0x0

16.3.3.3.16 BPDA_STS0

- Description:
- Offset: 0x64
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	BYPASSINDATADAT_L	RO	Per lane asynchronous output data for bypass mode for DBYTE

Bits	Field Name	Access	Description
			Value After Reset: 0x0

16.3.3.3.17 BPDA_STS1

- Description:
- Offset: 0x68
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	BYPASSINDATADAT_H	RO	Per lane asynchronous output data for bypass mode for DBYTE Value After Reset: 0x0

16.3.3.3.18 BPMA_CFG

- Description:
- Offset: 0x6c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	BYPASSMODEENMASTER	RW	Asynchronous bypass mode enable for master Value After Reset: 0x0
[30:10]	RESERVED_3	-	
[9:8]	BYPASSOUTENMASTER	RW	Per lane asynchronous input enable for bypass mode for master Value After Reset: 0x0
[7:6]	RESERVED_2	-	
[5:4]	BYPASSOUTDATAMASTER	RW	Per lane asynchronous input data for bypass mode for master Value After Reset: 0x0
[3:2]	RESERVED_1	-	
[1:0]	BYPASSINDATAMASTER	RO	Per lane asynchronous output data for bypass mode for master Value After Reset: 0x0

16.3.3.3.19 BPAC_DCH_CFG0

- Description:

- Offset: 0x70
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	BYPASSMODEENAC_DCH	RW	Asynchronous bypass mode enable for ACX4 Value After Reset: 0x0
[30:24]	RESERVED_1	-	
[23:0]	BYPASSOUTENAC_DCH	RW	Per lane asynchronous input enable for bypass mode for ACX4 Value After Reset: 0x0

16.3.3.3.20 BPAC_DCH_CFG1

- Description:
- Offset: 0x74
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	BYPASSOUTDATAAC_DCH	RW	Per lane asynchronous input data for bypass mode for ACX4 Value After Reset: 0x0

16.3.3.3.21 BPAC_DCH_STS

- Description:
- Offset: 0x78
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	BYPASSINDATAAC_DCH	RO	Per lane asynchronous output data for bypass mode for ACX4 Value After Reset: 0x0

16.3.3.3.22 BPDA_DCH_CFG0

- Description:
- Offset: 0x7c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	BYPASSMODEENDAT_DCH	RW	Asynchronous bypass mode enable for DBYTE Value After Reset: 0x0
[30:24]	RESERVED_1	-	
[23:0]	BYPASSOUTENDAT_DCH_L	RW	Per lane asynchronous input enable for bypass mode for DBYTE Value After Reset: 0x0

16.3.3.3.23 BPDA_DCH_CFG1

- Description:
- Offset: 0x80
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	BYPASSOUTENDAT_DCH_H	RW	Per lane asynchronous input enable for bypass mode for DBYTE Value After Reset: 0x0

16.3.3.3.24 BPDA_DCH_CFG2

- Description:
- Offset: 0x84
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	BYPASSOUTDATADAT_DCH_L	RW	Per lane asynchronous input data for bypass mode for DBYTE Value After Reset: 0x0

16.3.3.3.25 BPDA_DCH_CFG3

- Description:
- Offset: 0x88
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	

Bits	Field Name	Access	Description
[23:0]	BYPASSOUTDATADAT_DCH_H	RW	Per lane asynchronous input data for bypass mode for DBYTE Value After Reset: 0x0

16.3.3.3.26 BPDA_DCH_STS0

- Description:
- Offset: 0x8c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	BYPASSINDATADAT_DCH_L	RO	Per lane asynchronous output data for bypass mode for DBYTE Value After Reset: 0x0

16.3.3.3.27 BPDA_DCH_STS1

- Description:
- Offset: 0x90
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	BYPASSINDATADAT_DCH_H	RO	Per lane asynchronous output data for bypass mode for DBYTE Value After Reset: 0x0

16.3.3.3.28 BPMA_DCH_CFG

- Description:
- Offset: 0x94
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	BYPASSMODEENMASTER_DCH	RW	Asynchronous bypass mode enable for master Value After Reset: 0x0
[30:10]	RESERVED_3	-	
[9:8]	BYPASSOUTENMASTER_DCH	RW	Per lane asynchronous input enable for bypass mode for master

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[7:6]	RESERVED_2	-	
[5:4]	BYPASSOUTDATAMASTER_DCH	RW	Per lane asynchronous input data for bypass mode for master Value After Reset: 0x0
[3:2]	RESERVED_1	-	
[1:0]	BYPASSINDATAMASTER_DCH	RO	Per lane asynchronous output data for bypass mode for master Value After Reset: 0x0

16.3.3.4 DSP_SUBSYS Control Registers

16.3.3.4.1 TEST_CLK_FREQ_STAT

- Description: Clock frequency status register
- Offset: 0x2c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	TEST_CLK_FREQ_STAT	RO	clk_calc output freq_stat Value After Reset: 0x0

16.3.3.4.2 TEST_CLK_CFG

- Description: Test clock configuration register
- Offset: 0x30
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_2	-	
[7:4]	TEST_CLK_SEL	RW	clk_calc clock select 0: dspsys_dsp0_cde 1: dspsys_dsp0_mclk_cde 2: dspsys_dsp0_sclk_cde 3: dspsys_dsp1_cde 4: dspsys_dsp1_mclk_cde 5: dspsys_dsp1_sclk_cde Value After Reset: 0x0

Bits	Field Name	Access	Description
[3:1]	RESERVED_1	-	
[0]	TEST_CLK_SAMPLE_EN	RW	clk_calc sample enable Value After Reset: 0x0

16.3.3.4.3 AXI4_DSPSYS_PRI

- Description: AXI4 bus priority configuration register
- Offset: 0x34
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:30]	RESERVED_6	-	
[29:28]	AXI4_DSPSYS_PRIORITY_M1	RW	Master arbitration priority associated with master port 1 (DSP0 outbound) of AXI_DSPSYS AXI bus in DSP_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[27:26]	RESERVED_5	-	
[25:24]	AXI4_DSPSYS_PRIORITY_M2	RW	Master arbitration priority associated with master port 2 (DSP0 iDMA) of AXI_DSPSYS AXI bus in DSP_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[23:22]	RESERVED_4	-	
[21:20]	AXI4_DSPSYS_PRIORITY_M3	RW	Master arbitration priority associated with master port 3 (DSP1 outbound) of AXI_DSPSYS AXI bus in DSP_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[19:18]	RESERVED_3	-	
[17:16]	AXI4_DSPSYS_PRIORITY_M4	RW	Master arbitration priority associated with master port 4 (DSP1 iDMA) of AXI_DSPSYS AXI bus in DSP_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[15:6]	RESERVED_2	-	
[5:4]	AXI4_DSPSYS_PRIORITY_S1	RW	Slave arbitration priority associated with slave port 1 (DDR) of AXI_DSPSYS AXI bus in DSP_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0

Bits	Field Name	Access	Description
[3:2]	RESERVED_1	-	
[1:0]	AXI4_DSPSYS_PRIORITY_S2	RW	Slave arbitration priority associated with slave port 2 (to VI_SUBSYS) of AXI_DSPSYS AXI bus in DSP_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0

16.3.3.4.4 AXI4_DSPSYS_PRI_SLV

- Description: AXI4 slave bus priority configuration register
- Offset: 0x38
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:29]	RESERVED_3	-	
[28]	AXI4_DSPSYS_SLV_PRIORITY_M1	RW	Master arbitration priority associated with master port 1 of AXI_DSPSYS_SLV AXI bus in DSP_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[27:6]	RESERVED_2	-	
[5:4]	AXI4_DSPSYS_SLV_PRIORITY_S1	RW	Slave arbitration priority associated with slave port 1 (DSP0) of AXI_DSPSYS_SLV AXI bus in DSP_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0
[3:2]	RESERVED_1	-	
[1:0]	AXI4_DSPSYS_SLV_PRIORITY_S2	RW	Slave arbitration priority associated with slave port 2 (DSP1) of AXI_DSPSYS_SLV AXI bus in DSP_SUBSYS. Larger value represents higher priority. Value After Reset: 0x0

16.3.3.4.5 DSP0_BUS_ADDR

- Description: DSP0 MSB8 address register
- Offset: 0x90
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:8]	DSP0_AXI4M1_AXI_AWADDR_MSB8	RW	DSP0 awaddr msb8[7:0] add awaddr[31:0] to form 40-bit awaddr.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[7:0]	DSP0_AXI4M1_AXI_ARADDR_MSB8	RW	DSP0 araddr msb8[7:0] add araddr[31:0] to form 40-bit araddr. Value After Reset: 0x0

16.3.3.4.6 DSP1_BUS_ADDR

- Description: DSP1 MSB8 address register
- Offset: 0x94
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:8]	DSP1_AXI4M1_AXI_AWADDR_MSB8	RW	DSP1 awaddr msb8[7:0] add awaddr[31:0] to form 40-bit awaddr. Value After Reset: 0x0
[7:0]	DSP1_AXI4M1_AXI_ARADDR_MSB8	RW	DSP1 araddr msb8[7:0] add araddr[31:0] to form 40-bit araddr. Value After Reset: 0x0

16.3.3.4.7 DSP_REMAP

- Description: DSP address remap enable register
- Offset: 0x98
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	DSP1_REMAP_ENABLE	RW	DSP1 access VI subsystem address remap enable 1: Remap address to access VI. 0: Not remap address to access VI. Value After Reset: 0x1
[0]	DSP0_REMAP_ENABLE	RW	DSP0 access VI subsystem address remap enable 1: Remap address to access VI. 0: Not remap address to access VI. Value After Reset: 0x1

16.3.3.4.8 DSP_DDR_CH_SEL

- Description: DSP access DDR bus select register
- Offset: 0x9c
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	DSP1_DDR_CH_SEL	RW	DSP1 access DDR 0: DSP access DDR not through AXI4_NPU bus. 1: DSP access DDR through AXI4_NPU bus. Value After Reset: 0x1
[0]	DSP0_DDR_CH_SEL	RW	DSP0 access DDR 0: DSP access DDR not through AXI4_NPU bus. 1: DSP access DDR through AXI4_NPU bus. Value After Reset: 0x1

16.3.3.4.9 TEST_CLK_FREQ_STAT_TEE

- Description: Clock frequency status TEE register
- Offset: 0x102c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	TEST_CLK_FREQ_STAT	RO	clk_calc output freq_stat Value After Reset: 0x0

16.3.3.4.10 TEST_CLK_CFG_TEE

- Description: Test clock configuration TEE register
- Offset: 0x1030
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_2	-	
[7:4]	TEST_CLK_SEL	RW	clk_calc clock select 0: dspsys_dsp0_cde 1: dspsys_dsp0_mclk_cde 2: dspsys_dsp0_sclk_cde 3: dspsys_dsp1_cde

Bits	Field Name	Access	Description
			4: dspsys_dsp1_mclk_cde 5: dspsys_dsp1_sclk_cde Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	TEST_CLK_SAMPLE_EN	RW	clk_calc sample enable Value After Reset: 0x0

16.3.3.4.11 AXI4_DSPSYS_PRI_TEE

- Description: AXI4 bus priority configuration TEE register
- Offset: 0x1034
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:30]	RESERVED_6	-	
[29:28]	AXI4_DSPSYS_PRIORITY_M1	RW	axi4_dspsys bus priority Value After Reset: 0x0
[27:26]	RESERVED_5	-	
[25:24]	AXI4_DSPSYS_PRIORITY_M2	RW	axi4_dspsys bus priority Value After Reset: 0x0
[23:22]	RESERVED_4	-	
[21:20]	AXI4_DSPSYS_PRIORITY_M3	RW	axi4_dspsys bus priority Value After Reset: 0x0
[19:18]	RESERVED_3	-	
[17:16]	AXI4_DSPSYS_PRIORITY_M4	RW	axi4_dspsys bus priority Value After Reset: 0x0
[15:6]	RESERVED_2	-	
[5:4]	AXI4_DSPSYS_PRIORITY_S1	RW	axi4_dspsys bus priority Value After Reset: 0x0
[3:2]	RESERVED_1	-	
[1:0]	AXI4_DSPSYS_PRIORITY_S2	RW	axi4_dspsys bus priority Value After Reset: 0x0

16.3.3.4.12 AXI4_DSPSYS_PRI_SLV_TEE

- Description: AXI4 slave bus priority configuration TEE register
- Offset: 0x1038
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:29]	RESERVED_3	-	
[28]	AXI4_DSPSYS_SLV_PRIORITY_M1	RW	axi4_dspsys slave bus priority Value After Reset: 0x0
[27:6]	RESERVED_2	-	
[5:4]	AXI4_DSPSYS_SLV_PRIORITY_S1	RW	axi4_dspsys slave bus priority Value After Reset: 0x0
[3:2]	RESERVED_1	-	
[1:0]	AXI4_DSPSYS_SLV_PRIORITY_S2	RW	axi4_dspsys slave bus priority Value After Reset: 0x0

16.3.3.4.13 DSP0_BUS_ADDR_TEE

- Description: DSP0 MSB8 address TEE register
- Offset: 0x1090
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:8]	DSP0_AXI4M1_AXI_AWADDR_MSB8	RW	DSP0 awaddr msb8, [39:32] Value After Reset: 0x0
[7:0]	DSP0_AXI4M1_AXI_ARADDR_MSB8	RW	DSP0 araddr msb8, [39:32] Value After Reset: 0x0

16.3.3.4.14 DSP1_BUS_ADDR_TEE

- Description: DSP1 MSB8 address TEE register
- Offset: 0x1094
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:8]	DSP1_AXI4M1_AXI_AWADDR_M	RW	DSP1 awaddr msb8, [39:32]

Bits	Field Name	Access	Description
	SB8		Value After Reset: 0x0
[7:0]	DSP1_AXI4M1_AXI_ARADDR_MSB8	RW	DSP1 araddr msb8, [39:32] Value After Reset: 0x0

16.3.3.4.15 DSP_REMAP_TEE

- Description: DSP address remap enable TEE register
- Offset: 0x1098
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	DSP1_REMAP_ENABLE	RW	DSP1 access VI subsystem address remap enable 1: Remap address to access VI. 0: Not remap address to access VI. Value After Reset: 0x1
[0]	DSP0_REMAP_ENABLE	RW	DSP0 access VI subsystem address remap enable 1: Remap address to access VI. 0: Not remap address to access VI. Value After Reset: 0x1

16.3.3.4.16 DSP_DDR_CH_SEL_TEE

- Description: DSP access DDR bus select TEE register
- Offset: 0x109c
- Default Value: 0x3

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	DSP1_DDR_CH_SEL	RW	DSP1 access DDR 0: DSP access DDR not through AXI4_NPU bus. 1: DSP access DDR through AXI4_NPU bus. Value After Reset: 0x1
[0]	DSP0_DDR_CH_SEL	RW	DSP0 access DDR 0: DSP access DDR not through AXI4_NPU bus. 1: DSP access DDR through AXI4_NPU bus. Value After Reset: 0x1

16.3.3.4.17 CFG_CLK_LOCK_TEE

- Description: Clock lock TEE register
- Offset: 0x1140
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_4	-	
[30]	DSP_SUBSYS_CLKCFG_LOCK	RW	dsp_subsys_clkcfg_lock Value After Reset: 0x0
[29:26]	RESERVED_3	-	
[25]	DSP_SUBSYS_SLV_CLKCFG_LOCK	RW	dsp_subsys_slv_clkcfg_lock Value After Reset: 0x0
[24:7]	RESERVED_2	-	
[6]	DSPSYS_CLKCFG_LOCK	RW	dspsys_clkcfg_lock Value After Reset: 0x0
[5]	DSP0_CLKCFG_LOCK	RW	dsp0_clkcfg_lock Value After Reset: 0x0
[4]	DSP1_CLKCFG_LOCK	RW	dsp1_clkcfg_lock Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	TEST_CLK_CFG_LOCK	RW	test_clk_cfg_lock Value After Reset: 0x0

16.3.3.4.18 CFG_RST_LOCK_TEE

- Description: Reset lock TEE register
- Offset: 0x1144
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_4	-	
[30]	DSP_SUBSYS_RSTCFG_LOCK	RW	dsp_subsys_rstcfg_lock Value After Reset: 0x0
[29:26]	RESERVED_3	-	
[25]	DSP_SUBSYS_SLV_RSTCFG_LOCK	RW	dsp_subsys_slv_rstcfg_lock Value After Reset: 0x0

Bits	Field Name	Access	Description
[24:6]	RESERVED_2	-	
[5]	DSP0_RSTCFG_LOCK	RW	dsp0_rstcfg_lock Value After Reset: 0x0
[4]	DSP1_RSTCFG_LOCK	RW	dsp1_rstcfg_lock Value After Reset: 0x0
[3:0]	RESERVED_1	-	

16.3.3.4.19 CFG_DSPSYS_LOCK_TEE

- Description: DSP subsystem lock TEE register
- Offset: 0x1148
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_1	-	
[8]	DSP1_DDR_CH_SEL_LOCK	RW	dsp1_ddr_ch_sel_lock Value After Reset: 0x0
[7]	DSP0_DDR_CH_SEL_LOCK	RW	dsp0_ddr_ch_sel_lock Value After Reset: 0x0
[6]	DSP1_REMAP_LOCK	RW	dsp1_remap_lock Value After Reset: 0x0
[5]	DSP0_REMAP_LOCK	RW	dsp0_remap_lock Value After Reset: 0x0
[4]	DSPSYS_BUS_CFG_LOCK	RW	dspsys_bus_cfg_lock Value After Reset: 0x0
[3]	RESERVED_REG0_LOCK	RW	reserved_reg0_lock Value After Reset: 0x0
[2]	RESERVED_REG1_LOCK	RW	reserved_reg1_lock Value After Reset: 0x0
[1]	DSP0_BUS_CFG_LOCK	RW	dsp0_bus_cfg_lock Value After Reset: 0x0
[0]	DSP1_BUS_CFG_LOCK	RW	dsp1_bus_cfg_lock Value After Reset: 0x0

16.3.3.5 PERI_SUBSYS Control Registers

16.3.3.5.1 USB3_AXI_QOS_PRIORITY

- Description: USB AXI bus configuration register
- Offset: 0x200
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:8]	USB3_AXI_PRIORITY	RW	USB AXI bus master port priority set Value After Reset: 0x0
[7:4]	USB3_AXI_AWQOS	RW	USB AXI bus AWQOS configuration Value After Reset: 0x0
[3:0]	USB3_AXI_ARQOS	RW	USB AXI bus ARQOS configuration Value After Reset: 0x0

16.3.3.5.2 GMAC_AXI_QOS_PRIORITY

- Description: GMAC AXI bus configuration register
- Offset: 0x204
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:8]	GMAC_AXI_PRIORITY	RW	GMAC AXI bus master port priority set Value After Reset: 0x0
[7:4]	GMAC_AXI_AWQOS	RW	GMAC AXI bus AWQOS configuration Value After Reset: 0x0
[3:0]	GMAC_AXI_ARQOS	RW	GMAC AXI bus ARQOS configuration Value After Reset: 0x0

16.3.3.5.3 EMMC_AXI_QOS_PRIORITY

- Description: eMMC AXI bus configuration register
- Offset: 0x208
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	

Bits	Field Name	Access	Description
[10:8]	EMMC_AXI_PRIORITY	RW	eMMC AXI bus master port priority set Value After Reset: 0x0
[7:4]	EMMC_AXI_AWQOS	RW	eMMC AXI bus AWQOS configuration Value After Reset: 0x0
[3:0]	EMMC_AXI_ARQOS	RW	eMMC AXI bus ARQOS configuration Value After Reset: 0x0

16.3.3.5.4 SDIO0_AXI_QOS_PRIORITY

- Description: SDIO0 AXI bus configuration register
- Offset: 0x20c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:8]	SDIO0_AXI_PRIORITY	RW	SDIO0 AXI bus master port priority set Value After Reset: 0x0
[7:4]	SDIO0_AXI_AWQOS	RW	SDIO0 AXI bus AWQOS configuration Value After Reset: 0x0
[3:0]	SDIO0_AXI_ARQOS	RW	SDIO0 AXI bus ARQOS configuration Value After Reset: 0x0

16.3.3.5.5 SDIO1_AXI_QOS_PRIORITY

- Description: SDIO1 AXI bus configuration register
- Offset: 0x210
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:8]	SDIO1_AXI_PRIORITY	RW	SDIO1 AXI bus master port priority set Value After Reset: 0x0
[7:4]	SDIO1_AXI_AWQOS	RW	SDIO1 AXI bus AWQOS configuration Value After Reset: 0x0
[3:0]	SDIO1_AXI_ARQOS	RW	SDIO1 AXI bus ARQOS configuration Value After Reset: 0x0

16.3.3.5.6 EMMC_TEST_CTRL

- Description: eMMC test register 0
- Offset: 0x220
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_3	-	
[8]	EMMC_TEST_PAD_MODE	RW	eMMC test pad mode Value After Reset: 0x0
[7:5]	RESERVED_2	-	
[4]	EMMC_TEST_INTF_SEL	RW	eMMC test interface select Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	EMMC_TEST_DLOUT_EN	RW	eMMC test dlout enable Value After Reset: 0x0

16.3.3.5.7 EMMC_TEST_PAD_O

- Description:
- Offset: 0x224
- Default Value: 0xfff

Bits	Field Name	Access	Description
[31:12]	RESERVED_1	-	
[11:0]	EMMC_TEST_PAD_O	RW	eMMC test pad output Value After Reset: 0xFFF

16.3.3.5.8 EMMC_TEST_PAD_OEN

- Description:
- Offset: 0x228
- Default Value: 0xfff

Bits	Field Name	Access	Description
[31:12]	RESERVED_1	-	
[11:0]	EMMC_TEST_PAD_OEN	RW	eMMC test pad output enable Value After Reset: 0xFFF

16.3.3.5.9 EMMC_TEST_PAD_I

- Description:
- Offset: 0x22c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:12]	RESERVED_1	-	
[11:0]	EMMC_TEST_PAD_I	RO	eMMC test pad input Value After Reset: 0x0

16.3.3.5.10 SDIO0_TEST_CTRL

- Description: SDIO0 test register 0
- Offset: 0x230
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_3	-	
[8]	SDIO0_TEST_PAD_MODE	RW	SDIO0 test pad mode Value After Reset: 0x0
[7:5]	RESERVED_2	-	
[4]	SDIO0_TEST_INTF_SEL	RW	SDIO0 test interface select Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	SDIO0_TEST_DLOUT_EN	RW	SDIO0 test dlout enable Value After Reset: 0x0

16.3.3.5.11 SDIO0_TEST_PAD_O

- Description:
- Offset: 0x234
- Default Value: 0x3f

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:0]	SDIO0_TEST_PAD_O	RW	SDIO0 test pad output Value After Reset: 0x3F

16.3.3.5.12 SDIO0_TEST_PAD_OEN

- Description:
- Offset: 0x238
- Default Value: 0x3f

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:0]	SDIO0_TEST_PAD_OEN	RW	SDIO0 test pad output enable Value After Reset: 0x3F

16.3.3.5.13 SDIO0_TEST_PAD_I

- Description:
- Offset: 0x23c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:0]	SDIO0_TEST_PAD_I	RO	SDIO0 test pad input Value After Reset: 0x0

16.3.3.5.14 SDIO1_TEST_CTRL

- Description: SDIO1 test register 0
- Offset: 0x240
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_3	-	
[8]	SDIO1_TEST_PAD_MODE	RW	SDIO1 test pad mode Value After Reset: 0x0
[7:5]	RESERVED_2	-	
[4]	SDIO1_TEST_INTF_SEL	RW	SDIO1 test interface select Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	SDIO1_TEST_DLOUT_EN	RW	SDIO1 test dlout enable Value After Reset: 0x0

16.3.3.5.15 SDIO1_TEST_PAD_O

- Description:
- Offset: 0x244
- Default Value: 0x3f

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:0]	SDIO1_TEST_PAD_O	RW	SDIO1 test pad output Value After Reset: 0x3F

16.3.3.5.16 SDIO1_TEST_PAD_OEN

- Description:
- Offset: 0x248
- Default Value: 0x3f

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:0]	SDIO1_TEST_PAD_OEN	RW	SDIO1 test pad output enable Value After Reset: 0x3F

16.3.3.5.17 SDIO1_TEST_PAD_I

- Description:
- Offset: 0x24c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:0]	SDIO1_TEST_PAD_I	RO	SDIO1 test pad input Value After Reset: 0x0

16.3.3.5.18 SW_REG0

- Description: Software register 0
- Offset: 0x300
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG0	RW	Software register 0 Value After Reset: 0x0

16.3.3.5.19 SW_REG1

- Description: Software register 1
- Offset: 0x304
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG1	RW	Software register 1 Value After Reset: 0x0

16.3.3.5.20 SW_REG2

- Description: Software register 2
- Offset: 0x308
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG2	RW	Software register 2 Value After Reset: 0x0

16.3.3.5.21 SW_REG3

- Description: Software register 3
- Offset: 0x30C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG3	RW	Software register 3 Value After Reset: 0x0

16.3.3.5.22 USB3_AXI_QOS_PRIORITY_TEE

- Description: USB AXI bus configuration register
- Offset: 0x1200
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:8]	USB3_AXI_PRIORITY	RW	USB AXI bus master port priority set Value After Reset: 0x0
[7:4]	USB3_AXI_AWQOS	RW	USB AXI bus AWQOS configuration Value After Reset: 0x0

Bits	Field Name	Access	Description
[3:0]	USB3_AXI_ARQOS	RW	USB AXI bus ARQOS configuration Value After Reset: 0x0

16.3.3.5.23 GMAC_AXI_QOS_PRIORITY_TEE

- Description: GMAC AXI bus configuration register
- Offset: 0x1204
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:8]	GMAC_AXI_PRIORITY	RW	GMAC AXI bus master port priority set Value After Reset: 0x0
[7:4]	GMAC_AXI_AWQOS	RW	GMAC AXI bus AWQOS configuration Value After Reset: 0x0
[3:0]	GMAC_AXI_ARQOS	RW	GMAC AXI bus ARQOS configuration Value After Reset: 0x0

16.3.3.5.24 EMMC_AXI_QOS_PRIORITY_TEE

- Description: eMMC AXI bus configuration register
- Offset: 0x1208
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:8]	EMMC_AXI_PRIORITY	RW	eMMC AXI bus master port priority set Value After Reset: 0x0
[7:4]	EMMC_AXI_AWQOS	RW	eMMC AXI bus AWQOS configuration Value After Reset: 0x0
[3:0]	EMMC_AXI_ARQOS	RW	eMMC AXI bus ARQOS configuration Value After Reset: 0x0

16.3.3.5.25 SDIO0_AXI_QOS_PRIORITY_TEE

- Description: SDIO0 AXI bus configuration register
- Offset: 0x120c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:8]	SDIO0_AXI_PRIORITY	RW	SDIO0 AXI bus master port priority set Value After Reset: 0x0
[7:4]	SDIO0_AXI_AWQOS	RW	SDIO0 AXI bus AWQOS configuration Value After Reset: 0x0
[3:0]	SDIO0_AXI_ARQOS	RW	SDIO0 AXI bus ARQOS configuration Value After Reset: 0x0

16.3.3.5.26 SDIO1_AXI_QOS_PRIORITY_TEE

- Description: SDIO1 AXI bus configuration register
- Offset: 0x1210
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:8]	SDIO1_AXI_PRIORITY	RW	SDIO1 AXI bus master port priority set Value After Reset: 0x0
[7:4]	SDIO1_AXI_AWQOS	RW	SDIO1 AXI bus AWQOS configuration Value After Reset: 0x0
[3:0]	SDIO1_AXI_ARQOS	RW	SDIO1 AXI bus ARQOS configuration Value After Reset: 0x0

16.3.3.5.27 TEE_AXI_QOS_PRIORITY_TEE

- Description: TEE AXI bus configuration register
- Offset: 0x1214
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:8]	TEE_AXI_PRIORITY	RW	TEE AXI bus master port priority set Value After Reset: 0x0
[7:4]	TEE_AXI_AWQOS	RW	TEE AXI bus AWQOS configuration Value After Reset: 0x0
[3:0]	TEE_AXI_ARQOS	RW	TEE AXI bus ARQOS configuration

Bits	Field Name	Access	Description
			Value After Reset: 0x0

16.3.3.5.28 MISCSYS_AXI_QOS_PRIORITY_TEE

- Description: MISC AXI bus configuration register
- Offset: 0x1218
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MISCSYS_AXI_PRIORITY	RW	MISC AXI bus slave port priority set Value After Reset: 0x0

16.3.3.5.29 EMMC_TEST_CTRL_TEE

- Description: eMMC TEST register 0
- Offset: 0x1220
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_3	-	
[8]	EMMC_TEST_PAD_MODE	RW	eMMC test pad mode Value After Reset: 0x0
[7:5]	RESERVED_2	-	
[4]	EMMC_TEST_INTF_SEL	RW	eMMC test interface select Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	EMMC_TEST_DLOUT_EN	RW	eMMC TEST dlout enable Value After Reset: 0x0

16.3.3.5.30 EMMC_TEST_PAD_O_TEE

- Description:
- Offset: 0x1224
- Default Value: 0xfff

Bits	Field Name	Access	Description
[31:12]	RESERVED_1	-	

Bits	Field Name	Access	Description
[11:0]	EMMC_TEST_PAD_O	RW	eMMC test pad output Value After Reset: 0xFFF

16.3.3.5.31 EMMC_TEST_PAD_OEN_TEE

- Description:
- Offset: 0x1228
- Default Value: 0xfff

Bits	Field Name	Access	Description
[31:12]	RESERVED_1	-	
[11:0]	EMMC_TEST_PAD_OEN	RW	eMMC test pad output enable Value After Reset: 0xFFF

16.3.3.5.32 EMMC_TEST_PAD_I_TEE

- Description:
- Offset: 0x122c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:12]	RESERVED_1	-	
[11:0]	EMMC_TEST_PAD_I	RO	eMMC test pad input Value After Reset: 0x0

16.3.3.5.33 SDIO0_TEST_CTRL_TEE

- Description: SDIO0 test register 0
- Offset: 0x1230
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_3	-	
[8]	SDIO0_TEST_PAD_MODE	RW	SDIO0 test pad mode Value After Reset: 0x0
[7:5]	RESERVED_2	-	
[4]	SDIO0_TEST_INTF_SEL	RW	SDIO0 test interface select Value After Reset: 0x0
[3:1]	RESERVED_1	-	

Bits	Field Name	Access	Description
[0]	SDIO0_TEST_DLOUT_EN	RW	SDIO0 test dlout enable Value After Reset: 0x0

16.3.3.5.34 SDIO0_TEST_PAD_O_TEE

- Description:
- Offset: 0x1234
- Default Value: 0x3f

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:0]	SDIO0_TEST_PAD_O	RW	SDIO0 test pad output Value After Reset: 0x3F

16.3.3.5.35 SDIO0_TEST_PAD_OEN_TEE

- Description:
- Offset: 0x1238
- Default Value: 0x3f

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:0]	SDIO0_TEST_PAD_OEN	RW	SDIO0 test pad output enable Value After Reset: 0x3F

16.3.3.5.36 SDIO0_TEST_PAD_I_TEE

- Description:
- Offset: 0x123c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:0]	SDIO0_TEST_PAD_I	RO	SDIO0 test pad input Value After Reset: 0x0

16.3.3.5.37 SDIO1_TEST_CTRL_TEE

- Description: SDIO1 test register 0
- Offset: 0x1240
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_3	-	
[8]	SDIO1_TEST_PAD_MODE	RW	SDIO1 test pad mode Value After Reset: 0x0
[7:5]	RESERVED_2	-	
[4]	SDIO1_TEST_INTF_SEL	RW	SDIO1 test interface select Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	SDIO1_TEST_DLOUT_EN	RW	SDIO1 test dlout enable Value After Reset: 0x0

16.3.3.5.38 SDIO1_TEST_PAD_O_TEE

- Description:
- Offset: 0x1244
- Default Value: 0x3f

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:0]	SDIO1_TEST_PAD_O	RW	SDIO1 test pad output Value After Reset: 0x3F

16.3.3.5.39 SDIO1_TEST_PAD_OEN_TEE

- Description:
- Offset: 0x1248
- Default Value: 0x3f

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:0]	SDIO1_TEST_PAD_OEN	RW	SDIO1 test pad output enable Value After Reset: 0x3F

16.3.3.5.40 SDIO1_TEST_PAD_I_TEE

- Description:
- Offset: 0x124c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:0]	SDIO1_TEST_PAD_I	RO	SDIO1 test pad input Value After Reset: 0x0

16.3.3.5.41 SW_REG0_TEE

- Description: Software register 0
- Offset: 0x1300
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG0	RW	Software register 0 Value After Reset: 0x0

16.3.3.5.42 SW_REG1_TEE

- Description: Software register 1
- Offset: 0x1304
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG1	RW	Software register 1 Value After Reset: 0x0

16.3.3.5.43 SW_REG2_TEE

- Description: Software register 2
- Offset: 0x1308
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG2	RW	Software register 2 Value After Reset: 0x0

16.3.3.5.44 SW_REG3_TEE

- Description: Software register 3
- Offset: 0x130C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SW_REG3	RW	Software register 3 Value After Reset: 0x0

16.3.3.5.45 SYSREG_LOCK_0_TEE

- Description: MISC_SUBSYS sysreg lock registers
- Offset: 0x1800
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:22]	RESERVED_1	-	
[21]	SW_REG_LOCK	RW	MISC_SUBSYS SYSREG configuration register's lock bit Value After Reset: 0x0
[20]	SDIO1_TEST_CTRL_LOCK	RW	SDIO1 test register's lock bit Value After Reset: 0x0
[19]	SDIO0_TEST_CTRL_LOCK	RW	SDIO0 test register's lock bit Value After Reset: 0x0
[18]	EMMC_TEST_CTRL_LOCK	RW	EMMC test register's lock bit Value After Reset: 0x0
[17]	MISCSYS_AXI_QOS_PRIORITY_LOCK	RW	MISC_SUBSYS AXI bus configuration register's lock bit Value After Reset: 0x0
[16]	TEE_AXI_QOS_PRIORITY_LOCK	RW	TEE AXI bus configuration register's lock bit Value After Reset: 0x0
[15]	SDIO1_AXI_QOS_PRIORITY_LOCK	RW	SDIO1 AXI bus configuration register's lock bit Value After Reset: 0x0
[14]	SDIO0_AXI_QOS_PRIORITY_LOCK	RW	SDIO0 AXI bus configuration register's lock bit Value After Reset: 0x0
[13]	EMMC_AXI_QOS_PRIORITY_LOCK	RW	EMMC AXI bus configuration register's lock bit Value After Reset: 0x0
[12]	GMAC_AXI_QOS_PRIORITY_LOCK	RW	GMAC AXI bus configuration register's lock bit Value After Reset: 0x0
[11]	USB3_AXI_QOS_PRIORITY_LOCK	RW	USB AXI bus configuration register's lock bit Value After Reset: 0x0
[10]	MISCSYS_SDIO1_CLK_CTRL_LOC	RW	MISCSYS_SDIO1_CLK_configuration register's lock bit

Bits	Field Name	Access	Description
	K		Value After Reset: 0x0
[9]	MISCSYS_SDIO0_CLK_CTRL_LOCK	RW	MISCSYS_SDIO0_CLK_configuration register's lock bit Value After Reset: 0x0
[8]	MISCSYS_EMMC_CLK_CTRL_LOCK	RW	MISCSYS_EMMC_CLK_configuration register's lock bit Value After Reset: 0x0
[7]	MISCSYS_USB_CLK_CTRL_LOCK	RW	MISCSYS_USB_CLK_configuration register's lock bit Value After Reset: 0x0
[6]	MISCSYS_BUS_CLK_CTRL_LOCK	RW	MISCSYS_BUS_CLK_configuration register's lock bit Value After Reset: 0x0
[5]	USB3_DRD_SWRST_LOCK	RW	USB3_DRD's soft reset configuration register's lock bit Value After Reset: 0x0
[4]	SDIO1_SWRST_LOCK	RW	SDIO1's soft reset configuration register's lock bit Value After Reset: 0x0
[3]	SDIO0_SWRST_LOCK	RW	SDIO0's soft reset configuration register's lock bit Value After Reset: 0x0
[2]	MISCSYS_AXI_SWRST_LOCK	RW	MISCSYS AXI BUS's soft reset configuration register's lock bit Value After Reset: 0x0
[1]	MISCSYS_APB_SWRST_LOCK	RW	MISCSYS APB BUS's soft reset configuration register's lock bit Value After Reset: 0x0
[0]	EMMC_SWRST_LOCK	RW	eMMC's soft reset configuration register's lock bit Value After Reset: 0x0

16.3.3.6 VI_SUBSYS Control Registers

16.3.3.6.1 VISYS_CONTROL

- Description: VISYS_CONTROL
- Offset: 0x120
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:30]	RESERVED_6	-	
[29]	VIPRE_REMAP_EN	RW	vipre_remap_en, not used, need to set 0.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[28]	VIPRE_RANK_SEL	RW	vipre_rank_sel, not used Value After Reset: 0x0
[27:26]	RESERVED_5	-	
[25]	DW200_REMAP_EN	RW	dw200_remap_en, address remap enable when MMU is OFF, active high. Value After Reset: 0x0
[24]	DW200_RANK_SEL	RW	dw200_rank_sel 0: Original address to DDR. 1: Original address would add 0x1_0000_0000 to DDR. Value After Reset: 0x0
[23:22]	RESERVED_4	-	
[21]	ISP1_REMAP_EN	RW	isp1_remap_en, address remap enable when MMU is OFF, active high. Value After Reset: 0x0
[20]	ISP1_RANK_SEL	RW	isp1_rank_sel 0: Original address to DDR. 1: Original address would add 0x1_0000_0000 to DDR. Value After Reset: 0x0
[19:18]	RESERVED_3	-	
[17]	ISP0_REMAP_EN	RW	isp0_remap_en, address remap enable when MMU is OFF, active high. Value After Reset: 0x0
[16]	ISP0_RANK_SEL	RW	isp0_rank_sel 0: Original address to DDR. 1: Original address would add 0x1_0000_0000 to DDR. Value After Reset: 0x0
[15:9]	RESERVED_2	-	
[8]	ISP_VENC_SHAKE_CHANNEL_SEL	RW	0: Monitor vi2ddr channel_x000D_. 1: Monitor vi2sram channel. Value After Reset: 0x0
[7:3]	RESERVED_1	-	
[2]	ISP_RY_DISABLE_ISP_0	RW	Disable ISP RY, 1 means disable.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[1]	ISP1_DISABLE_ISP_0	RW	Disable ISP1, 1 means disable. Value After Reset: 0x0
[0]	ISP0_DISABLE_ISP_0	RW	Disable ISP0, 1 means disable. Value After Reset: 0x0

16.3.3.6.2 MIPI_CSI0_CTRL

- Description: MIPI_CSI0_CTRL
- Offset: 0x140
- Default Value: 0x10010a1c

Bits	Field Name	Access	Description
[31:29]	RESERVED_6	-	
[28]	MIPI_CSI2_BASEDIR_0	RW	1: lane0 RX, 0:lane0 TX Configures the base direction for CSI2-DPHY Lane. Value After Reset: 0x1
[27:26]	RESERVED_5	-	
[25]	MIPI_CSI2_FORCERXMODE_0	RW	1: Force lane0 to receive control mode and wait stop state. Value After Reset: 0x0
[24]	MIPI_CSI2_TURNDISABLE_0	RW	1: Prohibit turnaround. Value After Reset: 0x0
[23]	RESERVED_4	-	
[22]	MIPI_CSI2_FORCERXMODE_1	RW	1: Force lane1 to receive control mode and wait stop state. Value After Reset: 0x0
[21]	MIPI_CSI2_FORCERXMODE_2	RW	1: Force lane2 to receive control mode and wait stop state. Value After Reset: 0x0
[20]	MIPI_CSI2_FORCERXMODE_3	RW	1: Force lane3 to receive control mode and wait stop state. Value After Reset: 0x0
[19:17]	RESERVED_3	-	
[16]	MIPI_CSI2_ENABLECLK	RW	When Shutdownz = rstz = 0, set 1 clock to enable PPI, or

Bits	Field Name	Access	Description
			0: Turn off all PPI reception. Value After Reset: 0x1
[15]	RESERVED_2	-	
[14:8]	MIPI_CSI2_HSFREQRANGE	RW	High speed frequency range selection, default 1Gbps range. Value After Reset: 0xA
[7:6]	RESERVED_1	-	
[5:0]	MIPI_CSI2_CFGCLKFREQRANGE	RW	Round (Fcfg_clk(MHz) - 17)*4, default 28. Value After Reset: 0x1C

16.3.3.6.3 MIPI_CSI1_CTRL

- Description: MIPI_CSI1_CTRL
- Offset: 0x144
- Default Value: 0x10010a1c

Bits	Field Name	Access	Description
[31:29]	RESERVED_6	-	
[28]	MIPI_CSI2X2_A_BASEDIR_0	RW	1: lane0 RX, 0: lane0 TX Configures the base direction for BPHY lane. Value After Reset: 0x1
[27:26]	RESERVED_5	-	
[25]	MIPI_CSI2X2_A_FORCERXMODE_0	RW	1: Force APHY lane0 to receive control mode and wait stop state. Value After Reset: 0x0
[24]	MIPI_CSI2X2_A_TURNDISABLE_0	RW	1: Prohibit turnaround. Value After Reset: 0x0
[23]	RESERVED_4	-	
[22]	MIPI_CSI2X2_A_FORCERXMODE_1	RW	1: Force APHY lane1 to receive control mode and wait stop state. Value After Reset: 0x0
[21:17]	RESERVED_3	-	
[16]	MIPI_CSI2X2_A_ENABLECLK	RW	When Shutdownz = rstz = 0, set 1 clock to enable PPI, or 0: turn off all PPI reception. Value After Reset: 0x1

Bits	Field Name	Access	Description
[15]	RESERVED_2	-	
[14:8]	MIPI_CSI2X2_A_HSFREQRANGE	RW	High speed frequency range selection, default 1Gbps range. Value After Reset: 0xA
[7:6]	RESERVED_1	-	
[5:0]	MIPI_CSI2X2_A_CFGCLKFREQRANGE	RW	Round (Fcfg_clk(MHz) - 17)*4, default 28. Value After Reset: 0x1C

16.3.3.6.4 MIPI_CSI2_CTRL

- Description: MIPI_CSI2_CTRL
- Offset: 0x148
- Default Value: 0x10010a1c

Bits	Field Name	Access	Description
[31:29]	RESERVED_6	-	
[28]	MIPI_CSI2X2_B_BASEDIR_0	RW	1: lane0 RX, 0: lane0 TX Configures the base direction for BPHY lane. Value After Reset: 0x1
[27:26]	RESERVED_5	-	
[25]	MIPI_CSI2X2_B_FORCERXMODE_0	RW	1: Force BPHY lane0 to receive control mode and wait stop state. Value After Reset: 0x0
[24]	MIPI_CSI2X2_B_TURNDISABLE_0	RW	1: Prohibit turnaround. Value After Reset: 0x0
[23]	RESERVED_4	-	
[22]	MIPI_CSI2X2_B_FORCERXMODE_1	RW	1: Force BPHY lane1 to receive control mode and wait stop state. Value After Reset: 0x0
[21:17]	RESERVED_3	-	
[16]	MIPI_CSI2X2_B_ENABLECLK	RW	When Shutdownz = rstz = 0, set 1 clock to enable PPI, or 0: turn off all PPI reception. Value After Reset: 0x1
[15]	RESERVED_2	-	
[14:8]	MIPI_CSI2X2_B_HSFREQRANGE	RW	High speed frequency range selection, default 1Gbps

Bits	Field Name	Access	Description
			range. Value After Reset: 0xA
[7:6]	RESERVED_1	-	
[5:0]	MIPI_CSI2X2_B_CFGCLKFREQRANGE	RW	Round (Fcfg_clk(MHz) - 17)*4, default 28. Value After Reset: 0x1C

16.3.3.6.5 MIPI_CSI_FIFO_CTRL

- Description: MIPI_CSI_FIFO_CTRL
- Offset: 0x14C
- Default Value: 0x1f00

Bits	Field Name	Access	Description
[31]	MIPI_CSI2X2_A_ENABLE	RW	Default A DPHY test port connect to 4L controller 0: A DPHY test port connect to 4L controller. 1: B DPHY test port connect to 4L controller. Value After Reset: 0x0
[30:17]	RESERVED_4	-	
[16]	MIPI_CSI2X2_FIFO_ENABLE	RW	Default bypass mode 0: Bypass mode = non-aggregated mode 1: Aggregated mode Value After Reset: 0x0
[15:13]	RESERVED_3	-	
[12]	MIPI_CSI2X2_FIFO_MODE	RW	Default for aggregation scenario When fifo_enable = 1, that is, when in aggregation mode, this bit is effective. 0: Retiming mode, the alignment operation is completed by the controller, allowing up to 2 cycles of misalignment. 1: Alignment mode. The alignment operation is completed by the PHY's FIFO logic, allowing up to 1 cycle of misalignment. Value After Reset: 0x1
[11:8]	MIPI_CSI2X2_FIFO_HSLANE	RW	Enable 4 lane trans Value After Reset: 0xF
[7:6]	RESERVED_2	-	

Bits	Field Name	Access	Description
[5]	MIPI_CSI2X2_FIFO_ALIGN_OVR	RW	Debug Value After Reset: 0x0
[4]	MIPI_CSI2X2_FIFO_ALIGN_OVR_EN	RW	Debug Value After Reset: 0x0
[3:2]	MIPI_CSI2X2_FIFO_PHASE_OVR	RW	Debug Value After Reset: 0x0
[1]	RESERVED_1	-	
[0]	MIPI_CSI2X2_FIFO_PHASE_OVR_EN	RW	Debug Value After Reset: 0x0

16.3.3.6.6 AXI4_VISYS1_PRI

- Description: AXI4_VISYS1_PRI
- Offset: 0x150
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_6	-	
[30:28]	AXI4_VISYS1_PRIORITY_M1	RW	axi4_visys1_priority_m1 Value After Reset: 0x0
[27]	RESERVED_5	-	
[26:24]	AXI4_VISYS1_PRIORITY_M2	RW	axi4_visys1_priority_m2 Value After Reset: 0x0
[23]	RESERVED_4	-	
[22:20]	AXI4_VISYS1_PRIORITY_M3	RW	axi4_visys1_priority_m3 Value After Reset: 0x0
[19]	RESERVED_3	-	
[18:16]	AXI4_VISYS1_PRIORITY_M4	RW	axi4_visys1_priority_m4 Value After Reset: 0x0
[15]	RESERVED_2	-	
[14:12]	AXI4_VISYS1_PRIORITY_M5	RW	axi4_visys1_priority_m5 Value After Reset: 0x0
[11:1]	RESERVED_1	-	

Bits	Field Name	Access	Description
[0]	AXI4_VISYS1_PRIORITY_S1	RW	axi4_visys1_priority_s1 Value After Reset: 0x0

16.3.3.6.7 AXI4_VISYS2_PRI

- Description: AXI4_VISYS2_PRI
- Offset: 0x154
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_6	-	
[30:28]	AXI4_VISYS2_PRIORITY_M1	RW	axi4_visys2_priority_m1 Value After Reset: 0x0
[27]	RESERVED_5	-	
[26:24]	AXI4_VISYS2_PRIORITY_M2	RW	axi4_visys2_priority_m2 Value After Reset: 0x0
[23]	RESERVED_4	-	
[22:20]	AXI4_VISYS2_PRIORITY_M3	RW	axi4_visys2_priority_m3 Value After Reset: 0x0
[19]	RESERVED_3	-	
[18:16]	AXI4_VISYS2_PRIORITY_M4	RW	axi4_visys2_priority_m4 Value After Reset: 0x0
[15]	RESERVED_2	-	
[14:12]	AXI4_VISYS2_PRIORITY_M5	RW	axi4_visys2_priority_m5 Value After Reset: 0x0
[11:1]	RESERVED_1	-	
[0]	AXI4_VISYS2_PRIORITY_S1	RW	axi4_visys2_priority_s1 Value After Reset: 0x0

16.3.3.6.8 AXI4_VISYS3_PRI

- Description: AXI4_VISYS3_PRI
- Offset: 0x158
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_7	-	
[30:28]	AXI4_VISYS3_PRIORITY_M1	RW	axi4_visys3_priority_m1 Value After Reset: 0x0
[27]	RESERVED_6	-	
[26:24]	AXI4_VISYS3_PRIORITY_M2	RW	axi4_visys3_priority_m2 Value After Reset: 0x0
[23]	RESERVED_5	-	
[22:20]	AXI4_VISYS3_PRIORITY_M3	RW	axi4_visys3_priority_m3 Value After Reset: 0x0
[19]	RESERVED_4	-	
[18:16]	AXI4_VISYS3_PRIORITY_M4	RW	axi4_visys3_priority_m4 Value After Reset: 0x0
[15]	RESERVED_3	-	
[14:12]	AXI4_VISYS3_PRIORITY_M5	RW	axi4_visys3_priority_m5 Value After Reset: 0x0
[11]	RESERVED_2	-	
[10:8]	AXI4_VISYS3_PRIORITY_M6	RW	axi4_visys3_priority_m6 Value After Reset: 0x0
[7:1]	RESERVED_1	-	
[0]	AXI4_VISYS3_PRIORITY_S1	RW	axi4_visys3_priority_s1 Value After Reset: 0x0

16.3.3.6.9 AXI4_VISYS_PRI

- Description: AXI4_VISYS_PRI
- Offset: 0x160
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:30]	RESERVED_6	-	
[29:28]	AXI4_VISYS_PRIORITY_M1	RW	axi4_visys_priority_m1 Value After Reset: 0x0
[27:26]	RESERVED_5	-	

Bits	Field Name	Access	Description
[25:24]	AXI4_VISYS_PRIORITY_M2	RW	axi4_visys_priority_m2 Value After Reset: 0x0
[23:22]	RESERVED_4	-	
[21:20]	AXI4_VISYS_PRIORITY_M3	RW	axi4_visys_priority_m3 Value After Reset: 0x0
[19:18]	RESERVED_3	-	
[17:16]	AXI4_VISYS_PRIORITY_M4	RW	axi4_visys_priority_m4 Value After Reset: 0x0
[15:6]	RESERVED_2	-	
[5:4]	AXI4_VISYS_PRIORITY_S1	RW	axi4_visys_priority_s1 Value After Reset: 0x0
[3:2]	RESERVED_1	-	
[1:0]	AXI4_VISYS_PRIORITY_S2	RW	axi4_visys_priority_s2 Value After Reset: 0x0

16.3.3.6.10 VI_MMU_QOS

- Description: VI_MMU_QOS
- Offset: 0x164
- Default Value: 0xb0b0b0

Bits	Field Name	Access	Description
[31:24]	RESERVED_4	-	
[23:20]	DWMMU_QOS	RW	dwmmu_qos Value After Reset: 0xB
[19:17]	RESERVED_3	-	
[16]	DWMMU_QOS_EN	RW	dwmmu_qos_en 1: Use dwmmu_qos. 0: Use dewarp output qos. Value After Reset: 0x0
[15:12]	ISP1MMU_QOS	RW	isp1mmu_qos Value After Reset: 0xB
[11:9]	RESERVED_2	-	
[8]	ISP1MMU_QOS_EN	RW	isp1mmu_qos_en

Bits	Field Name	Access	Description
			1: Use isp1mmu_qos. 0: Use isp1 output qos. Value After Reset: 0x0
[7:4]	ISP0MMU_QOS	RW	isp0mmu_qos Value After Reset: 0xB
[3:1]	RESERVED_1	-	
[0]	ISP0MMU_QOS_EN	RW	isp0mmu_qos_en 1: Use isp0mmu_qos. 0: Use isp0 output qos. Value After Reset: 0x0

16.3.3.6.11 DEC400_STATUS

- Description: DEC400 idle status
- Offset: 0x16c
- Default Value: 0x7

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	DEC400_DW_IDLE	RO	DEC400 DW idle Value After Reset: 0x1
[1]	DEC400_ISP1_IDLE	RO	DEC400 ISP1 idle Value After Reset: 0x1
[0]	DEC400_ISP0_IDLE	RO	DEC400 ISP0 idle Value After Reset: 0x1

16.3.3.6.12 VI_RSV_REG_0

- Description: Reserved register
- Offset: 0x170
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	VI_RSV_REG_0	RW	Reserved register Value After Reset: 0x0

16.3.3.6.13 VI_VERSION_REG_0

- Description: Version register
- Offset: 0x174
- Default Value: 0x95210426

Bits	Field Name	Access	Description
[31:0]	VI_VERSION	RO	VI version Value After Reset: 0x95210426

16.3.3.6.14 MIPI_CSI2_FPGA

- Description: MIPI_CSI2_FPGA
- Offset: 0x180
- Default Value: 0x120

Bits	Field Name	Access	Description
[31]	MIPI_CSI2_ZCAL_DONE_SYSREG	RO	Just for FPGA Value After Reset: 0x0
[30:9]	RESERVED_3	-	
[8]	MIPI_CSI2_ZCAL_RSTZ_SYSREG	RW	Just for FPGA Value After Reset: 0x1
[7]	RESERVED_2	-	
[6:4]	MIPI_CSI2_GLUEIFTESTER_SYSREG	RW	Just for FPGA Value After Reset: 0x2
[3:2]	RESERVED_1	-	
[1]	MIPI_CSI2_ENABLECLK_RX_SYSREG	RW	Just for FPGA Value After Reset: 0x0
[0]	MIPI_CSI2_CLKEXT_SYSREG	RW	Just for FPGA Value After Reset: 0x0

16.3.3.6.15 MIPI_CSI2X2_FPGA

- Description: MIPI_CSI2X2_FPGA
- Offset: 0x184
- Default Value: 0x1200120

Bits	Field Name	Access	Description
[31]	MIPI_CSI2X2_L4_2_ZCAL_DONE_SYSREG	RO	Just for FPGA

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[30:25]	RESERVED_6	-	
[24]	MIPI_CSI2X2_L4_2_ZCAL_RSTZ_SYSREG	RW	Just for FPGA Value After Reset: 0x1
[23:22]	RESERVED_5	-	
[21:20]	MIPI_CSI2X2_L4_2_GLUEIFTESTER_SYSREG	RW	Just for FPGA Value After Reset: 0x2
[19:18]	RESERVED_4	-	
[17]	MIPI_CSI2X2_L4_2_ENABLECLK_RX_SYSREG	RW	Just for FPGA Value After Reset: 0x0
[16]	MIPI_CSI2X2_L4_2_CLKEXT_SYSREG	RW	Just for FPGA Value After Reset: 0x0
[15]	MIPI_CSI2X2_L4_1_ZCAL_DONE_SYSREG	RO	Just for FPGA Value After Reset: 0x0
[14:9]	RESERVED_3	-	
[8]	MIPI_CSI2X2_L4_1_ZCAL_RSTZ_SYSREG	RW	Just for FPGA Value After Reset: 0x1
[7]	RESERVED_2	-	
[6:4]	MIPI_CSI2X2_L4_1_GLUEIFTESTER_SYSREG	RW	Just for FPGA Value After Reset: 0x2
[3:2]	RESERVED_1	-	
[1]	MIPI_CSI2X2_L4_1_ENABLECLK_RX_SYSREG	RW	Just for FPGA Value After Reset: 0x0
[0]	MIPI_CSI2X2_L4_1_CLKEXT_SYSREG	RW	Just for FPGA Value After Reset: 0x0

16.3.3.6.16 DSP0_CPU_INT_MASK

- Description: DSP0_CPU_INT_MASK
- Offset: 0x190
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3:0]	DSP0_CPU_INT_MASK	RW	Mask DSP0 to CPU interrupt, 1: Mask interrupt. Value After Reset: 0x0

16.3.3.6.17 DSP0_CPU_INT_CLR

- Description: DSP0_CPU_INT_CLR
- Offset: 0x194
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSP0_CPU_INT_CLR3	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[2]	DSP0_CPU_INT_CLR2	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[1]	DSP0_CPU_INT_CLR1	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[0]	DSP0_CPU_INT_CLR0	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0

16.3.3.6.18 DSP0_CPU_INT_STA

- Description: DSP0_CPU_INT_STA
- Offset: 0x198
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSP0_CPU_INT_STA3	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP0. Value After Reset: 0x0
[2]	DSP0_CPU_INT_STA2	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP1. Value After Reset: 0x0
[1]	DSP0_CPU_INT_STA1	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP2.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[0]	DSP0_CPU_INT_STA0	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP3. Value After Reset: 0x0

16.3.3.6.19 DSP1_CPU_INT_MASK

- Description: DSP1_CPU_INT_MASK
- Offset: 0x1a0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3:0]	DSP1_CPU_INT_MASK	RW	Mask DSP1 to CPU interrupt, 1: Mask interrupt. Value After Reset: 0x0

16.3.3.6.20 DSP1_CPU_INT_CLR

- Description: DSP1_CPU_INT_CLR
- Offset: 0x1a4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSP1_CPU_INT_CLR3	W1S	Clear DSP1 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[2]	DSP1_CPU_INT_CLR2	W1S	Clear DSP1 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[1]	DSP1_CPU_INT_CLR1	W1S	Clear DSP1 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[0]	DSP1_CPU_INT_CLR0	W1S	Clear DSP1 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0

16.3.3.6.21 DSP1_CPU_INT_STA

- Description: DSP1_CPU_INT_STA
- Offset: 0x1a8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSP1_CPU_INT_STA3	W1S	DSP 1 to CPU interrupt status, 1 means interrupt. It's set by DSP1. Value After Reset: 0x0
[2]	DSP1_CPU_INT_STA2	W1S	DSP 1 to CPU interrupt status, 1 means interrupt. It's set by DSP2. Value After Reset: 0x0
[1]	DSP1_CPU_INT_STA1	W1S	DSP 1 to CPU interrupt status, 1 means interrupt. It's set by DSP3. Value After Reset: 0x0
[0]	DSP1_CPU_INT_STA0	W1S	DSP 1 to CPU interrupt status, 1 means interrupt. It's set by DSP 4. Value After Reset: 0x0

16.3.3.6.22 CPU_DSP0_INT_MASK

- Description: CPU_DSP0_INT_MASK
- Offset: 0x1b0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3:0]	CPU_DSP0_INT_MASK	RW	Mask CPU to DSP0 interrupt, 1: Mask interrupt. Value After Reset: 0x0

16.3.3.6.23 CPU_DSP0_INT_CLR

- Description: CPU_DSP0_INT_CLR
- Offset: 0x1b4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	CPU_DSP0_INT_CLR3	W1S	Clear CPU to DSP0 interrupt, 1: Clear interrupt. Value After Reset: 0x0
[2]	CPU_DSP0_INT_CLR2	W1S	Clear CPU to DSP0 interrupt, 1: Clear interrupt. Value After Reset: 0x0

Bits	Field Name	Access	Description
[1]	CPU_DSP0_INT_CLR1	W1S	Clear CPU to DSP0 interrupt, 1: Clear interrupt. Value After Reset: 0x0
[0]	CPU_DSP0_INT_CLR0	W1S	Clear CPU to DSP0 interrupt, 1: Clear interrupt. Value After Reset: 0x0

16.3.3.6.24 CPU_DSP0_INT_STA

- Description: CPU_DSP0_INT_STA
- Offset: 0x1b8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	CPU_DSP0_INT_STA3	W1S	CPU to DSP0 interrupt status, 1 means interrupt. It's set by CPU. Value After Reset: 0x0
[2]	CPU_DSP0_INT_STA2	W1S	CPU to DSP0 interrupt status, 2 means interrupt. It's set by CPU. Value After Reset: 0x0
[1]	CPU_DSP0_INT_STA1	W1S	CPU to DSP0 interrupt status, 3 means interrupt. It's set by CPU. Value After Reset: 0x0
[0]	CPU_DSP0_INT_STA0	W1S	CPU to DSP0 interrupt status, 4 means interrupt. It's set by CPU. Value After Reset: 0x0

16.3.3.6.25 CPU_DSP1_INT_MASK

- Description: CPU_DSP1_INT_MASK
- Offset: 0x1c0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3:0]	CPU_DSP1_INT_MASK	RW	Mask CPU to DSP1 interrupt, 1: Mask interrupt. Value After Reset: 0x0

16.3.3.6.26 CPU_DSP1_INT_CLR

- Description: CPU_DSP1_INT_CLR
- Offset: 0x1c4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	CPU_DSP1_INT_CLR3	W1S	Clear CPU to DSP1 interrupt, 1: Clear interrupt. Value After Reset: 0x0
[2]	CPU_DSP1_INT_CLR2	W1S	Clear CPU to DSP1 interrupt, 1: Clear interrupt. Value After Reset: 0x0
[1]	CPU_DSP1_INT_CLR1	W1S	Clear CPU to DSP1 interrupt, 1: Clear interrupt. Value After Reset: 0x0
[0]	CPU_DSP1_INT_CLR0	W1S	Clear CPU to DSP1 interrupt, 1: Clear interrupt. Value After Reset: 0x0

16.3.3.6.27 CPU_DSP1_INT_STA

- Description: CPU_DSP1_INT_STA
- Offset: 0x1c8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	CPU_DSP1_INT_STA3	W1S	CPU to DSP1 interrupt status, 1 means interrupt. It's set by CPU. Value After Reset: 0x0
[2]	CPU_DSP1_INT_STA2	W1S	CPU to DSP1 interrupt status, 2 means interrupt. It's set by CPU. Value After Reset: 0x0
[1]	CPU_DSP1_INT_STA1	W1S	CPU to DSP1 interrupt status, 3 means interrupt. It's set by CPU. Value After Reset: 0x0
[0]	CPU_DSP1_INT_STA0	W1S	CPU to DSP1 interrupt status, 4 means interrupt. It's set by CPU. Value After Reset: 0x0

16.3.3.6.28 DSP0_DSP1_INT_MASK

- Description: DSP0_DSP1_INT_MASK
- Offset: 0x1d0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3:0]	DSP0_DSP1_INT_MASK	RW	Mask DSP0 to CPU interrupt, 1: Mask interrupt. Value After Reset: 0x0

16.3.3.6.29 DSP0_DSP1_INT_CLR

- Description: DSP0_DSP1_INT_CLR
- Offset: 0x1d4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSP0_DSP1_INT_CLR3	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[2]	DSP0_DSP1_INT_CLR2	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[1]	DSP0_DSP1_INT_CLR1	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[0]	DSP0_DSP1_INT_CLR0	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0

16.3.3.6.30 DSP0_DSP1_INT_STA

- Description: DSP0_DSP1_INT_STA
- Offset: 0x1d8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSP0_DSP1_INT_STA3	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP0. Value After Reset: 0x0

Bits	Field Name	Access	Description
[2]	DSP0_DSP1_INT_STA2	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP1. Value After Reset: 0x0
[1]	DSP0_DSP1_INT_STA1	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP2. Value After Reset: 0x0
[0]	DSP0_DSP1_INT_STA0	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP3. Value After Reset: 0x0

16.3.3.6.31 DSP1_DSP0_INT_MASK

- Description: DSP1_DSP0_INT_MASK
- Offset: 0x1e0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3:0]	DSP1_DSP0_INT_MASK	RW	Mask DSP0 to CPU interrupt, 1: Mask interrupt. Value After Reset: 0x0

16.3.3.6.32 DSP1_DSP0_INT_CLR

- Description: DSP1_DSP0_INT_CLR
- Offset: 0x1e4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSP1_DSP0_INT_CLR3	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[2]	DSP1_DSP0_INT_CLR2	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[1]	DSP1_DSP0_INT_CLR1	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[0]	DSP1_DSP0_INT_CLR0	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0

16.3.3.6.33 DSP1_DSP0_INT_STA

- Description: DSP1_DSP0_INT_STA
- Offset: 0x1e8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSP1_DSP0_INT_STA3	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP0. Value After Reset: 0x0
[2]	DSP1_DSP0_INT_STA2	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP1. Value After Reset: 0x0
[1]	DSP1_DSP0_INT_STA1	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP2. Value After Reset: 0x0
[0]	DSP1_DSP0_INT_STA0	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP3. Value After Reset: 0x0

16.3.3.6.34 DSP0_INT_STA

- Description: DSP0_INT_STA
- Offset: 0x1f0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	CPU_DSP0_INT_STA	RO	CPU to DSP0 interrupt state Value After Reset: 0x0
[0]	DSP1_DSP0_INT_STA	RO	DSP1 to DSP0 interrupt state Value After Reset: 0x0

16.3.3.6.35 DSP1_INT_STA

- Description: DSP1_INT_STA
- Offset: 0x1f4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	CPU_DSP1_INT_STA	RO	CPU to DSP1 interrupt state Value After Reset: 0x0
[0]	DSP0_DSP1_INT_STA	RO	DSP0 to DSP1 interrupt state Value After Reset: 0x0

16.3.3.6.36 VISYS_CONTROL_TEE

- Description: VISYS_CONTROL
- Offset: 0x1120
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:30]	RESERVED_6	-	
[29]	VIPRE_REMAP_EN	RW	vipre_remap_en, not used, need to set 0. Value After Reset: 0x0
[28]	VIPRE_RANK_SEL	RW	vipre_rank_sel, not used. Value After Reset: 0x0
[27:26]	RESERVED_5	-	
[25]	DW200_REMAP_EN	RW	dw200_remap_en, address remap enable when MMU is off, acitve high. Value After Reset: 0x0
[24]	DW200_RANK_SEL	RW	dw200_rank_sel 0: Original address to DDR. 1: Original address would add 0x1_0000_0000 to DDR. Value After Reset: 0x0
[23:22]	RESERVED_4	-	
[21]	ISP1_REMAP_EN	RW	isp1_remap_en, address remap enable when MMU is off, acitve high. Value After Reset: 0x0
[20]	ISP1_RANK_SEL	RW	isp1_rank_sel 0: Original address to DDR. 1: Original address would add 0x1_0000_0000 to DDR. Value After Reset: 0x0
[19:18]	RESERVED_3	-	

Bits	Field Name	Access	Description
[17]	ISP0_REMAP_EN	RW	isp0_remap_en, address remap enable when MMU is off, active high. Value After Reset: 0x0
[16]	ISP0_RANK_SEL	RW	isp0_rank_sel 0: Original address to DDR. 1: Original address would add 0x1_0000_0000 to DDR. Value After Reset: 0x0
[15:9]	RESERVED_2	-	
[8]	ISP_VENC_SHAKE_CHANNEL_SEL	RW	0: Monitor vi2ddr channel_x000D_. 1: Monitor vi2sram channel. Value After Reset: 0x0
[7:3]	RESERVED_1	-	
[2]	ISP_RY_DISABLE_ISP_0	RW	Disable ISP RY, 1 means disable. Value After Reset: 0x0
[1]	ISP1_DISABLE_ISP_0	RW	Disable ISP1, 1 means disable. Value After Reset: 0x0
[0]	ISP0_DISABLE_ISP_0	RW	Disable ISP0, 1 means disable. Value After Reset: 0x0

16.3.3.6.37 MIPI_CSI0_CTRL_TEE

- Description: MIPI_CSI0_CTRL
- Offset: 0x1140
- Default Value: 0x10010a1c

Bits	Field Name	Access	Description
[31:29]	RESERVED_6	-	
[28]	MIPI_CSI2_BASEDIR_0	RW	1: lane0 RX, 0: lane0 TX Configures the base direction for CSI2-DPHY lane. Value After Reset: 0x1
[27:26]	RESERVED_5	-	
[25]	MIPI_CSI2_FORCERXMODE_0	RW	1: Force lane0 to receive control mode and wait stop state. Value After Reset: 0x0
[24]	MIPI_CSI2_TURNDISABLE_0	RW	1: Prohibit turnaround.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[23]	RESERVED_4	-	
[22]	MIPI_CSI2_FORCERXMODE_1	RW	1: Force lane1 to receive control mode and wait stop state. Value After Reset: 0x0
[21]	MIPI_CSI2_FORCERXMODE_2	RW	1: Force lane2 to receive control mode and wait stop state. Value After Reset: 0x0
[20]	MIPI_CSI2_FORCERXMODE_3	RW	1: Force lane3 to receive control mode and wait stop state. Value After Reset: 0x0
[19:17]	RESERVED_3	-	
[16]	MIPI_CSI2_ENABLECLK	RW	When Shutdownz=rstz=0, set 1 clock to enable PPI, or 0: turn off all PPI reception. Value After Reset: 0x1
[15]	RESERVED_2	-	
[14:8]	MIPI_CSI2_HSFREQRANGE	RW	High speed frequency range selection, default 1Gbps range. Value After Reset: 0xA
[7:6]	RESERVED_1	-	
[5:0]	MIPI_CSI2_CFGCLKFREQRANGE	RW	Round (Fcfg_clk(MHz) - 17)*4, default 28. Value After Reset: 0x1C

16.3.3.6.38 MIPI_CSI1_CTRL_TEE

- Description: MIPI_CSI1_CTRL
- Offset: 0x1144
- Default Value: 0x10010a1c

Bits	Field Name	Access	Description
[31:29]	RESERVED_6	-	
[28]	MIPI_CSI2X2_A_BASEDIR_0	RW	1: lane0 RX, 0: lane0 TX Configures the base direction for BPHY lane. Value After Reset: 0x1
[27:26]	RESERVED_5	-	

Bits	Field Name	Access	Description
[25]	MIPI_CSI2X2_A_FORCERXMODE_0	RW	1: Force APHY lane0 to receive control mode and wait stop state. Value After Reset: 0x0
[24]	MIPI_CSI2X2_A_TURNDISABLE_0	RW	1: Prohibit turnaround. Value After Reset: 0x0
[23]	RESERVED_4	-	
[22]	MIPI_CSI2X2_A_FORCERXMODE_1	RW	1: Force APHY lane1 to receive control mode and wait stop state. Value After Reset: 0x0
[21:17]	RESERVED_3	-	
[16]	MIPI_CSI2X2_A_ENABLECLK	RW	When Shutdownz = rstz = 0, set 1 clock to enable PPI, or 0: turn off all PPI reception. Value After Reset: 0x1
[15]	RESERVED_2	-	
[14:8]	MIPI_CSI2X2_A_HSFREQRANGE	RW	High speed frequency range selection, default 1Gbps range. Value After Reset: 0xA
[7:6]	RESERVED_1	-	
[5:0]	MIPI_CSI2X2_A_CFGCLKFREQRANGE	RW	Round (Fcfg_clk(MHz) - 17)*4, default 28. Value After Reset: 0x1C

16.3.3.6.39 MIPI_CSI2_CTRL_TEE

- Description: MIPI_CSI2_CTRL
- Offset: 0x1148
- Default Value: 0x10010a1c

Bits	Field Name	Access	Description
[31:29]	RESERVED_6	-	
[28]	MIPI_CSI2X2_B_BASEDIR_0	RW	1: lane0 RX, 0:lane0 TX Configures the base direction for BPHY lane. Value After Reset: 0x1
[27:26]	RESERVED_5	-	
[25]	MIPI_CSI2X2_B_FORCERXMODE_0	RW	1: Force BPHY lane0 to receive control mode and wait stop state.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[24]	MIPI_CSI2X2_B_TURNDISABLE_0	RW	1: Prohibit turnaround. Value After Reset: 0x0
[23]	RESERVED_4	-	
[22]	MIPI_CSI2X2_B_FORCERXMODE_1	RW	1: Force BPHY lane1 to receive control mode and wait stop state. Value After Reset: 0x0
[21:17]	RESERVED_3	-	
[16]	MIPI_CSI2X2_B_ENABLECLK	RW	When Shutdownz = rstz = 0, set 1 clock to enable PPI, or 0: Turn off all PPI reception. Value After Reset: 0x1
[15]	RESERVED_2	-	
[14:8]	MIPI_CSI2X2_B_HSFREQRANGE	RW	High speed frequency range selection, default 1Gbps range. Value After Reset: 0xA
[7:6]	RESERVED_1	-	
[5:0]	MIPI_CSI2X2_B_CFGCLKFREQRANGE	RW	Round (Fcfg_clk(MHz) - 17)*4, default 28. Value After Reset: 0x1C

16.3.3.6.40 MIPI_CSI_FIFO_CTRL_TEE

- Description: MIPI_CSI_FIFO_CTRL
- Offset: 0x114C
- Default Value: 0x1f00

Bits	Field Name	Access	Description
[31]	MIPI_CSI2X2_A_ENABLE	RW	Default A DPHY test port connect to 4L controller 0: A DPHY test port connect to 4L controller. 1: B DPHY test port connect to 4L controller. Value After Reset: 0x0
[30:17]	RESERVED_4	-	
[16]	MIPI_CSI2X2_FIFO_ENABLE	RW	Default bypass mode 0: Bypass mode = non-aggregated mode 1: Aggregated mode Value After Reset: 0x0

Bits	Field Name	Access	Description
[15:13]	RESERVED_3	-	
[12]	MIPI_CSI2X2_FIFO_MODE	RW	Default for aggregation scenario When fifo_enable = 1, that is, when in aggregation mode, this bit is effective. 0: Retiming mode, the alignment operation is completed by the controller, allowing up to 2 cycles of misalignment. 1: Alignment mode. The alignment operation is completed by the PHY's FIFO logic, allowing up to 1 cycle of misalignment. Value After Reset: 0x1
[11:8]	MIPI_CSI2X2_FIFO_HSLANE	RW	Enable 4 lane trans. Value After Reset: 0xF
[7:6]	RESERVED_2	-	
[5]	MIPI_CSI2X2_FIFO_ALIGN_OVR	RW	Debug Value After Reset: 0x0
[4]	MIPI_CSI2X2_FIFO_ALIGN_OVR_EN	RW	Debug Value After Reset: 0x0
[3:2]	MIPI_CSI2X2_FIFO_PHASE_OVR	RW	Debug Value After Reset: 0x0
[1]	RESERVED_1	-	
[0]	MIPI_CSI2X2_FIFO_PHASE_OVR_EN	RW	Debug Value After Reset: 0x0

16.3.3.6.41 AXI4_VISYS1_PRI_TEE

- Description: AXI4_VISYS1_PRI
- Offset: 0x1150
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_6	-	
[30:28]	AXI4_VISYS1_PRIORITY_M1	RW	axi4_visys1_priority_m1 Value After Reset: 0x0
[27]	RESERVED_5	-	

Bits	Field Name	Access	Description
[26:24]	AXI4_VISYS1_PRIORITY_M2	RW	axi4_visys1_priority_m2 Value After Reset: 0x0
[23]	RESERVED_4	-	
[22:20]	AXI4_VISYS1_PRIORITY_M3	RW	axi4_visys1_priority_m3 Value After Reset: 0x0
[19]	RESERVED_3	-	
[18:16]	AXI4_VISYS1_PRIORITY_M4	RW	axi4_visys1_priority_m4 Value After Reset: 0x0
[15]	RESERVED_2	-	
[14:12]	AXI4_VISYS1_PRIORITY_M5	RW	axi4_visys1_priority_m5 Value After Reset: 0x0
[11:1]	RESERVED_1	-	
[0]	AXI4_VISYS1_PRIORITY_S1	RW	axi4_visys1_priority_s1 Value After Reset: 0x0

16.3.3.6.42 AXI4_VISYS2_PRI_TEE

- Description: AXI4_VISYS2_PRI
- Offset: 0x1154
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_6	-	
[30:28]	AXI4_VISYS2_PRIORITY_M1	RW	axi4_visys2_priority_m1 Value After Reset: 0x0
[27]	RESERVED_5	-	
[26:24]	AXI4_VISYS2_PRIORITY_M2	RW	axi4_visys2_priority_m2 Value After Reset: 0x0
[23]	RESERVED_4	-	
[22:20]	AXI4_VISYS2_PRIORITY_M3	RW	axi4_visys2_priority_m3 Value After Reset: 0x0
[19]	RESERVED_3	-	
[18:16]	AXI4_VISYS2_PRIORITY_M4	RW	axi4_visys2_priority_m4

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[15]	RESERVED_2	-	
[14:12]	AXI4_VISYS2_PRIORITY_M5	RW	axi4_visys2_priority_m5 Value After Reset: 0x0
[11:1]	RESERVED_1	-	
[0]	AXI4_VISYS2_PRIORITY_S1	RW	axi4_visys2_priority_s1 Value After Reset: 0x0

16.3.3.6.43 AXI4_VISYS3_PRI_TEE

- Description: AXI4_VISYS3_PRI
- Offset: 0x1158
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_7	-	
[30:28]	AXI4_VISYS3_PRIORITY_M1	RW	axi4_visys3_priority_m1 Value After Reset: 0x0
[27]	RESERVED_6	-	
[26:24]	AXI4_VISYS3_PRIORITY_M2	RW	axi4_visys3_priority_m2 Value After Reset: 0x0
[23]	RESERVED_5	-	
[22:20]	AXI4_VISYS3_PRIORITY_M3	RW	axi4_visys3_priority_m3 Value After Reset: 0x0
[19]	RESERVED_4	-	
[18:16]	AXI4_VISYS3_PRIORITY_M4	RW	axi4_visys3_priority_m4 Value After Reset: 0x0
[15]	RESERVED_3	-	
[14:12]	AXI4_VISYS3_PRIORITY_M5	RW	axi4_visys3_priority_m5 Value After Reset: 0x0
[11]	RESERVED_2	-	
[10:8]	AXI4_VISYS3_PRIORITY_M6	RW	axi4_visys3_priority_m6 Value After Reset: 0x0

Bits	Field Name	Access	Description
[7:1]	RESERVED_1	-	
[0]	AXI4_VISYS3_PRIORITY_S1	RW	axi4_visys3_priority_s1 Value After Reset: 0x0

16.3.3.6.44 AXI4_VISYS_PRI_TEE

- Description: AXI4_VISYS_PRI
- Offset: 0x1160
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:30]	RESERVED_6	-	
[29:28]	AXI4_VISYS_PRIORITY_M1	RW	axi4_visys_priority_m1 Value After Reset: 0x0
[27:26]	RESERVED_5	-	
[25:24]	AXI4_VISYS_PRIORITY_M2	RW	axi4_visys_priority_m2 Value After Reset: 0x0
[23:22]	RESERVED_4	-	
[21:20]	AXI4_VISYS_PRIORITY_M3	RW	axi4_visys_priority_m3 Value After Reset: 0x0
[19:18]	RESERVED_3	-	
[17:16]	AXI4_VISYS_PRIORITY_M4	RW	axi4_visys_priority_m4 Value After Reset: 0x0
[15:6]	RESERVED_2	-	
[5:4]	AXI4_VISYS_PRIORITY_S1	RW	axi4_visys_priority_s1 Value After Reset: 0x0
[3:2]	RESERVED_1	-	
[1:0]	AXI4_VISYS_PRIORITY_S2	RW	axi4_visys_priority_s2 Value After Reset: 0x0

16.3.3.6.45 VI_MMU_QOS_TEE

- Description: VI_MMU_QOS
- Offset: 0x1164
- Default Value: 0xb0b0b0

Bits	Field Name	Access	Description
[31:24]	RESERVED_4	-	
[23:20]	DWMMU_QOS	RW	dwmmu_qos Value After Reset: 0xB
[19:17]	RESERVED_3	-	
[16]	DWMMU_QOS_EN	RW	dwmmu_qos_en Value After Reset: 0x0
[15:12]	ISP1MMU_QOS	RW	isp1mmu_qos Value After Reset: 0xB
[11:9]	RESERVED_2	-	
[8]	ISP1MMU_QOS_EN	RW	isp1mmu_qos_en Value After Reset: 0x0
[7:4]	ISP0MMU_QOS	RW	isp0mmu_qos Value After Reset: 0xB
[3:1]	RESERVED_1	-	
[0]	ISP0MMU_QOS_EN	RW	isp0mmu_qos_en Value After Reset: 0x0

16.3.3.6.46 VI_RSV_REG_0_TEE

- Description: Reserved register
- Offset: 0x1170
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	VI_RSV_REG_0	RW	reserved Value After Reset: 0x0

16.3.3.6.47 DSP0_CPU_INT_MASK_TEE

- Description: DSP0_CPU_INT_MASK
- Offset: 0x1190
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3:0]	DSP0_CPU_INT_MASK	RW	Mask DSP0 to CPU interrupt, 1: Mask interrupt.

Bits	Field Name	Access	Description
			Value After Reset: 0x0

16.3.3.6.48 DSP0_CPU_INT_CLR_TEE

- Description: DSP0_CPU_INT_CLR
- Offset: 0x1194
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSP0_CPU_INT_CLR3_TEE	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[2]	DSP0_CPU_INT_CLR2_TEE	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[1]	DSP0_CPU_INT_CLR1_TEE	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[0]	DSP0_CPU_INT_CLR0_TEE	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0

16.3.3.6.49 DSP0_CPU_INT_STA_TEE

- Description: DSP0_CPU_INT_STA
- Offset: 0x1198
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSP0_CPU_INT_STA3	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP0. Value After Reset: 0x0
[2]	DSP0_CPU_INT_STA2	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP1. Value After Reset: 0x0
[1]	DSP0_CPU_INT_STA1	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP2. Value After Reset: 0x0
[0]	DSP0_CPU_INT_STA0	W1S	DSP0 to CPU interrupt status, 1 means interrupt.

Bits	Field Name	Access	Description
			It's set by DSP3. Value After Reset: 0x0

16.3.3.6.50 DSP1_CPU_INT_MASK_TEE

- Description: DSP1_CPU_INT_MASK
- Offset: 0x11a0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3:0]	DSP1_CPU_INT_MASK	RW	Mask DSP10 to CPU interrupt, 1: Mask interrupt. Value After Reset: 0x0

16.3.3.6.51 DSP1_CPU_INT_CLR_TEE

- Description: DSP1_CPU_INT_CLR
- Offset: 0x11a4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSP1_CPU_INT_CLR3_TEE	W1S	Clear DSP1 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[2]	DSP1_CPU_INT_CLR2_TEE	W1S	Clear DSP1 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[1]	DSP1_CPU_INT_CLR1_TEE	W1S	Clear DSP1 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[0]	DSP1_CPU_INT_CLR0_TEE	W1S	Clear DSP1 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0

16.3.3.6.52 DSP1_CPU_INT_STA_TEE

- Description: DSP1_CPU_INT_STA
- Offset: 0x11a8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	

Bits	Field Name	Access	Description
[3]	DSP1_CPU_INT_STA3	W1S	DSP1 to CPU interrupt status, 1 means interrupt. It's set by DSP1. Value After Reset: 0x0
[2]	DSP1_CPU_INT_STA2	W1S	DSP1 to CPU interrupt status, 1 means interrupt. It's set by DSP2. Value After Reset: 0x0
[1]	DSP1_CPU_INT_STA1	W1S	DSP1 to CPU interrupt status, 1 means interrupt. It's set by DSP3. Value After Reset: 0x0
[0]	DSP1_CPU_INT_STA0	W1S	DSP1 to CPU interrupt status, 1 means interrupt. It's set by DSP4. Value After Reset: 0x0

16.3.3.6.53 CPU_DSP0_INT_MASK_TEE

- Description: CPU_DSP0_INT_MASK
- Offset: 0x11b0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3:0]	CPU_DSP0_INT_MASK	RW	Mask CPU to DSP0 interrupt, 1: Mask interrupt. Value After Reset: 0x0

16.3.3.6.54 CPU_DSP0_INT_CLR_TEE

- Description: CPU_DSP0_INT_CLR
- Offset: 0x11b4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	CPU_DSP0_INT_CLR3_TEE	W1S	Clear CPU to DSP0 interrupt, 1: Clear interrupt. Value After Reset: 0x0
[2]	CPU_DSP0_INT_CLR2_TEE	W1S	Clear CPU to DSP0 interrupt, 1: Clear interrupt. Value After Reset: 0x0
[1]	CPU_DSP0_INT_CLR1_TEE	W1S	Clear CPU to DSP0 interrupt, 1: Clear interrupt.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[0]	CPU_DSP0_INT_CLR0_TEE	W1S	Clear CPU to DSP0 interrupt, 1: Clear interrupt. Value After Reset: 0x0

16.3.3.6.55 CPU_DSP0_INT_STA_TEE

- Description: CPU_DSP0_INT_STA
- Offset: 0x11b8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	CPU_DSP0_INT_STA3	W1S	CPU to DSP0 interrupt status, 1 means interrupt. It's set by CPU. Value After Reset: 0x0
[2]	CPU_DSP0_INT_STA2	W1S	CPU to DSP0 interrupt status, 2 means interrupt. It's set by CPU. Value After Reset: 0x0
[1]	CPU_DSP0_INT_STA1	W1S	CPU to DSP0 interrupt status, 3 means interrupt. It's set by CPU. Value After Reset: 0x0
[0]	CPU_DSP0_INT_STA0	W1S	CPU to DSP0 interrupt status, 4 means interrupt. It's set by CPU. Value After Reset: 0x0

16.3.3.6.56 CPU_DSP1_INT_MASK_TEE

- Description: CPU_DSP1_INT_MASK
- Offset: 0x11c0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3:0]	CPU_DSP1_INT_MASK	RW	Mask CPU to DSP1 interrupt, 1: Mask interrupt. Value After Reset: 0x0

16.3.3.6.57 CPU_DSP1_INT_CLR_TEE

- Description: CPU_DSP1_INT_CLR
- Offset: 0x11c4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	CPU_DSP1_INT_CLR3_TEE	W1S	Clear CPU to DSP1 interrupt, 1: Clear interrupt. Value After Reset: 0x0
[2]	CPU_DSP1_INT_CLR2_TEE	W1S	Clear CPU to DSP1 interrupt, 1: Clear interrupt. Value After Reset: 0x0
[1]	CPU_DSP1_INT_CLR1_TEE	W1S	Clear CPU to DSP1 interrupt, 1: Clear interrupt. Value After Reset: 0x0
[0]	CPU_DSP1_INT_CLR0_TEE	W1S	Clear CPU to DSP1 interrupt, 1: Clear interrupt. Value After Reset: 0x0

16.3.3.6.58 CPU_DSP1_INT_STA_TEE

- Description: CPU_DSP1_INT_STA
- Offset: 0x11c8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	CPU_DSP1_INT_STA3	W1S	CPU to DSP1 interrupt status, 1 means interrupt. It's set by CPU. Value After Reset: 0x0
[2]	CPU_DSP1_INT_STA2	W1S	CPU to DSP1 interrupt status, 2 means interrupt. It's set by CPU. Value After Reset: 0x0
[1]	CPU_DSP1_INT_STA1	W1S	CPU to DSP1 interrupt status, 3 means interrupt. It's set by CPU. Value After Reset: 0x0
[0]	CPU_DSP1_INT_STA0	W1S	CPU to DSP1 interrupt status, 4 means interrupt. It's set by CPU. Value After Reset: 0x0

16.3.3.6.59 DSP0_DSP1_INT_MASK_TEE

- Description: DSP0_DSP1_INT_MASK
- Offset: 0x11d0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3:0]	DSP0_DSP1_INT_MASK	RW	Mask DSP0 to CPU interrupt, 1: Mask interrupt. Value After Reset: 0x0

16.3.3.6.60 DSP0_DSP1_INT_CLR_TEE

- Description: DSP0_DSP1_INT_CLR
- Offset: 0x11d4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSP0_DSP1_INT_CLR3_TEE	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[2]	DSP0_DSP1_INT_CLR2_TEE	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[1]	DSP0_DSP1_INT_CLR1_TEE	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[0]	DSP0_DSP1_INT_CLR0_TEE	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0

16.3.3.6.61 DSP0_DSP1_INT_STA_TEE

- Description: DSP0_DSP1_INT_STA
- Offset: 0x11d8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSP0_DSP1_INT_STA3	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP0. Value After Reset: 0x0

Bits	Field Name	Access	Description
[2]	DSP0_DSP1_INT_STA2	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP1. Value After Reset: 0x0
[1]	DSP0_DSP1_INT_STA1	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP2. Value After Reset: 0x0
[0]	DSP0_DSP1_INT_STA0	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP3. Value After Reset: 0x0

16.3.3.6.62 DSP1_DSP0_INT_MASK_TEE

- Description: DSP1_DSP0_INT_MASK
- Offset: 0x11e0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3:0]	DSP1_DSP0_INT_MASK	RW	Mask DSP0 to CPU interrupt, 1: Mask interrupt. Value After Reset: 0x0

16.3.3.6.63 DSP1_DSP0_INT_CLR_TEE

- Description: DSP1_DSP0_INT_CLR
- Offset: 0x11e4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSP1_DSP0_INT_CLR3_TEE	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[2]	DSP1_DSP0_INT_CLR2_TEE	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[1]	DSP1_DSP0_INT_CLR1_TEE	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0
[0]	DSP1_DSP0_INT_CLR0_TEE	W1S	Clear DSP0 to CPU interrupt, 1: Clear interrupt. Value After Reset: 0x0

16.3.3.6.64 DSP1_DSP0_INT_STA_TEE

- Description: DSP1_DSP0_INT_STA
- Offset: 0x11e8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DSP1_DSP0_INT_STA3	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP0. Value After Reset: 0x0
[2]	DSP1_DSP0_INT_STA2	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP1. Value After Reset: 0x0
[1]	DSP1_DSP0_INT_STA1	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP2. Value After Reset: 0x0
[0]	DSP1_DSP0_INT_STA0	W1S	DSP0 to CPU interrupt status, 1 means interrupt. It's set by DSP3. Value After Reset: 0x0

16.3.3.6.65 CFG_FUNC_LOCK_TEE

- Description: VI function registers TEE lock
- Offset: 0x1220
- Default Value: 0x0

Bits	Field Name	Access	Description
[31]	RESERVED_4	-	
[30]	VI_SUBSYS_FUNCCFG_LOCK	RW	vi_subsys_funccfg_lock Value After Reset: 0x0
[29]	VI_SUBSYS1_FUNCCFG_LOCK	RW	vi_subsys1_funccfg_lock Value After Reset: 0x0
[28]	VI_SUBSYS2_FUNCCFG_LOCK	RW	vi_subsys2_funccfg_lock Value After Reset: 0x0
[27]	VI_SUBSYS3_FUNCCFG_LOCK	RW	vi_subsys3_funccfg_lock Value After Reset: 0x0

Bits	Field Name	Access	Description
[26:24]	RESERVED_3	-	
[23]	VIPRE_ADDRMAP_LOCK	RW	vipre_addrmap_lock Value After Reset: 0x0
[22]	DW200_ADDRMAP_LOCK	RW	dw200_addrmap_lock Value After Reset: 0x0
[21]	ISP1_ADDRMAP_LOCK	RW	isp1_addrmap_lock Value After Reset: 0x0
[20]	ISP0_ADDRMAP_LOCK	RW	isp0_addrmap_lock Value After Reset: 0x0
[19]	RESERVED_2	-	
[18]	ISP0_FUNCCFG_LOCK	RW	isp0_funccfg_lock Value After Reset: 0x0
[17]	ISP1_FUNCCFG_LOCK	RW	isp1_funccfg_lock Value After Reset: 0x0
[16]	ISP_RY_FUNCCFG_LOCK	RW	isp_ry_funccfg_lock Value After Reset: 0x0
[15]	MIPI_CSI2X2_FIFO_FUNCCFG_LOCK	RW	mipi_csi2x2_fifo_funccfg_lock Value After Reset: 0x0
[14]	MIPI_CSI0_FUNCCFG_LOCK	RW	mipi_csi0_funccfg_lock Value After Reset: 0x0
[13]	MIPI_CSI1_FUNCCFG_LOCK	RW	mipi_csi1_funccfg_lock Value After Reset: 0x0
[12]	MIPI_CSI2_FUNCCFG_LOCK	RW	mipi_csi2_funccfg_lock Value After Reset: 0x0
[11]	DSP0_CPU_LOCK	RW	dsp0_cpu_lock Value After Reset: 0x0
[10]	DSP1_CPU_LOCK	RW	dsp1_cpu_lock Value After Reset: 0x0
[9]	DSP0_DSP1_LOCK	RW	dsp0_dsp1_lock Value After Reset: 0x0
[8]	DSP1_DSP0_LOCK	RW	dsp1_dsp0_lock Value After Reset: 0x0

Bits	Field Name	Access	Description
[7]	CPU_DSP0_LOCK	RW	cpu_dsp0_lock Value After Reset: 0x0
[6]	CPU_DSP1_LOCK	RW	cpu_dsp1_lock Value After Reset: 0x0
[5:2]	RESERVED_1	-	
[1]	ISP_VENC_SHAKE_FUNC_LOCK	RW	isp_venc_shake_func_lock Value After Reset: 0x0
[0]	RESV_FUNCCFG_LOCK	RW	resv_funccfg_lock Value After Reset: 0x0

16.3.3.7 VO_SUBSYS Control Registers

16.3.3.7.1 VOSYS_GPU_SYSREG

- Description: GPU dxt bc enable register
- Offset: 0x6c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	GPU_DXT_BC_ENABLE	RW	Reserved Value After Reset: 0x0

16.3.3.7.2 VOSYS_GPU_SYSREG1

- Description: GPU idle indicate register
- Offset: 0x70
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	GPU_IDLE	RO	GPU idle status Value After Reset: 0x0

16.3.3.7.3 VOSYS_MIPIDSI0_SYSREG

- Description: DSI0 control register
- Offset: 0x74
- Default Value: 0x7050

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:10]	MIPI_DSI0_CFGCLKFREQRANGE	RW	MIPI_DSI0 cfg clock frequency range Value After Reset: 0x1C
[9:3]	MIPI_DSI0_HSFREQRANGE	RW	MIPI_DSI0 hs frequency configuration Value After Reset: 0xA
[2]	MIPI_DSI0_DPIUPDATECFG	RW	MIPI_DSI0 update configuration Value After Reset: 0x0
[1]	MIPI_DSI0_DPICOLORM	RW	MIPI_DSI0 color mode control Value After Reset: 0x0
[0]	MIPI_DSI0_DPISHUTDN	RW	MIPI_DSI0 shut down control Value After Reset: 0x0

16.3.3.7.4 VOSYS_MIPIDSI1_SYSREG

- Description: DSI1 control register
- Offset: 0x78
- Default Value: 0x7050

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:10]	MIPI_DSI1_CFGCLKFREQRANGE	RW	MIPI_DSI1 cfg clock frequency range Value After Reset: 0x1C
[9:3]	MIPI_DSI1_HSFREQRANGE	RW	MIPI_DSI1 hs frequency configuration Value After Reset: 0xA
[2]	MIPI_DSI1_DPIUPDATECFG	RW	MIPI_DSI1 update configuration Value After Reset: 0x0
[1]	MIPI_DSI1_DPICOLORM	RW	MIPI_DSI1 color mode control Value After Reset: 0x0
[0]	MIPI_DSI1_DPISHUTDN	RW	MIPI_DSI1 shut down control Value After Reset: 0x0

16.3.3.7.5 AXI4_VO_BUS_CFG

- Description: AXI4_VO bus priority register
- Offset: 0xa0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:7]	RESERVED_1	-	
[6]	AXI4_VO_PRIORITY_S1	RW	AXI_VO bus slave priority configuration Value After Reset: 0x0
[5:4]	AXI4_VO_PRIORITY_M3	RW	AXI_VO bus master3 priority configuration Value After Reset: 0x0
[3:2]	AXI4_VO_PRIORITY_M2	RW	AXI_VO bus master2 priority configuration Value After Reset: 0x0
[1:0]	AXI4_VO_PRIORITY_M1	RW	AXI_VO bus master1 priority configuration Value After Reset: 0x0

16.3.3.7.6 IOPMP_VOSYS_GPU_QOS

- Description: GPU IOPMP QoS register
- Offset: 0xa4
- Default Value: 0xff000

Bits	Field Name	Access	Description
[31:28]	RESERVED_1	-	
[27:24]	AR_OTHER_PRIOITY	RW	GPU_IOPMP ar other priority value Value After Reset: 0x0
[23:20]	AW_OTHER_PRIOITY	RW	GPU_IOPMP aw other priority value Value After Reset: 0x0
[19:16]	AR_MMU_PRIOITY	RW	GPU_IOPMP ar mmu priority value Value After Reset: 0xF
[15:12]	AW_MMU_PRIOITY	RW	GPU_IOPMP aw mmu priority value Value After Reset: 0xF
[11:6]	AR_MMU_TAG_ID	RW	GPU_IOPMP ar mmu tag id value Value After Reset: 0x0
[5:0]	AW_MMU_TAG_ID	RW	GPU_IOPMP aw mmu tag id value Value After Reset: 0x0

16.3.3.7.7 DPU1_SELECT

- Description: DPU1 pixel clock mux register
- Offset: 0xa8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	MIPI_DSI0_VIDEOIN_MUX_SEL	RW	MIPI DSI0 video data input mux, default 0. 0: Select DPU0 video output. 1: Select DPU1 video output. Value After Reset: 0x0
[0]	VOSYS_DPU0_PIXELCLK_SWITCH_SEL	RW	DPU1 pixel clock mux, default 1. 0: Select dpu0_pll_foutpostdiv. 1: Select dpu1_pll_foutpostdiv. Value After Reset: 0x0

16.3.3.7.8 DSI0_VSYNC_CFG

- Description: DSI0 polarity register for FPGA
- Offset: 0xac
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_2	-	
[8]	MIPI_DSI0_SHADOW_CLEAR	RW	DSI PLL register clear, just for FPGA version 0: Inactive 1: Active Value After Reset: 0x0
[7:1]	RESERVED_1	-	
[0]	MIPI_DSI0_VSYNC_POL	RW	Indicate DPU Vsync polarity, just for FPGA version. 0: Active high 1: Active low Value After Reset: 0x0

16.3.3.7.9 DSI0_HALT_MASK

- Description: DSI0 halt error mask register for FPGA
- Offset: 0xb4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI0_HALT_ERR_MASK	RW	DSI halt error mask, just for FPGA version

Bits	Field Name	Access	Description
			0: Not mask 1: Mask Value After Reset: 0x0

16.3.3.7.10 DSI1_VSYNC_CFG

- Description: DSI1 polarity register for FPGA
- Offset: 0xb8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_2	-	
[8]	MIPI_DSI1_SHADOW_CLEAR	RW	DSI PLL register clear, just for FPGA version 0: Inactive 1: Active Value After Reset: 0x0
[7:1]	RESERVED_1	-	
[0]	MIPI_DSI1_VSYNC_POL	RW	Indicate DPU Vsync polarity, just for FPGA version 0: Active high 1: Active low Value After Reset: 0x0

16.3.3.7.11 DSI1_HALT_ERR

- Description: DSI1 halt error register
- Offset: 0xbc
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI1_HALT_ERR	RO	Record DSI halt error. Value After Reset: 0x0

16.3.3.7.12 DSI1_HALT_MASK

- Description: DSI1 halt error mask register for FPGA
- Offset: 0xc0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI1_HALT_ERR_MASK	RW	DSI halt error mask 0: Not mask 1: Mask Value After Reset: 0x0

16.3.3.7.13 TEST_CLK_FREQ_STAT

- Description: Clock frequency register
- Offset: 0xc4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	TEST_CLK_FREQ_STAT	RO	clk_calc output freq_stat Value After Reset: 0x0

16.3.3.7.14 TEST_CLK_CFG

- Description: Clock sample control register
- Offset: 0xc8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_2	-	
[7:4]	TEST_CLK_SEL	RW	4: DPU cclk 5: APB pclk Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	TEST_CLK_SAMPLE_EN	RW	clk_calc sample enable Value After Reset: 0x0

16.3.3.7.15 GPU_GPIO

- Description: GPU GPIO register
- Offset: 0xcc
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:29]	RESERVED_4	-	

Bits	Field Name	Access	Description
[28]	GPIO_OUTPUT_REQ	RO	GPU GPIO output request Value After Reset: 0x0
[27:25]	RESERVED_3	-	
[24]	GPIO_OUTPUT_ACK	RW	GPU GPIO output ack Value After Reset: 0x0
[23:16]	GPIO_OUTPUT_DATA	RO	GPU GPIO output data Value After Reset: 0x0
[15:13]	RESERVED_2	-	
[12]	GPIO_INPUT_REQ	RW	GPU GPIO input request Value After Reset: 0x0
[11:9]	RESERVED_1	-	
[8]	GPIO_INPUT_ACK	RO	GPU GPIO input ack Value After Reset: 0x0
[7:0]	GPIO_INPUT_DATA	RW	GPU GPIO input data Value After Reset: 0x0

16.3.3.7.16 HDMI_COLOR_BAR_CFG

- Description: HDMI color bar control register
- Offset: 0xd0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:7]	RESERVED_2	-	
[6:4]	HDMI_COLOR_BAR_TEST_MODE	RW	HDMI color bar configuration test enable 3'b000: 640_480_60HZ 3'b001: 720_480_60HZ 3'b010: 1280_720_24HZ 3'b011: 1280_720_60HZ 3'b100: 1920_1080_30HZ 3'b101: 3840_2160_30HZ 3'b110: 4096_2160_30HZ Value After Reset: 0x0
[3:1]	RESERVED_1	-	

Bits	Field Name	Access	Description
[0]	HDMI_COLOR_BAR_TEST_EN	RW	HDMI color bar configuration test enable Value After Reset: 0x0

16.3.3.7.17 GPU_CNT_CLR

- Description: GPU timer counter clear register
- Offset: 0xd4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	GPU_CNT_CLR	RW	GPU counter clear, software set 1 to clear counter value. Value After Reset: 0x0

16.3.3.7.18 GPU_CNT_VALUE

- Description: GPU timer counter value register
- Offset: 0xd8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	GPU_TIMER_VALUE	RO	Get GPU counter value. Value After Reset: 0x0

16.3.3.7.19 DPU_ADDR_REMAP

- Description: DPU address remap register
- Offset: 0xe0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DPU_AXI1_REMAP_EN	RW	DPU AXI1 remap enable Value After Reset: 0x0
[2]	DPU_AXI1_RANK_SEL	RW	DPU AXI1 addr_remap module rank_sel Value After Reset: 0x0
[1]	DPU_AXI0_REMAP_EN	RW	DPU AXI0 remap enable Value After Reset: 0x0

Bits	Field Name	Access	Description
[0]	DPU_AXI0_RANK_SEL	RW	DPU AXI0 addr_remap module rank_sel Value After Reset: 0x0

16.3.3.7.20 MIPI_DSI0_ZCAL_RSTZ_SYSREG

- Description: mipi_dsi0_zcal_rstz register
- Offset: 0x100
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI0_ZCAL_RSTZ_SYSREG	RW	mipi_dsi0_zcal_rstz Value After Reset: 0x1

16.3.3.7.21 MIPI_DSI0_ZCAL_DONE_SYSREG

- Description: mipi_dsi0_zcal_done register for FPGA
- Offset: 0x104
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI0_ZCAL_DONE_SYSREG	RO	mipi_dsi0_zcal_done Value After Reset: 0x0

16.3.3.7.22 MIPI_DSI0_GLUEIFTESTER_SYSREG

- Description: mipi_dsi0_glueiftester register for FPGA
- Offset: 0x108
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	MIPI_DSI0_GLUEIFTESTER_SYSREG	RW	mipi_dsi0_glueiftester Value After Reset: 0x1

16.3.3.7.23 MIPI_DSI0_CLKEXT_SYSREG

- Description: mipi_dsi0_clkext register for FPGA
- Offset: 0x10c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI0_CLKEXT_SYSREG	RW	mipi_dsi0_clkext Value After Reset: 0x0

16.3.3.7.24 MIPI_DSI0_DIV_EN_IN_TX_SYSREG

- Description: mipi_dsi0_div_en_in_tx register for FPGA
- Offset: 0x110
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI0_DIV_EN_IN_TX_SYSREG	RW	mipi_dsi0_div_en_in_tx Value After Reset: 0x0

16.3.3.7.25 MIPI_DSI0_CLOCKUNGATING_IN_TX_SYSREG

- Description: mipi_dsi0_clockungating_in_tx register for FPGA
- Offset: 0x114
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI0_CLOCKUNGATING_IN_TX_SYSREG	RW	mipi_dsi0_clockungating_in_tx Value After Reset: 0x0

16.3.3.7.26 MIPI_DSI0_CLOCK8SENT_IN_TX_SYSREG

- Description: mipi_dsi0_clock8sent_in_tx register for FPGA
- Offset: 0x118
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI0_CLOCK8SENT_IN_TX_SYSREG	RW	mipi_dsi0_clock8sent_in_tx Value After Reset: 0x0

16.3.3.7.27 MIPI_DSI0_CLK_KILL_IN_TX_SYSREG

- Description: mipi_dsi0_clk_kill_in_tx register for FPGA

- Offset: 0x11c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI0_CLK_KILL_IN_TX_SYSREG	RW	mipi_dsi0_clk_kill_in_tx Value After Reset: 0x0

16.3.3.7.28 MIPI_DSI0_CLK_EN_IN_TX_SYSREG

- Description: mipi_dsi0_clk_en_in_tx register for FPGA
- Offset: 0x120
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI0_CLK_EN_IN_TX_SYSREG	RW	mipi_dsi0_clk_en_in_tx Value After Reset: 0x0

16.3.3.7.29 MIPI_DSI0_HSTRAILDONE_IN_TX_SYSREG

- Description: mipi_dsi0_hstraildone_in_tx register for FPGA
- Offset: 0x124
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI0_HSTRAILDONE_IN_TX_SYSREG	RW	mipi_dsi0_hstraildone_in_tx Value After Reset: 0x0

16.3.3.7.30 MIPI_DSI1_ZCAL_RSTZ_SYSREG

- Description: mipi_dsi1_zcal_rstz register for FPGA
- Offset: 0x130
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI1_ZCAL_RSTZ_SYSREG	RW	mipi_dsi1_zcal_rstz Value After Reset: 0x1

16.3.3.7.31 MIPI_DSI1_ZCAL_DONE_SYSREG

- Description: mipi_dsi1_zcal_done register for FPGA
- Offset: 0x134
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI1_ZCAL_DONE_SYSREG	RO	mipi_dsi1_zcal_done Value After Reset: 0x0

16.3.3.7.32 MIPI_DSI1_GLUEIFTESTER_SYSREG

- Description: mipi_dsi1_glueiftester register for FPGA
- Offset: 0x138
- Default Value: 0x1

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	MIPI_DSI1_GLUEIFTESTER_SYSREG	RW	mipi_dsi1_glueiftester Value After Reset: 0x1

16.3.3.7.33 MIPI_DSI1_CLKEXT_SYSREG

- Description: mipi_dsi1_clkext register for FPGA
- Offset: 0x13c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI1_CLKEXT_SYSREG	RW	mipi_dsi1_clkext Value After Reset: 0x0

16.3.3.7.34 MIPI_DSI1_DIV_EN_IN_TX_SYSREG

- Description: mipi_dsi1_div_en_in_tx register for FPGA
- Offset: 0x140
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI1_DIV_EN_IN_TX_SYSRE	RW	mipi_dsi1_div_en_in_tx

Bits	Field Name	Access	Description
	G		Value After Reset: 0x0

16.3.3.7.35 MIPI_DSI1_CLOCKUNGATING_IN_TX_SYSREG

- Description: mipi_dsi1_clockungating_in_tx register for FPGA
- Offset: 0x144
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI1_CLOCKUNGATING_IN_TX_SYSREG	RW	mipi_dsi1_clockungating_in_tx Value After Reset: 0x0

16.3.3.7.36 MIPI_DSI1_CLOCK8SENT_IN_TX_SYSREG

- Description: mipi_dsi1_clock8sent_in_tx register for FPGA
- Offset: 0x148
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI1_CLOCK8SENT_IN_TX_SYSREG	RW	mipi_dsi1_clock8sent_in_tx Value After Reset: 0x0

16.3.3.7.37 MIPI_DSI1_CLK_KILL_IN_TX_SYSREG

- Description: mipi_dsi1_clk_kill_in_tx register for FPGA
- Offset: 0x14c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI1_CLK_KILL_IN_TX_SYSREG	RW	mipi_dsi1_clk_kill_in_tx Value After Reset: 0x0

16.3.3.7.38 MIPI_DSI1_CLK_EN_IN_TX_SYSREG

- Description: mipi_dsi1_clk_en_in_tx register for FPGA
- Offset: 0x150
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI1_CLK_EN_IN_TX_SYSREG	RW	mipi_dsi1_clk_en_in_tx Value After Reset: 0x0

16.3.3.7.39 MIPI_DSI1_HSTRAILDONE_IN_TX_SYSREG

- Description: mipi_dsi1_hstraildone_in_tx register for FPGA
- Offset: 0x154
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI1_HSTRAILDONE_IN_TX_SYSREG	RW	mipi_dsi1_hstraildone_in_tx Value After Reset: 0x0

16.3.3.7.40 HDMI_ZCAL_RSTZ_SYSREG

- Description: hdmi_zcal_rstz register for FPGA
- Offset: 0x160
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	HDMI_ZCAL_RSTZ_SYSREG	RW	hdmi_zcal rstz Value After Reset: 0x0

16.3.3.7.41 HDMI_ZCAL_DONE_SYSREG

- Description: hdmi_zcal_done register for FPGA
- Offset: 0x164
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	HDMI_ZCAL_DONE_SYSREG	RO	hdmi_zcal done Value After Reset: 0x0

16.3.3.7.42 HDMI_CONTINUITY_SYSREG

- Description: hdmi_cont_en register for FPGA

- Offset: 0x168
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:1]	HDMI_CONT_DATA	RO	hdmi_cont data Value After Reset: 0x0
[0]	HDMI_CONT_EN	RW	hdmi_cont enable Value After Reset: 0x0

16.3.3.7.43 HDMI_BIST_SYSREG

- Description: hdmi_bisten register for FPGA
- Offset: 0x16c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	HDMI_BISTOK	RO	hdmi_bist ok Value After Reset: 0x0
[1]	HDMI_BISTDONE	RO	hdmi_bist done Value After Reset: 0x0
[0]	HDMI_BISTEN	RW	hdmi bist enable Value After Reset: 0x0

16.3.3.7.44 RESERVED_REG_0

- Description: Reserved register
- Offset: 0x200
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_0	RW	Reserved Value After Reset: 0x0

16.3.3.7.45 RESERVED_REG_1

- Description: Reserved register
- Offset: 0x204
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_1	RW	Reserved Value After Reset: 0x0

16.3.3.7.46 RESERVED_REG_2

- Description: Reserved register
- Offset: 0x208
- Default Value: 0xffffffff

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_2	RW	Reserved Value After Reset: 0xFFFFFFFF

16.3.3.7.47 RESERVED_REG_3

- Description: Reserved register
- Offset: 0x20c
- Default Value: 0xffffffff

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_3	RW	Reserved Value After Reset: 0xFFFFFFFF

16.3.3.7.48 VOSYS_GPU_SYSREG_TEE

- Description: GPU dxt_bc TEE register
- Offset: 0x106c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	GPU_DXT_BC_ENABLE	RW	gpu_dxt_bc signal enable Value After Reset: 0x0

16.3.3.7.49 VOSYS_GPU_SYSREG1_TEE

- Description: GPU idle TEE register
- Offset: 0x1070
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	GPU_IDLE	RO	GPU idle status Value After Reset: 0x0

16.3.3.7.50 VOSYS_MIPIDSI0_SYSREG_TEE

- Description: DSI0 control TEE register
- Offset: 0x1074
- Default Value: 0x7050

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:10]	MIPI_DSI0_CFGCLKFREQRANGE	RW	MIPI_DSI0 cfg clock frequency range Value After Reset: 0x1C
[9:3]	MIPI_DSI0_HSFREQRANGE	RW	MIPI_DSI0 hs frequency configuration Value After Reset: 0xA
[2]	MIPI_DSI0_DPIUPDATECFG	RW	MIPI_DSI0 update configuration Value After Reset: 0x0
[1]	MIPI_DSI0_DPICOLORM	RW	MIPI_DSI0 color mode control Value After Reset: 0x0
[0]	MIPI_DSI0_DPISHUTDN	RW	MIPI_DSI0 shut down control Value After Reset: 0x0

16.3.3.7.51 VOSYS_MIPIDSI1_SYSREG_TEE

- Description: DSI1 control TEE register
- Offset: 0x1078
- Default Value: 0x7050

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:10]	MIPI_DSI1_CFGCLKFREQRANGE	RW	MIPI_DSI1 cfg clock frequency range Value After Reset: 0x1C
[9:3]	MIPI_DSI1_HSFREQRANGE	RW	MIPI_DSI1 hs frequency configuration Value After Reset: 0xA
[2]	MIPI_DSI1_DPIUPDATECFG	RW	MIPI_DSI1 update configuration

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[1]	MIPI_DSI1_DPICOLORM	RW	MIPI_DSI1 color mode control Value After Reset: 0x0
[0]	MIPI_DSI1_DPISHUTDN	RW	MIPI_DSI1 shut down control Value After Reset: 0x0

16.3.3.7.52 AXI4_VO_BUS_CFG_TEE

- Description: AXI4_VO bus priority TEE register
- Offset: 0x10a0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:7]	RESERVED_1	-	
[6]	AXI4_VO_PRIORITY_S1	RW	AXI_VO bus slave priority configuration Value After Reset: 0x0
[5:4]	AXI4_VO_PRIORITY_M3	RW	AXI_VO bus master3 priority configuration Value After Reset: 0x0
[3:2]	AXI4_VO_PRIORITY_M2	RW	AXI_VO bus master2 priority configuration Value After Reset: 0x0
[1:0]	AXI4_VO_PRIORITY_M1	RW	AXI_VO bus master1 priority configuration Value After Reset: 0x0

16.3.3.7.53 IOPMP_VOSYS_GPU_QOS_TEE

- Description: GPU IOPMP QoS TEE register
- Offset: 0x10a4
- Default Value: 0xff000

Bits	Field Name	Access	Description
[31:28]	RESERVED_1	-	
[27:24]	AR_OTHER_PRIOITY	RW	GPU_IOPMP ar other priority value Value After Reset: 0x0
[23:20]	AW_OTHER_PRIOITY	RW	GPU_IOPMP aw other priority value Value After Reset: 0x0
[19:16]	AR_MMU_PRIOITY	RW	GPU_IOPMP ar mmu priority value

Bits	Field Name	Access	Description
			Value After Reset: 0xF
[15:12]	AW_MMU_PRIOITY	RW	GPU_IOPMP aw mmu priority value Value After Reset: 0xF
[11:6]	AR_MMU_TAG_ID	RW	GPU_IOPMP ar mmu tag id value Value After Reset: 0x0
[5:0]	AW_MMU_TAG_ID	RW	GPU_IOPMP aw mmu tag id value Value After Reset: 0x0

16.3.3.7.54 DPU1_SELECT_TEE

- Description: DPU1 pixel clock mux TEE register
- Offset: 0x10a8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:2]	RESERVED_1	-	
[1]	MIPI_DSI0_VIDEOIN_MUX_SEL	RW	MIPI DSI0 video data input mux, default 0. 0: Select DPU0 video output. 1: Select DPU1 video output. Value After Reset: 0x0
[0]	VOSYS_DPU0_PIXELCLK_SWITCH_SEL	RW	DPU1 pixel clock mux, default 1. 0: Select dpu0_pll_foutpostdiv. 1: Select dpu1_pll_foutpostdiv. Value After Reset: 0x0

16.3.3.7.55 DSI0_VSYNC_CFG_TEE

- Description: DSI0 polarity TEE register for FPGA
- Offset: 0x10ac
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_2	-	
[8]	MIPI_DSI0_SHADOW_CLEAR	RW	DSI PLL register clear 0: Inactive 1: Active Value After Reset: 0x0

Bits	Field Name	Access	Description
[7:1]	RESERVED_1	-	
[0]	MIPI_DSI0_VSYNC_POL	RW	Indicate DPU Vsync polarity. 0: Active high 1: Active low Value After Reset: 0x0

16.3.3.7.56 DSI0_HALT_ERR_TEE

- Description: DSI0 halt error mask TEE register
- Offset: 0x10b0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI0_HALT_ERR	RO	Record DSI halt error. Value After Reset: 0x0

16.3.3.7.57 DSI0_HALT_MASK_TEE

- Description: DSI0 halt mask TEE register
- Offset: 0x10b4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI0_HALT_ERR_MASK	RW	DSI halt error mask 0: Not mask 1: Mask Value After Reset: 0x0

16.3.3.7.58 DSI1_VSYNC_CFG_TEE

- Description: DSI1 polarity TEE register for FPGA
- Offset: 0x10b8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_2	-	
[8]	MIPI_DSI1_SHADOW_CLEAR	RW	DSI PLL register clear

Bits	Field Name	Access	Description
			0: Inactive 1: Active Value After Reset: 0x0
[7:1]	RESERVED_1	-	
[0]	MIPI_DSI1_VSYNC_POL	RW	Indicate DPU Vsync polarity. 0: Active high 1: Active low Value After Reset: 0x0

16.3.3.7.59 DSI1_HALT_ERR_TEE

- Description: DSI1 halt error TEE register
- Offset: 0x10bc
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI1_HALT_ERR	RO	Record DSI halt error. Value After Reset: 0x0

16.3.3.7.60 DSI1_HALT_MASK_TEE

- Description: DSI1 halt mask TEE register
- Offset: 0x10c0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	MIPI_DSI1_HALT_ERR_MASK	RW	DSI halt error mask 0: Not mask 1: Mask Value After Reset: 0x0

16.3.3.7.61 TEST_CLK_FREQ_STAT_TEE

- Description: Test clock frequency TEE register
- Offset: 0x10c4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	TEST_CLK_FREQ_STAT	RO	clk_calc output freq_stat Value After Reset: 0x0

16.3.3.7.62 TEST_CLK_CFG_TEE

- Description: Test clock configuration TEE register
- Offset: 0x10c8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_2	-	
[7:4]	TEST_CLK_SEL	RW	clk_calc clock select Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	TEST_CLK_SAMPLE_EN	RW	clk_calc sample enable Value After Reset: 0x0

16.3.3.7.63 GPU_GPIO_TEE

- Description: GPU GPIO TEE register
- Offset: 0x10cc
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:29]	RESERVED_4	-	
[28]	GPIO_OUTPUT_REQ	RO	GPU GPIO output request Value After Reset: 0x0
[27:25]	RESERVED_3	-	
[24]	GPIO_OUTPUT_ACK	RW	GPU GPIO output ack Value After Reset: 0x0
[23:16]	GPIO_OUTPUT_DATA	RO	GPU GPIO output data Value After Reset: 0x0
[15:13]	RESERVED_2	-	
[12]	GPIO_INPUT_REQ	RW	GPU GPIO input request Value After Reset: 0x0
[11:9]	RESERVED_1	-	

Bits	Field Name	Access	Description
[8]	GPIO_INPUT_ACK	RO	GPU GPIO input ack Value After Reset: 0x0
[7:0]	GPIO_INPUT_DATA	RW	GPU GPIO input data Value After Reset: 0x0

16.3.3.7.64 HDMI_COLOR_BAR_CFG_TEE

- Description: HDMI color bar configuration TEE register
- Offset: 0x10d0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:7]	RESERVED_2	-	
[6:4]	HDMI_COLOR_BAR_TEST_MODE	RW	HDMI color bar configuration test enable 3'b000: 640_480_60Hz 3'b001: 720_480_60Hz 3'b010: 1280_720_24Hz 3'b011: 1280_720_60Hz 3'b100: 1920_1080_30Hz 3'b101: 3840_2160_30Hz 3'b110: 4096_2160_30Hz Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	HDMI_COLOR_BAR_TEST_EN	RW	HDMI color bar configuration test enable Value After Reset: 0x0

16.3.3.7.65 GPU_CNT_CLR_TEE

- Description: GPU timer counter clear TEE register
- Offset: 0x10d4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	GPU_CNT_CLR	RW	GPU counter clear, software set 1 to clear counter value. Value After Reset: 0x0

16.3.3.7.66 GPU_CNT_VALUE_TEE

- Description: GPU timer counter value TEE register
- Offset: 0x10d8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	GPU_TIMER_VALUE	RO	Get GPU counter value. Value After Reset: 0x0

16.3.3.7.67 DPU_ADDR_REMAP_TEE

- Description: DPU address remap TEE register
- Offset: 0x10e0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3]	DPU_AXI1_REMAP_EN	RW	DPU AXI1 remap enable Value After Reset: 0x0
[2]	DPU_AXI1_RANK_SEL	RW	DPU AXI1 addr_remap module rank_sel Value After Reset: 0x0
[1]	DPU_AXI0_REMAP_EN	RW	DPU AXI0 remap enable Value After Reset: 0x0
[0]	DPU_AXI0_RANK_SEL	RW	DPU AXI0 addr_remap module rank_sel Value After Reset: 0x0

16.3.3.7.68 HDMI_CONTINUITY_SYSREG_TEE

- Description: HDMI continuity TEE register
- Offset: 0x1168
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:11]	RESERVED_1	-	
[10:1]	HDMI_CONT_DATA	RO	hdmi_cont data Value After Reset: 0x0
[0]	HDMI_CONT_EN	RW	hdmi_cont enable Value After Reset: 0x0

16.3.3.7.69 HDMI_BIST_SYSREG_TEE

- Description: HDMI bist TEE register
- Offset: 0x116c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	HDMI_BISTOK	RO	hdmi_bist ok Value After Reset: 0x0
[1]	HDMI_BISTDONE	RO	hdmi_bist done Value After Reset: 0x0
[0]	HDMI_BISTEN	RW	hdmi bist enable Value After Reset: 0x0

16.3.3.7.70 RESERVED_REG_0_TEE

- Description: Reserved TEE register
- Offset: 0x1200
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_0	RW	Reserved Value After Reset: 0x0

16.3.3.7.71 RESERVED_REG_1_TEE

- Description: Reserved TEE register
- Offset: 0x1204
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_1	RW	Reserved Value After Reset: 0x0

16.3.3.7.72 RESERVED_REG_2_TEE

- Description: Reserved TEE register
- Offset: 0x1208
- Default Value: 0xffffffff

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_2	RW	Reserved Value After Reset: 0xFFFFFFFF

16.3.3.7.73 RESERVED_REG_3_TEE

- Description: Reserved TEE register
- Offset: 0x120c
- Default Value: 0xffffffff

Bits	Field Name	Access	Description
[31:0]	RESERVED_REG_3	RW	Reserved Value After Reset: 0xFFFFFFFF

16.3.3.7.74 CFG_LOCK_TEE

- Description: Configuration lock TEE register
- Offset: 0x1a00
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7]	DPU_ADDR_REMAP_LOCK	RW	DPU address remap lock Value After Reset: 0x0
[6]	VO_SUBSYS_CFG_LOCK	RW	VO SUBSYS bus configuration lock Value After Reset: 0x0
[5]	TEST_CLK_CFG_LOCK	RW	test_clk configuration lock for clk_calc module Value After Reset: 0x0
[4]	MIPI_DSI1_CFG_LOCK	RW	MIPI_DSI1 module configuration lock Value After Reset: 0x0
[3]	MIPI_DSI0_CFG_LOCK	RW	MIPI_DSI0 module configuration lock Value After Reset: 0x0
[2]	HDMI_CFG_LOCK	RW	HDMI module configuration lock Value After Reset: 0x0
[1]	GPU_CFG_LOCK	RW	GPU module configuration lock Value After Reset: 0x0
[0]	DPU_CFG_LOCK	RW	DPU module configuration lock Value After Reset: 0x0

16.3.3.8 VP_SUBSYS Control Registers

16.3.3.8.1 VPSYS_DBG_STS

- Description: VPSYS_DBG_STS
- Offset: 0x40
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	G2D_DBG	RO	Value After Reset: 0x0

16.3.3.8.2 VPSYS_VDEC_FUSE_CFG

- Description: VPSYS_VDEC_FUSE_CFG
- Offset: 0x44
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	VDEC_FUSE	RW	0: Enable 1: Disable Value After Reset: 0x0

16.3.3.8.3 VPSYS_VENC_FUSE_CFG

- Description: VPSYS_VENC_FUSE_CFG
- Offset: 0x48
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:20]	RESERVED_1	-	
[19:0]	VENC_FUSE	RW	0: Enable, 1: Disable [0] fuse_enc_vp9 [1] fuse_enc_jpeg Others: Reserved Value After Reset: 0x0

16.3.3.8.4 VPSYS_ADDR_SEL

- Description: VPSYS_ADDR_SEL
- Offset: 0x60

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_3	-	
[9]	G2D_RANK_SEL	RW	1: G2D access rank1: 4~(8GB-6MB) 0: G2D access rank0: 0~(4GB-6MB) Value After Reset: 0x0
[8]	G2D_REMAP_EN	RW	1: G2D address remap enable 0: G2D address remap disable Value After Reset: 0x0
[7:6]	RESERVED_2	-	
[5]	VDEC_RANK_SEL	RW	1: VDEC access rank1: 4~(8GB-6MB) 0: VDEC access rank0: 0~(4GB-6MB) Value After Reset: 0x0
[4]	VDEC_REMAP_EN	RW	1: VDEC address remap enable 0: VDEC address remap disable Value After Reset: 0x0
[3:2]	RESERVED_1	-	
[1]	VENC_RANK_SEL	RW	1: VENC access rank1: 4~(8GB-6MB) 0: VENC access rank0: 0~(4GB-6MB) Value After Reset: 0x0
[0]	VENC_REMAP_EN	RW	1: VENC address remap enable 0: VENC address remap disable Value After Reset: 0x0

16.3.3.8.5 VPSYS_DBG_TEESTS

- Description: VPSYS_DBG_TEESTS
- Offset: 0x1040
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	G2D_DBG	RO	Value After Reset: 0x0

16.3.3.8.6 VPSYS_VDEC_FUSE_TEECFG

- Description: VPSYS_VDEC_FUSE_TEECFG

- Offset: 0x1044
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	VDEC_FUSE	RW	0: Enable 1: Disable Value After Reset: 0x0

16.3.3.8.7 VPSYS_VENC_FUSE_TEECFG

- Description: VPSYS_VENC_FUSE_TEECFG
- Offset: 0x1048
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:20]	RESERVED_1	-	
[19:0]	VENC_FUSE	RW	0: Enable, 1: Disable [0] fuse_enc_vp9 [1] fuse_enc_jpeg Others: Reserved Value After Reset: 0x0

16.3.3.8.8 LOCK_CFG

- Description: LOCK_CFG
- Offset: 0x1800
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:5]	RESERVED_1	-	
[4]	VP_CFG_LOCK	RW	Lock Value After Reset: 0x0
[3]	FCE_CFG_LOCK	RW	Lock Value After Reset: 0x0
[2]	G2D_CFG_LOCK	RW	Lock Value After Reset: 0x0
[1]	VENC_CFG_LOCK	RW	Lock Value After Reset: 0x0
[0]	VDEC_CFG_LOCK	RW	Lock

Bits	Field Name	Access	Description
			Value After Reset: 0x0

16.3.3.8.9 VPSYS_ADDR_TEESEL

- Description: VPSYS_ADDR_TEESEL
- Offset: 0x1060
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_3	-	
[9]	G2D_RANK_SEL	RW	1: G2D access rank1: 4~(8GB-6MB) 0: G2D access rank0: 0~(4GB-6MB) Value After Reset: 0x0
[8]	G2D_REMAP_EN	RW	1: G2D address remap enable 0: G2D address remap disable Value After Reset: 0x0
[7:6]	RESERVED_2	-	
[5]	VDEC_RANK_SEL	RW	1: VDEC access rank1: 4~(8GB-6MB) 0: VDEC access rank0: 0~(4GB-6MB) Value After Reset: 0x0
[4]	VDEC_REMAP_EN	RW	1: VDEC address remap enable 0: VDEC address remap disable Value After Reset: 0x0
[3:2]	RESERVED_1	-	
[1]	VENC_RANK_SEL	RW	1: VENC access rank1: 4~(8GB-6MB) 0: VENC access rank0: 0~(4GB-6MB) Value After Reset: 0x0
[0]	VENC_REMAP_EN	RW	1: VENC address remap enable 0: VENC address remap disable Value After Reset: 0x0

17 BMU

17.1 Overview

The Bus Monitor Unit (BMU) block is integrated in the same layer with the monitor module. It can monitor bandwidth, access cycle and burst length of AXI port. Supports single monitor and period monitor. Supports ID/address range/transaction size filtering for transactions. The diagram of top-layer module instantiation is as follows:

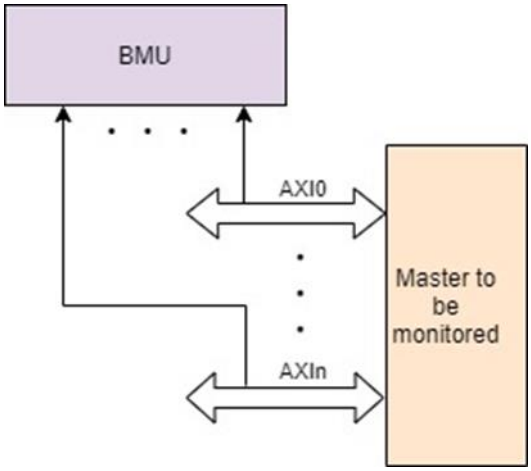


Figure & Table 17-1 BMU system integration

17.2 Main Features

Each BMU supports monitor of 10 events. The monitor of the 10 events supports ID filtering. Event8 and Event9 are used to filter address range/address alignment/burst length.

Figure & Table 17-2 AXI port event monitor

No.	Event	Description
0	Total read transaction number	Total read transaction number
1	Total read byte number	Total read byte number
2	Total read duration number	Total read duration number
3	Total read command delay number	The number of read commands that duration over the threshold
4	Total write transaction number	Total write transaction number
5	Total write byte number	Total write byte number
6	Total write duration number	Total write duration number
7	Total write command delay number	The number of write commands that duration over the

No.	Event	Description
		threshold
8	Variable read command counter	Address alignment/address range/length/size filter
9	Variable write command counter	Address alignment/address range /length/size filter

NOTE

Event8/ Event9, each with two groups of counters, supports outputting two sets of states at the same time.

The 10 events can take different combinations to provide information required by the user. For example, if the user wants to monitor the average burst length of read transmission, it can be calculated by counter1/counter0, and the average period of read transmission is calculated by counter2/counter0. Counter8, the variable read command counter, provides a filter of address range, which is convenient for the user to learn the hit ratio of the target address range and assists the user in debugging bandwidth problems.

17.3 Function Description

17.3.1 Overview

BMU consists of two modules: APB control module and AXI monitor module. The counters work in their respective AXI clock domains. When BMU is not enabled, the entire function can be clock gated to reduce power consumption.

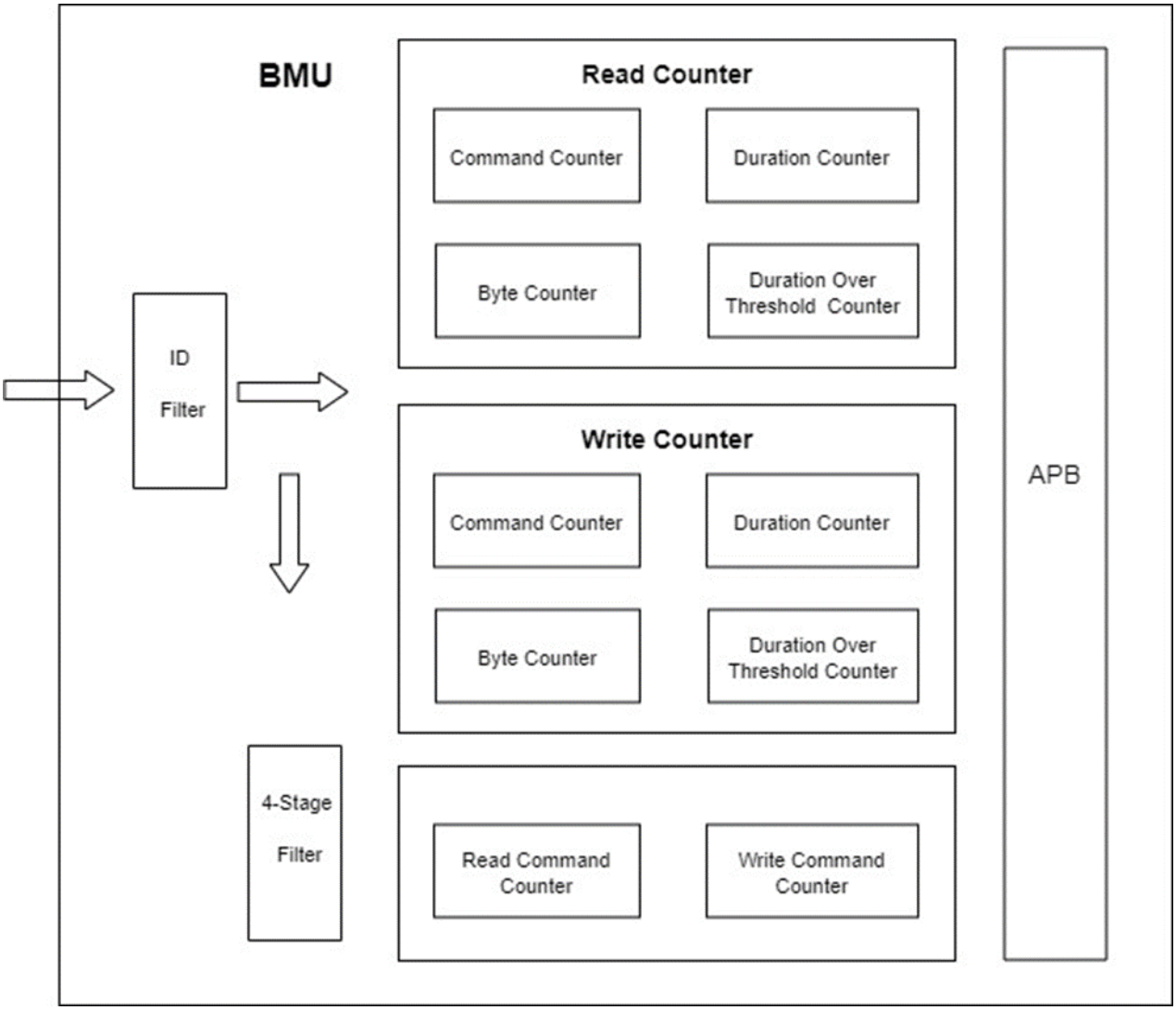


Figure & Table 17-3 BMU block diagram

17.3.2 Bandwidth Monitor Mode

17.3.2.1 Filter

The ID filter allows the user to select the target master for monitoring. ID Mask is used to configure the ID bit that needs to be compared, and Target ID is used to set the ID of the target master. Events 0-7 in Figure & Table 17-2 support ID filter. ID filter will only filter read and write command channels, read data and write response channels.

Events 8 and 9 additionally support variables filters, specifically 4-stage filter for address range, address alignment, burst length and size. This 4-stage filter is designed in series for users to choose freely. The specific registers are BMU_CFG6, BMU_CFG10, BMU_CFG0[31:16], BMU_CFG5, and BMU_CFG4.

17.3.2.2 Data Monitor

Events 0, 1, 4 and 5 in Figure & Table 17-2 can be used for users to count the number of transmission commands and the amount of data to be transmitted, which, in combination with the monitor period, can be directly converted into bandwidth information.
The register BMU_OSTD_STS also provides an average outstanding array for users to analyze.

17.3.2.3 Delay Monitor

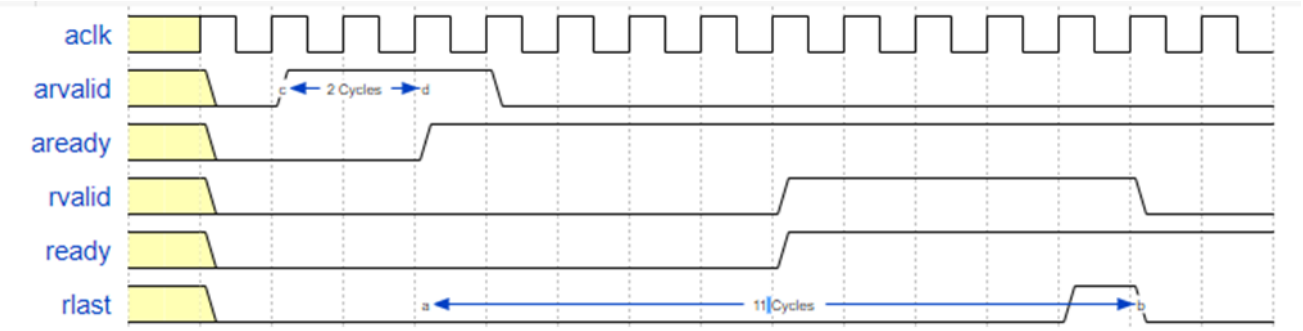


Figure & Table 17-4 Command delay and data delay

BMU supports statistics on the overall command delay and data delay information in the monitor period. As shown in Figure & Table 17-4, the command delay is 2 and the data delay is 11. The overall command delay information of read and write is recorded in the registers BMU_RD_STS4 and BMU_WR_STS4 respectively. The overall data delay information of read and write is recorded in the registers BMU_RD_STS0 and BMU_WR_STS0 respectively. The overall delay data that the user can read is divided by the number of commands to obtain the corresponding average delay. The total number of read commands is recorded in the register BMU_RD_STS1, and the total number of write commands is recorded in the register BMU_WR_STS1.
In order to facilitate users to evaluate the distribution of delay, it also supports to count the number of commands whose delay exceeds a specific threshold. For example, it is known that the average delay of read data is 1000 clock cycles. If the user needs to know the number of commands with a delay of more than 2000 clock cycles, he can set the threshold in BMU_CFG1 to enable BMU to monitor the number of commands whose read data delay exceeds 2000 clock cycles, and the final data is reflected in the register BMU_RD_STS3. In addition, it should be noted that the current hardware design only supports 16 sets of threshold counters. Therefore, when the transmission outstanding exceeds 16, the threshold count overflow will be generated. The overflow flags are in bit4 and bit7 of BMU_IR_STS0.rg_sta_apb_src. If the user observes that an overflow occurs, the corresponding count data BMU_RD_STS3 needs to be multiplied by the coefficient of the corresponding command filter BMU_FLT.

17.3.2.4 Data Upload

In the period monitor mode, the updated count data of the BMU cycle is stored in the register BMU_*_STS*. The data counted in the next monitor cycle will overwrite that counted in the previous cycle and BMU will also issue an interrupt to inform the system that the data has been updated.

In the single monitor mode, BMU will only count the data in a single monitor.

17.3.3 Debug Mode

BMU detects whether there is a target address access behavior and triggers an interrupt to inform the user. For setting the address range, refer to the registers BMU_CFG6 and BMU_CFG10. The corresponding interrupt sources are bit16 and bit17 of BMU_IR_STS2.

17.4 Usage

17.4.1 Single Monitor

1. Configure the monitor period window through BMU_CFG3, the unit is the cycle of the configuration register.
2. Configure BMU_CFG0.RG_CTL_TRIGGER_MODE = 1.
3. Release reset, BMU_CFG0.RG_CTL_SW_RSTN = 1.
4. Configure the threshold for access duration through BMU_CFG1, which is convenient for counting the number of commands that exceed the specific threshold.
5. Configure ID of the master to be monitored through BMU_CFG2.
6. Configure BMU_CFG4~6, BMU_CFG10, and BMU_CFG14 as required.
7. Trigger enable bit, write 1 and then 0 to BMU_CFG0.RG_CTL_MON_EN.

17.4.2 Period Monitor

1. Configure the monitor period window through BMU_CFG3, the unit is the cycle of the configuration register.
2. Configure BMU_CFG0.RG_CTL_TRIGGER_MODE = 0.
3. Release reset, BMU_CFG0.RG_CTL_SW_RSTN = 1.
4. Configure ID to the master to be monitored.
5. Configure BMU_CFG4~6, BMU_CFG10, and BMU_CFG14 as required.
6. Enable monitor, BMU_CFG0.RG_CTL_MON_EN=1.

17.5 Register Description

17.5.1 Register Memory Map

Register	Offset	Description	Section/Page
BMU_CFG0	0x0	MISC control of BMU	17.5.2.1/1217
BMU_CFG1	0x4	Threshold of duration configuration	17.5.2.2/1218
BMU_CFG2	0x8	ID configuration of BMU	17.5.2.3/1218
BMU_CFG3	0xc	Monitor window	17.5.2.4/1219

Register	Offset	Description	Section/Page
BMU_CFG4	0x10	Filter enable	17.5.2.5/1219
BMU_CFG5	0x14	Length filter enable	17.5.2.6/1220
BMU_CFG6	0x18	Upper0 address configuration	17.5.2.7/1220
BMU_CFG7	0x1c	Upper1 address configuration	17.5.2.8/1220
BMU_CFG8	0x20	Upper2 address configuration	17.5.2.9/1221
BMU_CFG9	0x24	Upper3 address configuration	17.5.2.10/1221
BMU_FILT	0x28	Duration filter configuration	17.5.2.11/1221
BMU_CFG10	0x2c	Lower0 address configuration	17.5.2.12/1222
BMU_CFG11	0x30	Lower1 address configuration	17.5.2.13/1222
BMU_CFG12	0x34	Lower2 address configuration	17.5.2.14/1223
BMU_CFG13	0x38	Lower3 address configuration	17.5.2.15/1223
BMU_CFG14	0x3c	Target data configuration	17.5.2.16/1223
BMU_RD_STS0	0x40	EVENT2 status	17.5.2.17/1223
BMU_RD_STS1	0x44	EVENT0 status	17.5.2.18/1224
BMU_RD_STS2	0x48	EVENT1 status	17.5.2.19/1224
BMU_RD_STS3	0x4c	EVENT3 status	17.5.2.20/1224
BMU_WR_STS0	0x50	EVENT6 status	17.5.2.21/1224
BMU_WR_STS1	0x54	EVENT4 status	17.5.2.22/1225
BMU_WR_STS2	0x58	EVENT5 status	17.5.2.23/1225
BMU_WR_STS3	0x5c	EVENT7 status	17.5.2.24/1225
BMU_VRD_STS0	0x60	EVENT8-0	17.5.2.25/1225
BMU_VRD_STS1	0x64	EVENT8-1	17.5.2.26/1226
BMU_VWR_STS0	0x70	EVENT9-0	17.5.2.27/1226
BMU_VWR_STS1	0x74	EVENT9-1	17.5.2.28/1226
BMU_IR_STS0	0x80	BMU_IR_STS0	17.5.2.29/1226
BMU_IR_STS1	0x84	BMU_IR_STS1	17.5.2.30/1227
BMU_VER_STS0	0x88	Version status 0	17.5.2.31/1228
BMU_VER_STS1	0x8C	Version status 1	17.5.2.32/1228
BMU_OSTD_STS	0x90	OSTD status	17.5.2.33/1228

Register	Offset	Description	Section/Page
BMU_OSTD_CFG	0x94	OSTD configuration	17.5.2.34/1229
BMU_IR_STS2	0x98	BMU_IR_STS2	17.5.2.35/1229
BMU_RD_STS4	0xa0	Read delay monitor	17.5.2.36/1230
BMU_WR_STS4	0xa4	Write delay monitor	17.5.2.37/1230

17.5.2 Register and Field Description

17.5.2.1 BMU_CFG0

- Description: MISC control of BMU
- Offset: 0x0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RG_ADDR_ALN_FLT	RW	Address align filter setting [3:0] for variable counter 0 [7:4] for variable counter 1 Others: reserved [3:0] = 0xf: Select address non 16B align, adr[3:0] != 0 [0] = 1: Select address 16B align, adr[4:0] = 0x10 [1] = 1: Select address 32B align, adr[5:0] = 0x20 [2] = 1: Select address 64B align, adr[6:0] = 0x40 [3] = 1: Select address 128B align, adr[7:0] = 0x80 Value After Reset: 0x0
[15]	RG_CTL_PERIOD_MON_DIV32	RW	Monitor period/div32 Value After Reset: 0x0
[14]	RG_CTL_PERIOD_MON_DIV16	RW	Monitor period/div16 Value After Reset: 0x0
[13]	RG_CTL_PERIOD_MON_DIV8	RW	Monitor period/div8 Value After Reset: 0x0
[12]	RG_CTL_PERIOD_MON_DIV4	RW	Monitor period/div4 Value After Reset: 0x0
[11:9]	RESERVED_1	-	
[8]	RG_CTL_TRIGGER_MODE	RW	[0]: Period monitor mode. Will update monitor data in every rg_ctl_period_mon cycles.

Bits	Field Name	Access	Description
			[1]: Single monitor mode. Monitor only work only one time. Value After Reset: 0x0
[7:3]	RG_CTL_INT_SRC_SEL	RW	Select interrupt source to send to CPU. [0]: Address range hit. [1]: Monitor period expired. [2]: Write target wdata occur. [3]: Error response happened. [4]: Counter overflow. Value After Reset: 0x0
[2]	RG_CTL_MON_CLK_FREE	RW	Monitor clock free on Value After Reset: 0x0
[1]	RG_CTL_MON_EN	RW	Monitor enable [0]: Monitor disable. [1]: Monitor enable. Value After Reset: 0x0
[0]	RG_CTL_SW_RSTN	RW	Monitor sw reset [0]: Monitor in reset mode. [1]: Monitor in active mode. Value After Reset: 0x0

17.5.2.2 BMU_CFG1

- Description: Threshold of duration configuration
- Offset: 0x4
- Default Value: 0x10001

Bits	Field Name	Access	Description
[31:16]	RG_CTL_RD_DURA_THRESHOLD	RW	Threshold for read cmd duration, can't be set to 0. Value After Reset: 0x1
[15:0]	RG_CTL_WR_DURA_THRESHOLD	RW	Threshold for write cmd duration, can't be set to 0. Value After Reset: 0x1

17.5.2.3 BMU_CFG2

- Description: ID configuration of BMU
- Offset: 0x8

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RG_CTL_ID_TARGET	RW	Monitor master target id. Value After Reset: 0x0
[15:0]	RG_CTL_ID_MSK	RW	[15:0]: Per bit ID compare enable 0: Ignore id compare. 1: Compare transaction id with rg_ctl_id_target. Ex: 0xFF00 means only compare target ID[15:8], ignore other bits. Value After Reset: 0x0

17.5.2.4 BMU_CFG3

- Description: Monitor window
- Offset: 0xc
- Default Value: 0x1000000

Bits	Field Name	Access	Description
[31:0]	RG_CTL_PERIOD_MON	RW	Monitor period unit: APB clock cycles Value After Reset: 0x1000000

17.5.2.5 BMU_CFG4

- Description: Filter enable
- Offset: 0x10
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RG_SIZE_FLT	RW	[2:0]: Size filter for variable counter 0 [5:3]: Size filter for variable counter 1 Others: Reserved Value After Reset: 0x0
[15:12]	RG_LEN_FLT_EN	RW	[13:12]: Variable counter1~counter0 burst length filter enable Others: Reserved Value After Reset: 0x0
[11:8]	RG_SIZE_FLT_EN	RW	[9:8]: Variable counter1~counter0 burst size filter enable Others: Reserved

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[7:4]	RG_ADDR_RANGE_FLT_EN	RW	[5:4]: Variable counter1~counter0 address range filter enable Others: Reserved Value After Reset: 0x0
[3:0]	RG_ADDR_ALN_FLT_EN	RW	[1:0]: Variable counter1~counter0 address alignment filter enable Others: Reserved Value After Reset: 0x0

17.5.2.6 BMU_CFG5

- Description: Length filter enable
- Offset: 0x14
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_LEN_FLT	RW	[7:0]: Length filter for variable counter 0 [15:8]: Length filter for variable counter 1 [31:16]: Reserved Value After Reset: 0x0

17.5.2.7 BMU_CFG6

- Description: Upper0 address configuration
- Offset: 0x18
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_UPPER0_ADDRESS	RW	[ADDRMSB-1:0]: Upper0 address [ADDMSB*2-1:ADDMSB]: Upper1 address Others: Reserved Value After Reset: 0x0

17.5.2.8 BMU_CFG7

- Description: Upper1 address configuration
- Offset: 0x1c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_UPPER1_ADDRESS	RW	Value After Reset: 0x0

17.5.2.9 BMU_CFG8

- Description: Upper2 address configuration
- Offset: 0x20
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_UPPER2_ADDRESS	RW	Value After Reset: 0x0

17.5.2.10 BMU_CFG9

- Description: Upper3 address configuration
- Offset: 0x24
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_UPPER3_ADDRESS	RW	Value After Reset: 0x0

17.5.2.11 BMU_FILT

- Description: Duration filter configuration
- Offset: 0x28
- Default Value: 0x300

Bits	Field Name	Access	Description
[31:10]	RESERVED_3	-	
[9]	RG_CTL_WR_BYPASS_LAT_FLT	RW	For write duration over threshold counter bypass cmd filter Value After Reset: 0x1
[8]	RG_CTL_RD_BYPASS_LAT_FLT	RW	For read duration over threshold counter bypass cmd filter Value After Reset: 0x1
[7]	RESERVED_2	-	
[6]	RG_CTL_WR_FILT8TO1	RW	Sample 1 cmd in every 8 cmds for duration with

Bits	Field Name	Access	Description
			threshold monitor Value After Reset: 0x0
[5]	RG_CTL_WR_FILT4TO1	RW	Sample 1 cmd in every 4 cmds for duration with threshold monitor Value After Reset: 0x0
[4]	RG_CTL_WR_FILT2TO1	RW	Sample 1 cmd in every 2 cmds for duration with threshold monitor Value After Reset: 0x0
[3]	RESERVED_1	-	
[2]	RG_CTL_RD_FILT8TO1	RW	Sample 1 cmd in every 8 cmds for duration with threshold monitor Value After Reset: 0x0
[1]	RG_CTL_RD_FILT4TO1	RW	Sample 1 cmd in every 4 cmds for duration with threshold monitor Value After Reset: 0x0
[0]	RG_CTL_RD_FILT2TO1	RW	Sample 1 cmd in every 2 cmds for duration with threshold monitor Value After Reset: 0x0

17.5.2.12 BMU_CFG10

- Description: Lower0 address configuration
- Offset: 0x2c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_LOWER0_ADDRESS	RW	[ADDRMSB-1:0]: Lower0 address for variable counter 0 [ADDMSB*2-1: ADDMSB]: Lower1 address for variable counter 1 Others: Reserved Value After Reset: 0x0

17.5.2.13 BMU_CFG11

- Description: Lower1 address configuration
- Offset: 0x30
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_LOWER1_ADDRESS	RW	Value After Reset: 0x0

17.5.2.14 BMU_CFG12

- Description: Lower2 address configuration
- Offset: 0x34
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_LOWER2_ADDRESS	RW	Value After Reset: 0x0

17.5.2.15 BMU_CFG13

- Description: Lower3 address configuration
- Offset: 0x38
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_LOWER3_ADDRESS	RW	Value After Reset: 0x0

17.5.2.16 BMU_CFG14

- Description: Target data configuration
- Offset: 0x3c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_CTL_TARGET_WDAT	RW	Compare wdata or rdata with “rg_ctl_target_wdat”. Value After Reset: 0x0

17.5.2.17 BMU_RD_STS0

- Description: EVENT2 status
- Offset: 0x40
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_RD_DURATION_CNT	RO	EVENT2, total read duration counter

Bits	Field Name	Access	Description
			Value After Reset: 0x0

17.5.2.18 BMU_RD_STS1

- Description: EVENT0 status
- Offset: 0x44
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_RD_TRANS_CNT	RO	EVENT0, total read transaction number Value After Reset: 0x0

17.5.2.19 BMU_RD_STS2

- Description: EVENT1 status
- Offset: 0x48
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_RD_BYTE_CNT	RO	EVENT1, total read byte number Value After Reset: 0x0

17.5.2.20 BMU_RD_STS3

- Description: EVENT3 status
- Offset: 0x4c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_RD_DURA_W_THR_CNT	RO	EVENT3, the number of read commands that duration over rg_ctrl_rd_dura_threshod Value After Reset: 0x0

17.5.2.21 BMU_WR_STS0

- Description: EVENT6 status
- Offset: 0x50
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_WR_DURATION_CNT	RO	EVENT6, total write duration counter

Bits	Field Name	Access	Description
			Value After Reset: 0x0

17.5.2.22 BMU_WR_STS1

- Description: EVENT4 status
- Offset: 0x54
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_WR_TRANS_CNT	RO	EVENT4, total write transaction number Value After Reset: 0x0

17.5.2.23 BMU_WR_STS2

- Description: EVENT5 status
- Offset: 0x58
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_WR_BYTE_CNT	RO	EVENT5, total write transaction number Value After Reset: 0x0

17.5.2.24 BMU_WR_STS3

- Description: EVENT7 status
- Offset: 0x5c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_WR_DURA_W_THR_CNT	RO	EVENT7, the number of write commands that duration over rg_ctl_wr_dura_threshold Value After Reset: 0x0

17.5.2.25 BMU_VRD_STS0

- Description: EVENT8-0
- Offset: 0x60
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_VRD0_TRANS_CNT	RO	EVENT8-0

Bits	Field Name	Access	Description
			Value After Reset: 0x0

17.5.2.26 BMU_VRD_STS1

- Description: EVENT8-1
- Offset: 0x64
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_VRD1_TRANS_CNT	RO	EVENT8-1 Value After Reset: 0x0

17.5.2.27 BMU_VWR_STS0

- Description: EVENT9-0
- Offset: 0x70
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_VWR0_TRANS_CNT	RO	EVENT9-0 Value After Reset: 0x0

17.5.2.28 BMU_VWR_STS1

- Description: EVENT9-1
- Offset: 0x74
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_VWR1_TRANS_CNT	RO	EVENT9-1 Value After Reset: 0x0

17.5.2.29 BMU_IR_STS0

- Description: BMU_IR_STS0
- Offset: 0x80
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RG_STA_IR_ROSTD_CNT	RO	Indicate the number of read transactions, which was not finished in last monitor period.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[23:16]	RG_STA_IR_WOSTD_CNT	RO	Indicate the number of write transactions, which was not finished in last monitor period. Value After Reset: 0x0
[15]	RESERVED_1	-	
[14:5]	RG_STA_INT_APB_SRC	RO	[0]: Timer expired. [1]: Target wdata or rdata hit occur. [2]: Write error resp occur. [3]: Write duration with threshold FIFO full. (if full need enable cmd filter) [4]: Write duration counter full. [5]: Write transactions from last monitor period is still not finished in the tcurrent monitor period. [6]: Read duration with threshold FIFO full. (if full need enable cmd filter) [7]: Read duration counter full. [8]: Read transactions from last monitor period is still not finished in the current monitor period. [9]: Read error resp occur. Value After Reset: 0x0
[4:1]	RG_CTL_TWDAT_SEL	RW	[0]: Compare target wdat or rdata with wdata[31:0]. [1]: Compare target wdat or rdata with wdata[63:32]. [2]: Compare target wdat or rdata with wdata[95:64]. [3]: Compare target wdat or rdata with wdata[127:96]. Value After Reset: 0x0
[0]	RG_CTL_INT_CLR	RW	1: Clear interrupt, will auto clear to 0 by hardware. Value After Reset: 0x0

17.5.2.30 BMU_IR_STS1

- Description: BMU_IR_STS1
- Offset: 0x84
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_ERR_RESP_ID	RO	[15:0]: Write error resp id [31:16]: Read error resp id

Bits	Field Name	Access	Description
			Value After Reset: 0x0

17.5.2.31 BMU_VER_STS0

- Description: Version status 0
- Offset: 0x88
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_VERSION0	RO	[31:24]: Monitor FIFO depth for write duration [23:16]: Monitor FIFO depth for read duration [15:8]: ID width [7:0]: Address width Value After Reset: 0x0

17.5.2.32 BMU_VER_STS1

- Description: Version status 1
- Offset: 0x8C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_VERSION1	RO	[31:16]: AXI data width [15:8]: Variable counter number [7:0]: AXI length width Value After Reset: 0x0

17.5.2.33 BMU_OSTD_STS

- Description: OSTD status
- Offset: 0x90
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:24]	RG_STA_WR_MAX_OSTD	RO	Maximum write OSTD number in monitor period Value After Reset: 0x0
[23:16]	RG_STA_WR_AVG_OSTD	RO	Average write OSTD in last 8192/4096 cycles in monitor period Value After Reset: 0x0

Bits	Field Name	Access	Description
[15:8]	RG_STA_RD_MAX_OSTD	RO	Maximum read OSTD number in monitor period Value After Reset: 0x0
[7:0]	RG_STA_RD_AVG_OSTD	RO	Average read OSTD in last 8192/4096 cycles in monitor period Value After Reset: 0x0

17.5.2.34 BMU_OSTD_CFG

- Description: OSTD configuration
- Offset: 0x94
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:17]	RESERVED_1	-	
[16]	RG_CTL_OSTD_CNT_MODE	RW	0: 8192 cycle output average OSTD 1: 4096 cycle output average OSTD Value After Reset: 0x0
[15:8]	RG_STA_WR_AVG_OSTD_DBG	RO	Average write OSTD number in every 8192 AXI cycles Value After Reset: 0x0
[7:0]	RG_STA_RD_AVG_OSTD_DBG	RO	Average read OSTD number in every 8192 AXI cycles Value After Reset: 0x0

17.5.2.35 BMU_IR_STS2

- Description: BMU_IR_STS2
- Offset: 0x98
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:18]	RESERVED_2	-	
[17]	RG_STA_INT_WR_HIT	RO	Write cmd hit target address range Value After Reset: 0x0
[16]	RG_STA_INT_RD_HIT	RO	Read cmd hit target address range Value After Reset: 0x0
[15:1]	RESERVED_1	-	
[0]	RG_CTL_DATA_CM_MODE	RW	1: Compare data for read.

Bits	Field Name	Access	Description
			0: Compare data for write. Value After Reset: 0x0

17.5.2.36 BMU_RD_STS4

- Description: Read delay monitor
- Offset: 0xa0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_RD_CMD_DLY_CNT	RO	Read cmd latency, arvalid to aready Value After Reset: 0x0

17.5.2.37 BMU_WR_STS4

- Description: Write delay monitor
- Offset: 0xa4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	RG_STA_WR_CMD_DLY_CNT	RO	Write cmd latency, awvalid to awready Value After Reset: 0x0