TH1520 Audio Processing User Manual

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Revisions

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List of Abbreviations

Abbreviations	Full Spelling	Chinese Explanation

1 Overview

1.1 Features

- Processor Core
  - C906 single-core processor, main frequency 400-812.8512MHz
  - RV64IMA[FD]C[V] instruction architecture
  - 5-stage single-issue in-order pipeline
  - First-level Havard-architectured instruction and data cache, size 32KB, cache behavior 64B;
  - SV39 memory management unit realizes virtual and real address translation and memory management
  - Supports AXI4.0 128-bit master interface
  - Supports CLINT and PLIC
  - Configurable floating-point and vector units
- On-Chip Bus
  - 128-bit AXI4.0 bus, in proportion of 1:N with CPU main frequency
  - One set of AXI master interface and two sets of slave interfaces for communication with AP system and Shared-MEM
  - 32-bit AHB bus and 32-bit APB bus
- DMAC
  - AXI master interface, 16 channels. Supports 8-bit, 16-bit, 32-bit, 64-bit and 128-bit data transfer
  - Maximum block size 65535
  - Supports LLP mode
  - On-Chip Memory
  - Two 128KB single-port SRAMs
- Audio Interface
  - One 8-channel I2S communicates with the external CODEC to sample input audio (16k)
  - Three 2-channel I2S/PCM connect external CODEC to play (16k/32k/48k/44.1k/64k/192k/384k), or via Bluetooth connection (8k/16k/32k/48k/44.1k)
  - Supports low power VAD, supports up to 8-channel I2S or PDM
  - Supports 8-channel PDM communicates with external DMIC for audio acquisition. PDMCLK supports 1.536MHz/768kHz
  - Supports 8-channel TDM/PCM input
  - Two SPDIFs support IN/OUT duplex and Fs 32/44.1/48/88.2/96/192kHz
- Timer Counter
  - One timer, supports linking
  - One WDT
- Other Peripherals

  - One UART, supports flow control, can be used to connect WIFI
  - Two I2Cs, can be used to connect the external CODEC, supports high-speed mode
  - A group of GPIOx30.
- Security Mechanism
  - IOPMP security management module

The master interface of CPU and DMAC comes with security mechanism.

1.2 C906 Interrupt Vector Table

All interrupts in the system are level triggered and active high.

Figure & Table 1-1 Audio CPU interrupt vector table

Interrupt No.	Interrupt Source
0	-
1	WDT
2	AP-MAILBOX
3	DMAC
4	Timer counter 0
5	Timer counter 1
6	Timer counter 2
7	Timer counter 3
8	VAD-FIFO
9	VAD-WK
10	I2S0
11	I2S1
12	I2S2
13	I2S_8CH
14	TDM
15	SPDIF0
16	SPDIF1
17	GPIO
18	I2C0
19	I2C1
20	UART

Interrupt No.	Interrupt Source
21	Bus monitor
22	-
23	NPU_intr[0]
24	NPU_intr[1]
25	NPU_intr[2]
26	AON_REQ (E902)

NOTE

I2S0, I2S1, I2S2, I2S_8CH, TDM, SPDIF0 and SPDIF1 interrupt sources are the OR operation of error interrupt signals and conventional interrupt signals sent by each module.

1.3 CP Output Interrupt Signal Description

The interrupts output by the system are level triggered and active high.

Figure & Table 1-2 CP Output interrupt signal sequence description

Interrupt No.	Interrupt Source
0	-
1	WDT
2	-
3	DMAC
4	Timer counter 0
5	Timer counter 1
6	Timer counter 2
7	Timer counter 3
8	VAD-FIFO
9	VAD-WK
10	I2S0
11	I2S1
12	I2S2
13	I2S_8CH
14	TDM
15	SPDIF0

Interrupt No.	Interrupt Source
16	SPDIF1
17	GPIO
18	I2C0
19	I2C1
20	UART
21	Bus monitor
22	-
23	NPU_intr[0]
24	NPU_intr[1]
25	NPU_intr[2]
26	AON_REQ (E902)
27	-
28	-
29	-

1.4 DMA Handshake Signal Table

Figure & Table 1-3 Audio DMA handshake signal table

DMA Handshake Interface	Peripheral Interface
0	VAD RX0_L
1	VAD RX0_R
2	VAD RX1_L
3	VAD RX1_R
4	VAD RX2_L
5	VAD RX2_R
6	VAD RX3_L
7	VAD RX3_R
8	I2S0 RX
9	I2S0 TX

DMA Handshake Interface	Peripheral Interface
10	I2S1 RX
11	I2S1 TX
12	I2S2 RX
13	I2S2 TX
14	I2S_8CH RX0
15	I2S_8CH RX1
16	I2S_8CH RX2
17	I2S_8CH RX3
18	UART RX
19	UART TX
20	I2C0 RX
21	I2C0 TX
22	I2C1 RX
23	I2C1 TX
24	SPDIF0 RX
25	SPDIF0 TX
26	SPDIF1 RX
27	SPDIF1 TX
28	TDM RX0
29	TDM RX1
30	TDM RX2
31	TDM RX3
32	TDM RX4
33	TDM RX5
34	TDM RX6
35	TDM RX7
36	I2S_8CH TX0
37	I2S_8CH TX1

DMA Handshake Interface	Peripheral Interface
38	I2S_8CH TX2
39	I2S_8CH TX3

1.5 System Address Map

Figure & Table 1-4 Audio system address map

Bus Name	Bus No.	Usage	Start	End	Total Size	Actual Size
AXI SYS	S1	SRAM	0xFF_C000_0000	0xFF_C001_FFFF	128KB	128KB
	S2	SRAM	0xFF_C002_0000	0xFF_C003_FFFF	128KB	128KB
	S3	AHB	0xFF_C800_0000	0xFF_CFFF_FFFF	128MB	128MB
	-	PLIC	0xFF_D000_0000	0xFF_D7FF_FFFF	128MB	128MB
	S4	DDR	0x00_0000_0000	0x03_FFFF_FFFF	16GB	16GB
		AP	0xFF_E100_0000	0xFF_FFFF_FFFF	496MB	496MB
	S5	SRAM	0xFF_E000_0000	0xFF_E0FF_FFFF	16MB	16MB
AHB	S0	DMA	0xFF_C800_0000	0xFF_C800_FFFF	64KB	64KB
	S1/2	RESERVED	0xFF_C801_0000	0xFF_CAFF_FFFF	32MB	32MB
	S3	CPR	0xFF_CB00_0000	0xFF_CB00_FFFF	64KB	64KB
	S4	APBO	0xFF_CB01_0000	0xFF_CB01_FFFF	64KB	64KB
	S5	APB1	0xFF_CB02_0000	0xFF_CB02_FFFF	64KB	64KB
	S6	RESERVED	0xFF_CB03_0000	0xFF_CB03_0FFF	16MB	16MB
APB0	S0	WDT	0xFF_CB01_0000	0xFF_CB01_0FFF	4KB	4KB
	S1	TIMER	0xFF_CB01_1000	0xFF_CB01_1FFF	4KB	4KB
	S2	TDM	0xFF_CB01_2000	0xFF_CB01_2FFF	4KB	4KB
	S3	GPIO	0xFF_CB01_3000	0xFF_CB01_3FFF	4KB	4KB
	S4	I2S0	0xFF_CB01_4000	0xFF_CB01_4FFF	4KB	4KB
	S5	I2S1	0xFF_CB01_5000	0xFF_CB01_5FFF	4KB	4KB
	S6	I2S2	0xFF_CB01_6000	0xFF_CB01_6FFF	4KB	4KB
	S7	I2S-IN	0xFF_CB01_7000	0xFF_CB01_7FFF	4KB	4KB

Bus Name	Bus No.	Usage	Start	End	Total Size	Actual Size
	S8	SPDIF0	0xFF_CB01_8000	0xFF_CB01_8FFF	4KB	4KB
	S9	SPDIF1	0xFF_CB01_9000	0xFF_CB01_9FFF	4KB	4KB
	S10	I2C0	0xFF_CB01_A000	0xFF_CB01_AFFF	4KB	4KB
	S11	I2C1	0xFF_CB01_B000	0xFF_CB01_BFFF	4KB	4KB
	S12	UART	0xFF_CB01_C000	0xFF_CB01_CFFF	4KB	4KB
	S13	IOCtrl	0xFF_CB01_D000	0xFF_CB01_DFFF	4KB	4KB
	S14	VAD	0xFF_CB01_E000	0xFF_CB01_EFFF	4KB	4KB
	S15	RESERVED	0xFF_CB01_F000	0xFF_CB01_FFFF	4KB	4KB
APB1	S0	BSM	0xFF_CB02_0000	0xFF_CB02_0FFF	4KB	4KB
	S1~S13	RESERVED	0xFF_CB02_1000	0xFF_CB02_DFFF	52KB	52KB
	S14	IOPMP0	0xFF_CB02_E000	0xFF_CB02_EFFF	4KB	4KB
	S15	IOPMP1	0xFF_CB02_F000	0xFF_CB02_FFFF	4KB	4KB

2 CPR

2.1 Features

- Supports 32-bit AHB-Lite protocol configuration register
- Supports subsystem clock divider control and module CG control
- Supports module soft reset control
- CPU reset status register, system reset history status register
- Supports version ID read-only register, initial version number 0x00
- Supports CPU low-power mode system CG control
- Supports the mechanism to prevent module access conflict
- After reset, the default output of system clock is a low-speed 24M clock and the bus divider ratio is the default value
- Supports CP communication with external PMU using the four signals as follows:
  - cp_pmu_req/cp_pmu_st[3:0]: CP sends communication request signal and status value to the PMU on the AP side.
  - pmu_cp_req/pmu_cp_st[3:0]: The PMU on the AP side sends communication request signal and status value to CP.
- System control reserved register (initial value 0 or 1, supports bus read and write)

2.2 Block Diagram

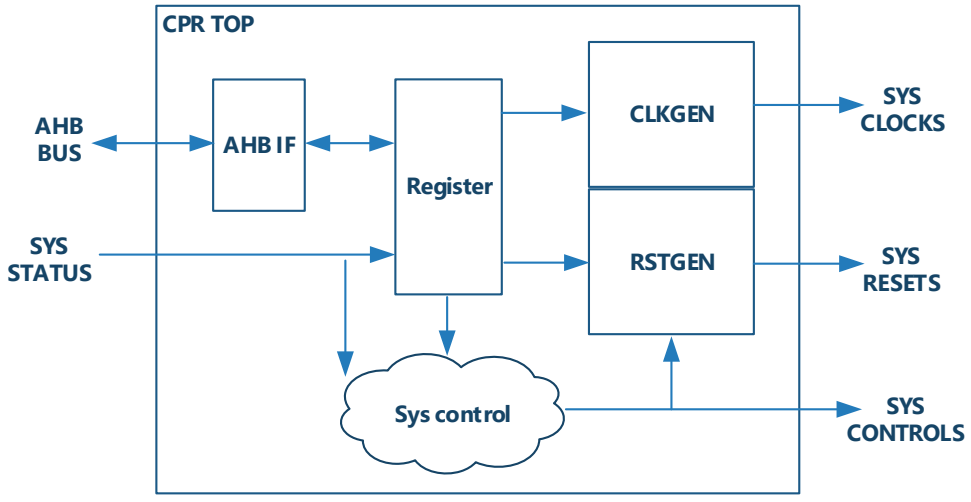


Figure & Table 2-1 Block diagram

2.3 Register

2.3.1 Register Memory Map

The detailed description of SP_CPR_REG registers is shown in Figure & Table 2-2.

Figure & Table 2-2 Memory map of CPR registers

Register	Offset	Width	Access	Reset Value	Description	Section/Page
SYS_CLK_DIV_REG	0x0	32	RW	0x124008	System clock divider select register	2.3.2.1/12
PERI_DIV_SEL_REG	0x4	32	RW	0x3f0725f	Peripheral working clock divider select register	2.3.2.2/14
PERI_CLK_SEL_REG	0x8	32	RW	0x0	Audio peripheral clock source select register	2.3.2.3/16
PERI_CTRL_REG	0xC	32	RW	0x0	Peripheral control register	2.3.2.4/17
IP_CG_REG	0x10	32	RW	0x7	Module CG control register	2.3.2.5/19
IP_RST_REG	0x14	32	RW	0x7ffff10	Module reset control register	2.3.2.6/23
I2S0_BUSY_REG	0x18	32	RW	0x0	I2S0 BUSY status register	2.3.2.7/25
I2S1_BUSY_REG	0x1C	32	RW	0x0	I2S1 BUSY status register	2.3.2.8/26
I2S2_BUSY_REG	0x20	32	RW	0x0	I2S2 BUSY status register	2.3.2.9/26
I2S8CH_BUSY_REG	0x24	32	RW	0x0	I2S-8CH BUSY status register	2.3.2.10/26
SPDIF0_BUSY_REG	0x28	32	RW	0x0	SPDIF0 BUSY status register	2.3.2.11/27
SPDIF1_BUSY_REG	0x2C	32	RW	0x0	SPDIF1 BUSY status register	2.3.2.12/27
TDM_BUSY_REG	0x30	32	RW	0x0	TDM BUSY status register	2.3.2.13/27
I2C0_BUSY_REG	0x34	32	RW	0x0	I2C0 BUSY status register	2.3.2.14/28
I2C1_BUSY_REG	0x38	32	RW	0x0	I2C1 BUSY status register	2.3.2.15/28
UART_BUSY_REG	0x3C	32	RW	0x0	UART BUSY status register	2.3.2.16/28

Register	Offset	Width	Access	Reset Value	Description	Section/Page
TIMER_BUSY_REG	0x40	32	RW	0x0	TIMER BUSY status register	2.3.2.17/28
VAD_BUSY_REG	0x44	32	RW	0x0	VAD BUSY status register	2.3.2.18/29
GPIO_BUSY_REG	0x48	32	RW	0x0	GPIO BUSY status register	2.3.2.19/29
DMA_CH1_BUSY_REG	0x4C	32	RW	0x0	DMA_CH1 BUSY status register	2.3.2.20/29
DMA_CH2_BUSY_REG	0x50	32	RW	0x0	DMA_CH2 BUSY status register	2.3.2.21/30
DMA_CH3_BUSY_REG	0x54	32	RW	0x0	DMA_CH3 BUSY status register	2.3.2.22/30
DMA_CH4_BUSY_REG	0x58	32	RW	0x0	DMA_CH4 BUSY status register	2.3.2.23/30
DMA_CH5_BUSY_REG	0x5C	32	RW	0x0	DMA_CH5 BUSY status register	2.3.2.24/31
DMA_CH6_BUSY_REG	0x60	32	RW	0x0	DMA_CH6 BUSY status register	2.3.2.25/31
DMA_CH7_BUSY_REG	0x64	32	RW	0x0	DMA_CH7 BUSY status register	2.3.2.26/31
DMA_CH8_BUSY_REG	0x68	32	RW	0x0	DMA_CH8 BUSY status register	2.3.2.27/32
DMA_CH9_BUSY_REG	0x6C	32	RW	0x0	DMA_CH9 BUSY status register	2.3.2.28/32
DMA_CH10_BUSY_REG	0x70	32	RW	0x0	DMA_CH10 BUSY status register	2.3.2.29/32
DMA_CH11_BUSY_REG	0x74	32	RW	0x0	DMA_CH11 BUSY status register	2.3.2.30/33
DMA_CH12_BUSY_REG	0x78	32	RW	0x0	DMA_CH12 BUSY status register	2.3.2.31/33
DMA_CH13_BUSY_REG	0x7c	32	RW	0x0	DMA_CH13 BUSY status register	2.3.2.32/33
DMA_CH14_BUSY_REG	0x80	32	RW	0x0	DMA_CH14 BUSY status register	2.3.2.33/34

Register	Offset	Width	Access	Reset Value	Description	Section/Page
DMA_CH15_BUSY_REG	0x84	32	RW	0x0	DMA_CH15 BUSY status register	2.3.2.34/34
DMA_CH16_BUSY_REG	0x88	32	RW	0x0	DMA_CH16 BUSY status register	2.3.2.35/34
SYS_STATUS_REG	0x8c	32	RO	0x0	System status register	2.3.2.36/35
SYS_CTRL_REG	0x90	32	RW	0xff00	System control register	2.3.2.37/36
TESTCLK_CTRL_REG	0x98	32	RW	0x0	Test clock control register	2.3.2.38/37
SYSBUS_CTRL_REG	0x9C	32	RW	0x5384B0	System bus control register	2.3.2.39/39
SYS_ID_REG	0xA0	32	WO	0xFF	System version ID register	2.3.2.40/40
RESERVD1_REG	0xA4	32	RW	0xaaaaaaaa	Reserved register 1	2.3.2.41/40
WKINTR_STATUS_REG	0xA8	32	R/W1C	0x0	Wakeup interrupt status register	2.3.2.42/40
WKINTR_MASK_REG	0xAC	32	RW	0x200	Wakeup interrupt mask register	2.3.2.43/42
MEM_CTRL_REG	0xB0	32	RW	0x0	Memory control register	2.3.2.44/42
DMA_ST0_REG	0xB4	32	RO	0x0	DMA status register 0	2.3.2.45/43
DMA_ST1_REG	0xB8	32	RO	0x0	DMA status register 1	2.3.2.46/44
DMA_ST2_REG	0xBC	32	RO	0x0	DMA status register 2	2.3.2.47/44
DMA_DBG_CTRL_REG	0xC0	32	RW	0x0	DMA debug control register	2.3.2.48/46
PMU_CP_ST_REG	0xC4	32	RW	0x0	AON status sync register	-
CP_PMU_ST_REG	0xC8	32	RW	0x0	CP status sync register	-
RESERVD2_REG	0x100	32	RO	0xaaaaaaaa	Reserved register 2	-

Register	Offset	Width	Access	Reset Value	Description	Section/Page
RESERVD3_REG	0x110	32	RO	0xaaaaaaaa	Reserved register 3	-

2.3.2 Register and Field Description

2.3.2.1 SYS_CLK_DIV_REG [0x0]

- Description: System clock divider select register

Figure & Table 2-3 Register SYS_CLK_DIV_REG description

Bits	Name	Access	Description
31:24	Reserved	RSV	Reserved Reset Value: 0x0
23:20	DMA_DIV	RW	DMA bus clock divider configuration, DMA clock frequency cannot exceed 410MHz. 0: No divider 1: 2 frequency division 2: 3 frequency division 3: 4 frequency division .. 15: 16 frequency division Reset Value: 0x1
19	LPMD_APBCLK_CG	RW	APB clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
18:16	APB_DIV	RW	APB clock divider configuration, only supports even frequency division. 0: No divider 1: 2 frequency division 2: 4 frequency division 3: 6 frequency division .. 7: 14 frequency division Reset Value: 0x2
15	LPMD_AHBCLK_CG	RW	AHB clock CG control 0: Clock off.

Bits	Name	Access	Description
			1: Turn on the clock. Reset Value: 0x0
14:12	AHB_DIV	RW	AHB clock divider configure, only supports even frequency division. 0: No divider 1: 2 frequency division 2: 4 frequency division 3: 6 frequency division .. 7: 14 frequency division Reset Value: 0x3
11	Reserved	RSV	Reserved Reset Value: 0x0
10:8	SYS_DIV	RW	AXI bus clock divider configuration 0: No divider 1: 2 frequency division 2: 3 frequency division 3: 4 frequency division .. 7: 8 frequency division Reset Value: 0x0
7:4	CPU_DIV	RW	CPU clock divider configuration 0: No divider 1: 2 frequency division 2: 3 frequency division 3: 4 frequency division .. 15: 16 frequency division Reset Value: 0x0
3	LPMD_IOPMP_CG	RW	IOPMP clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
2:1	LPMD_SYSCLK_SEL	RW	System clock select after the preconfigured system switches to LPMD.

Bits	Name	Access	Description
			0: sys_clk uses 24MHz, clock on. 1: AXIS bus and SRAM clocks off. 2/3: Clock select and clock gate not change. Reset Value: 0x0
0	SYS_CLK_SEL	RW	CPU clock source select. If LPMD_SYSCLK_SEL is set to 0 and the system enters LPMD, this bit auto changes to 0. 0: 24MHz 1: cp_sys_pll Reset Value: 0x0

2.3.2.2 PERI_DIV_SEL_REG [0x4]

- Description: Peripheral work clock divider register

Figure & Table 2-4 Register PERI_DIV_SEL_REG description

Bits	Name	Access	Description
31:27	Reserved	RSV	Reserved Reset Value: 0x0
26:24	GPIO_CLK_SEL	RW	GPIO debounce clock divider select 0: 1024kHz 1: 512Hz 2: 256Hz 3: 170Hz 4: 128Hz 5: 102Hz 6: 85Hz 7: 73Hz Reset Value: 0x3
23:20	VAD_DIV	RW	VAD mclk clock divider configuration 0: No divider 1: 2 frequency division 2: 3 frequency division 3: 4 frequency division ... 15: 16 frequency division Reset Value: 0x3

Bits	Name	Access	Description
19:18	Reserved	RSV	Reserved Reset Value: 0x0
17	AUDIO_DIV1_CG	RW	AUDIO_DIV1 clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
16:12	AUDIO_DIV1	RW	AUDIO_DIVCLK1 clock divider configuration. This clock is one of the work clock sources of the audio interface. The divider ratio must exceed 4 frequency division and the frequency less than 210MHz. The clock source is CP_SYS_PLL clock. 0~2: Reserved 3: 4 frequency division ... 31: 32 frequency division Reset Value: 0x2
11:10	Reserved	RSV	Reserved Reset Value: 0x0
9	AUDIO_DIV0_CG	RW	AUDIO_DIV0 clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
8:4	AUDIO_DIV0	RW	AUDIO_DIVCLK0 clock divider configuration. This clock is one of the work clock sources of the audio interface. The clock source is CP_AUDIO_PLL clock. 0: No divider 1: 2 frequency division 2: 3 frequency division 3: 4 frequency division ... 31: 32 frequency division Reset Value: 0x2
3:0	UART_DIV	RW	UART work clock divider configuration. The frequency cannot exceed 105MHz. 0: No divider 1: 2 frequency division

Bits	Name	Access	Description
			2: 3 frequency division 3: 4 frequency division ... 15: 16 frequency division Reset Value: 0x7

2.3.2.3 PERI_CLK_SEL_REG [0x8]

- Description: Audio peripheral clock source select register

Figure & Table 2-5 Register PERI_CLK_SEL_REG description

Bits	Name	Access	Description
31:25	Reserved	RSV	Reserved Reset Value: 0x0
24	SPDIF_SRC_SEL	RW	SPDIF src_clk clock source select 0: CP_AUDIO_PLL 1: AUDIO_DIVCLK1 Reset Value: 0x0
23:22	Reserved	RSV	Reserved Reset Value: 0x0
21:20	VAD_MCLK_SEL	RW	VAD mclk clock source select 0: AUDIO_DIVCLK0 1: 24MHz 2: AUDIO_DIVCLK1 3: Reserved Reset Value: 0x0
19:18	Reserved	RSV	Reserved Reset Value: 0x0
17:16	TDM_SRC_SEL	RW	TDM src_clk clock source select 0: AUDIO_DIVCLK0 1: 24MHz 2: AUDIO_DIVCLK1 3: Reserved Reset Value: 0x0
15:14	Reserved	RSV	Reserved Reset Value: 0x0

Bits	Name	Access	Description
13:12	I2S8CH_SRC_SEL	RW	I2S-8CH src_clk clock source select 0: AUDIO_DIVCLK0 1: 24MHz 2: AUDIO_DIVCLK1 3: Reserved Reset Value: 0x0
11:10	Reserved	RSV	Reserved Reset Value: 0x0
9:8	I2S2_SRC_SEL	RW	I2S2 src_clk clock source select 0: AUDIO_DIVCLK0 1: 24MHz 2: AUDIO_DIVCLK1 3: Reserved Reset Value: 0x0
7:6	Reserved	RSV	Reserved Reset Value: 0x0
5:4	I2S1_SRC_SEL	RW	I2S1 src_clk clock source select 0: AUDIO_DIVCLK0 1: 24MHz 2: AUDIO_DIVCLK1 3: Reserved Reset Value: 0x0
3:2	Reserved	RSV	Reserved Reset Value: 0x0
1:0	I2S0_SRC_SEL	RW	I2S0 src_clk clock source select 0: AUDIO_DIVCLK0 1: 24MHz 2: AUDIO_DIVCLK1 3: Reserved Reset Value: 0x0

2.3.2.4 PERI_CTRL_REG [0xC]

- Description: Peripheral control register

Figure & Table 2-6 Register PERI_CTRL_REG description

Bits	Name	Access	Description
31:18	Reserved	RSV	Reserved Reset Value: 0x0
17:16	bsm_sel	RW	Bus monitor select 00: CPU master interface 01: DMA master interface 10: CP2AP master interface 11: Reserved Reset Value: 0x0
15	Reserved	RSV	Reserved Reset Value: 0x0
14	SPDIF_SYNC_EN	RW	SPDIF0/1 module sync enable 0: Disabled 1: Enabled Reset Value: 0x0
13	I2S_SYNC_EN	RW	I2S0/1/2 module sync enable 0: Disabled 1: Enabled Reset Value: 0x0
12	VAD_I2S8CH_SYNC_EN	RW	VAD and I2S-8CH module sync enable 0: Disabled 1: Enabled Reset Value: 0x0
11:9	Reserved	RSV	Reserved Reset Value: 0x0
8	WDT_PAUSE	RW	WDT counter pause control 0: Not pause 1: Pause Reset Value: 0x0
7	CNT4_PAUSE	RW	TIMER counter 4 pause control 0: Not pause 1: Pause Reset Value: 0x0

Bits	Name	Access	Description
6	CNT3_PAUSE	RW	TIMER counter 3 pause control 0: Not pause 1: Pause Reset Value: 0x0
5	CNT2_PAUSE	RW	TIMER counter 2 pause control 0: Not pause 1: Pause Reset Value: 0x0
4	CNT1_PAUSE	RW	TIMER counter 1 pause control 0: Not pause 1: Pause Reset Value: 0x0
3	Reserved	RSV	Reserved Reset Value: 0x0
2	CNT3_4_LINK	RW	TIMER counters 3 and 4 TOGGEL link select 0: Not link 1: Link Reset Value: 0x0
1	CNT2_3_LINK	RW	TIMER counters 2 and 3 TOGGEL link select 0: Not link 1: Link Reset Value: 0x0
0	CNT1_2_LINK	RW	TIMER counters 1 and 2 TOGGEL link select 0: Not link 1: Link Reset Value: 0x0

2.3.2.5 IP_CG_REG [0x10]

- Description: Module CG control register

Figure & Table 2-7 Register IP_CG_REG description

Bits	Name	Access	Description
31:27	Reserved	RSV	Reserved Reset Value: 0x0

Bits	Name	Access	Description
26	IOMUX_CG	RW	IOMUX clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
25	VAD_CG	RW	VAD clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
24	SPDIF1_CG	RW	SPDIF1 clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
23	SPDIF0_CG	RW	SPDIF0 clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
22	GPIO_CG	RW	GPIO clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
21	TDM_CG	RW	TDM clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
20	I2S8CH_CG	RW	I2S-8CH clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
19	I2S2_CG	RW	I2S2 clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
18	I2S1_CG	RW	I2S1 clock CG control 0: Clock off.

Bits	Name	Access	Description
			1: Turn on the clock. Reset Value: 0x0
17	I2S0_CG	RW	I2S0 clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
16	UART_CG	RW	UART clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
15	I2C1_CG	RW	I2C1 clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
14	I2C0_CG	RW	I2C0 clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
13	WDR_CG	RW	WDT clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
12	TIMER_CNT4_CG	RW	TIMER counter 4 clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
11	TIMER_CNT3_CG	RW	TIMER counter 3 clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
10	TIMER_CNT2_CG	RW	TIMER counter 2 clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0

Bits	Name	Access	Description
9	TIMER_CNT1_CG	RW	TIMER counter 1 clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
8	TIMER_CG	RW	TIMER APB clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
7:5	Reserved	RSV	Reserved Reset Value: 0x0
4	BSM_CG	RW	BUS Monitor clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
3	DMA_CG	RW	DMA clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
2	SRAM1_CG	RW	SRAM1 clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x1
1	SRAM0_CG	RW	SRAM0 clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x1
0	CPU_CG	RW	CPU clock CG control. Automatically turned off after entering LPMD. Auto set to 1 after wakeup interrupt is triggered. 0: Clock off. 1: Turn on the clock. Reset Value: 0x1

2.3.2.6 IP_RST_REG [0x14]

- Description: Module reset control register

Figure & Table 2-8 Register IP_RST_REG description

Bits	Name	Access	Description
31:27	Reserved	RSV	Reserved Reset Value: 0x0
26	IOMUX_SRST_N	RW	IOMUX soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
25	VAD_SRST_N	RW	VAD soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
24	SPDIF1_SRST_N	RW	SPDIF1 soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
23	SPDIF0_SRST_N	RW	SPDIF0 soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
22	GPIO_SRST_N	RW	GPIO soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
21	TDM_SRST_N	RW	TDM soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
20	I2S8CH_SRST_N	RW	I2S-8CH soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1

Bits	Name	Access	Description
19	I2S2_SRST_N	RW	I2S2 soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
18	I2S1_SRST_N	RW	I2S1 soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
17	I2S0_SRST_N	RW	I2S0 soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
16	UART_SRST_N	RW	UART soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
15	I2C1_SRST_N	RW	I2C1 soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
14	I2C 0_SRST_N	RW	I2C0 soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
13	WDR_SRST_N	RW	WDT soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
12	TIM_CNT4_SRST_N	RW	TIMER CNT4 soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
11	TIM_CNT3_SRST_N	RW	TIMER CNT3 soft reset 0: Enter reset.

Bits	Name	Access	Description
			1: Release reset. Reset Value: 0x1
10	TIM_CNT2_SRST_N	RW	TIMER CNT2 soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
9	TIM_CNT1_SRST_N	RW	TIMER CNT1 soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
8	TIMER_SRST_N	RW	TIMER APB soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
7:5	Reserved	RSV	Reserved Reset Value: 0x0
4	BSM_SRST_N	RW	BUS Monitor soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x1
3	DMA_SRST_N	RW	DMA soft reset 0: Enter reset. 1: Release reset. Reset Value: 0x0
2:0	Reserved	RSV	Reserved Reset Value: 0x0

2.3.2.7 I2S0_BUSY_REG [0x18]

- Description: I2S0 BUSY status register

Figure & Table 2-9 Register I2S0_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0

Bits	Name	Access	Description
0	I2S0_BUSY	W1C	I2S0 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.8 I2S1_BUSY_REG [0x1C]

- Description: I2S1 BUSY status register

Figure & Table 2-10 Register I2S1_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	I2S1_BUSY	W1C	I2S1 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.9 I2S2_BUSY_REG [0x20]

- Description: I2S2 BUSY status register

Figure & Table 2-11 Register I2S2_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	I2S2_BUSY	W1C	I2S2 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.10 I2S8CH_BUSY_REG [0x24]

- Description: I2S-8CH BUSY status register

Figure & Table 2-12 Register I2S8CH_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	I2S8CH_BUSY	W1C	I2S-8CH BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1.

Bits	Name	Access	Description
			Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.11 SPDIF0_BUSY_REG [0x28]

- Description: SPDIF0 BUSY status register

Figure & Table 2-13 Register SPDIF0_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	SPDIF0_BUSY	W1C	SPDIF0 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.12 SPDIF1_BUSY_REG [0x2C]

- Description: SPDIF1 BUSY status register

Figure & Table 2-14 Register SPDIF1_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	SPDIF1_BUSY	W1C	SPDIF1 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.13 TDM_BUSY_REG [0x30]

- Description: TDM BUSY status register

Figure & Table 2-15 Register TDM_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	TDM_BUSY	W1C	TDM BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.14 I2C0_BUSY_REG [0x34]

- Description: I2C0 BUSY status register

Figure & Table 2-16 Register I2C0_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	I2C0_BUSY	W1C	I2C0 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.15 I2C1_BUSY_REG [0x38]

- Description: I2C1 BUSY status register

Figure & Table 2-17 Register I2C1_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	I2C1_BUSY	W1C	I2C1 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.16 UART_BUSY_REG [0x3C]

- Description: UART BUSY status register

Figure & Table 2-18 Register UART_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	UART_BUSY	W1C	UART BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.17 TIMER_BUSY_REG [0x40]

- Description: TIMER BUSY status register

Figure & Table 2-19 Register TIMER_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	TIMER_BUSY	W1C	TIMER BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.18 VAD_BUSY_REG [0x44]

- Description: VAD BUSY status register

Figure & Table 2-20 Register VAD_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	VAD_BUSY	W1C	VAD BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.19 GPIO_BUSY_REG [0x48]

- Description: GPIO BUSY status register

Figure & Table 2-21 Register GPIO_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	GPIO_BUSY	W1C	GPIO BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.20 DMA_CH1_BUSY_REG [0x4C]

- Description: DMA_CH1 BUSY status register

Figure & Table 2-22 Register DMA_CH1_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH1_BUSY_BUSY	W1C	DMA_CH1 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.21 DMA_CH2_BUSY_REG [0x50]

- Description: DMA_CH2 BUSY status register

Figure & Table 2-23 Register DMA_CH2_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH2_BUSY	W1C	DMA_CH2 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.22 DMA_CH3_BUSY_REG [0x54]

- Description: DMA_CH3 BUSY status register

Figure & Table 2-24 Register DMA_CH3_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH3_BUSY	W1C	DMA_CH3 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.23 DMA_CH4_BUSY_REG [0x58]

- Description: MA_CH4 BUSY status register

Figure & Table 2-25 Register DMA_CH4_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH4_BUSY	W1C	DMA_CH4 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.24 DMA_CH5_BUSY_REG [0x5C]

- Description: DMA_CH5 BUSY status register

Figure & Table 2-26 Register DMA_CH5_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH5_BUSY	W1C	DMA_CH5 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.25 DMA_CH6_BUSY_REG [0x60]

- Description: DMA_CH6 BUSY status register

Figure & Table 2-27 Register DMA_CH6_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH6_BUSY	W1C	DMA_CH6 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.26 DMA_CH7_BUSY_REG [0x64]

- Description: DMA_CH7 BUSY status register

Figure & Table 2-28 Register DMA_CH7_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH7_BUSY	W1C	DMA_CH7 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.27 DMA_CH8_BUSY_REG [0x68]

- Description: DMA_CH8 BUSY status register

Figure & Table 2-29 Register DMA_CH8_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH8_BUSY	W1C	DMA_CH8 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.28 DMA_CH9_BUSY_REG [0x6C]

- Description: DMA_CH9 BUSY status register

Figure & Table 2-30 Register DMA_CH9_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH9_BUSY	W1C	DMA_CH9 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.29 DMA_CH10_BUSY_REG [0x70]

- Description: DMA_CH10 BUSY status register

Figure & Table 2-31 Register DMA_CH10_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH10_BUSY	W1C	DMA_CH10 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.30 DMA_CH11_BUSY_REG [0x74]

- Description: DMA_CH11 BUSY status register

Figure & Table 2-32 Register DMA_CH11_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH11_BUSY	W1C	DMA_CH11 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.31 DMA_CH12_BUSY_REG [0x78]

- Description: DMA_CH12 BUSY status register

Figure & Table 2-33 Register DMA_CH12_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH12_BUSY	W1C	DMA_CH12 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.32 DMA_CH13_BUSY_REG [0x7c]

- Description: DMA_CH13 BUSY status register

Figure & Table 2-34 Register DMA_CH13_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH13_BUSY	W1C	DMA_CH13 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.33 DMA_CH14_BUSY_REG [0x80]

- Description: DMA_CH14 BUSY status register

Figure & Table 2-35 Register DMA_CH14_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH14_BUSY	W1C	DMA_CH14 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.34 DMA_CH15_BUSY_REG [0x84]

- Description: DMA_CH15 BUSY status register

Figure & Table 2-36 Register DMA_CH15_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH15_BUSY	W1C	DMA_CH15 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.35 DMA_CH16_BUSY_REG [0x88]

- Description: DMA_CH16 BUSY status register

Figure & Table 2-37 Register DMA_CH16_BUSY_REG description

Bits	Name	Access	Description
31:1	Reserved	RSV	Reserved Reset Value: 0x0
0	DMA_CH16_BUSY	W1C	DMA_CH16 BUSY bit. The internal value is 0 after reset, returns 0 after read, the internal value becomes 1. Returns 1 after read again. Write 1 to clear this bit. Reset Value: 0x1

2.3.2.36 SYS_STATUS_REG [0x8c]

- Description: System status register

Figure & Table 2-38 Register SYS_STATUS_REG description

Bits	Name	Access	Description
31:17	Reserved	RSV	Reserved Reset Value: 0x0
16	PMU_CP_REQ_INTR	R/W1C	Request interrupt sent by PMU to CP. Set to 1 at the rising edge of pmu_cp_req. Write 1 to clear this bit. Reset Value: 0x0
15:12	CPR_FSM_ST	RO	4'b0000: Default status after reset 4'b0001: RUN 4'b0010: H-VAD 4'b0100: CG 4'b1000: WAKE UP Reset Value: 0x0
11:6	Reserved	RSV	Reserved Reset Value: 0x0
5:4	CPU_LPMD_ST	RO	CPU lower power mode status When CPU executes the WFI instruction, core0_pad_lpmd_b[1:0] is changed accordingly: 0: Lower power mode 1-2: Reserved 3: RUN Reset Value: 0x0
3	WDT_HRST_ST	R/W1C	WDT history reset status. This register cannot be reset. Write 1 to clear bit to 0.

Bits	Name	Access	Description
			0: WDT has not been reset. 1: WDT has been reset. Reset Value: 0x0
2	SYS_HRST_ST	R/W1C	CPU history reset status. This register cannot be reset. Write 1 to clear bit to 0. 0: CPU has not been reset. 1: CPU has been reset. Reset Value: 0x1
1	CPU_HRST_ST	R/W1C	CPU history reset status. This register cannot be reset. Write 1 to clear bit to 0. 0: CPU has not been reset. 1: CPU has been reset. Reset Value: 0x1
0	CPU_RST_ST	RO	CPU reset status 0: CPU is reset. 1: CPU is not reset. Reset Value: 0x0

2.3.2.37 SYS_CTRL_REG [0x90]

- Description: System control register

Figure & Table 2-39 Register SYS_CTRL_REG description

Bits	Name	Access	Description
31:25	Reserved	RSV	Reserved Reset Value: 0x0
24	DBG_REG_EN	RW	Debug register enable 0: Enable the debug register. The debug register value can be read. 1: Disable the debug register. Reset Value: 0x0
23:8	LP_CNT	RW	Low power wait counter. The system can enter the low power mode after waiting for a counting period since CPU enters the low power mode. This counter uses a 24MHz clock to count. Reset Value: 0x00ff
7:4	CP_PMU_ST	RW	Request status sent by CP to AONPMU, defined by

Bits	Name	Access	Description
			software. [7]: SRAM1 reset [6]: SRAM0 reset [5]: SRAM1 low power clock CG enable [4]: SRAM0 low power clock CG enable Reset Value: 0x0
3:1	Reserved	RSV	Reserved Reset Value: 0x0
0	CP_PMU_REQ	RW	Status request sent by CP to AONPMU 0: No request 1: Have request. A level signal will be sent to PMU after 1 is written. Reset Value: 0x0

2.3.2.38 TESTCLK_CTRL_REG [0x98]

- Description: Test clock control register

Figure & Table 2-40 Register TESTCLK_CTRL_REG description

Bits	Name	Access	Description
31:23	Reserved	RSV	Reserved Reset Value: 0x0
22	M12_TESTCLK_CG	RW	12MHz test clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
21	UART_TESTCLK_CG	RW	UART test clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
20	AUDIO_TESTCLK_CG	RSV	AUDIOCLK test clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
19	AXI_TESTCLK_CG	RW	AXI bus test clock CG control 0: Clock off.

Bits	Name	Access	Description
			1: Turn on the clock. Reset Value: 0x0
18	APB_TESTCLK_CG	RSV	APB bus test clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
17	AHB_TESTCLK_CG	RW	AHB bus test clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
16	CPU_TESTCLK_CG	RW	CPU test clock CG control 0: Clock off. 1: Turn on the clock. Reset Value: 0x0
15:13	Reserved	RSV	Reserved Reset Value: 0x0
12:8	AHB_TESTCLK_DIV	RW	Clock configuration after frequency division of AHB main frequency sent by CP to AP. Frequency division factors: 16*(AHB_TESTCLK_DIV)+8 0: 8 frequency division 1: 24 frequency division 2: 40 frequency division ... 31: 504 frequency division Reset Value: 0x0
7:6	Reserved	RSV	Reserved Reset Value: 0x0
5:0	CPU_TESTCLK_DIV	RW	Clock configuration after frequency division of C906 main frequency sent by CP to AP. Frequency division factors: 16*(CPU_TESTCLK_DIV)+8 0: 8 frequency division 1: 24 frequency division 2: 40 frequency division ... 63: 1016 frequency division

Bits	Name	Access	Description
			Reset Value: 0x0

2.3.2.39 SYSBUS_CTRL_REG [0x9C]

- Description: System bus control register

Figure & Table 2-41 Register SYSBUS_CTRL_REG description

Bits	Name	Access	Description
31:28	Reserved	RSV	Reserved Reset Value: 0x0
27:25	SYSBUS_APS_P	RW	AP bus priority (0 to 7). The priority order is as follows: 7>6>5>4>3>2>1>0 Reset Value: 0x0
24:22	SYSBUS_DDR_P	RW	DDR bus priority (0 to 7). The priority order is as follows: 7>6>5>4>3>2>1>0 Reset Value: 0x1
21:19	SYSBUS_PERI_P	RW	Peripheral bus priority (0 to 7). The priority order is as follows: 7>6>5>4>3>2>1>0 Reset Value: 0x2
18:16	SYSBUS_SRAM1_P	RW	SRAM1 bus priority (0 to 7). The priority order is as follows: 7>6>5>4>3>2>1>0 Reset Value: 0x3
15:13	SYSBUS_SRAM0_P	RW	SRAM0 bus priority (0 to 7). The priority order is as follows: 7>6>5>4>3>2>1>0 Reset Value: 0x4
12	Reserved	RSV	Reserved Reset Value: 0x0
11:10	SYSBUS_APM_P	RW	AP Master interface bus priority (0 to 3). The priority order is as follows: 3>2>1>0 Reset Value: 0x1
9:8	Reserved	RSV	Reserved Reset Value: 0x0
7:6	SYSBUS_DMA_P	RW	DMA Master interface bus priority (0 to 3). The priority order is as follows: 3>2>1>0 Reset Value: 0x2
5:4	SYSBUS_CPU_P	RW	CPU Master interface bus priority (0 to 3). The priority

Bits	Name	Access	Description
			order is as follows: 3>2>1>0 Reset Value: 0x3
3:0	Reserved	RSV	Reserved Reset Value: 0x0

2.3.2.40 SYS_ID_REG [0xA0]

- Description: System version ID register

Figure & Table 2-42 Register SYS_ID_REG description

Bits	Name	Access	Description
31:8	Reserved	RSV	Reserved Reset Value: 0x0
7:0	SYS_ID	RO	System version ID, 0xff when reset, 0x00 after reset release Reset Value: 0x00

2.3.2.41 RESERVD1_REG [0xA4]

- Description: Reserved register 1

Figure & Table 2-43 Register RESERVD1_REG description

Bits	Name	Access	Description
31:0	RESERVD1	RW	Reserved register 1 Reset Value: 0xAAAAAAAA

2.3.2.42 WKINTR_STATUS_REG [0xA8]

- Description: Wakeup interrupt status register (after masking)

Figure & Table 2-44 Register WKINTR_STATUS_REG description

Bits	Name	Access	Description
31:27	Reserved	RSV	Reserved Reset Value: 0x0
26:1	wkintr_src_st	R/W1C	Wakeup interrupt source status register. Write 1 to clear bit to 0. 26'd0: Default status after reset. bit[n] = 1: Wakeup interrupt source n is valid. Reset Value: 0x0

Bits	Name	Access	Description
0	Reserved	RSV	Reserved Reset Value: 0x0

NOTE

The list of wakeup interrupt sources is as follows (same as C906, the deleted bits are reserved)

Input Wakeup Interrupt Signal Bit	Interrupt Source
0	Reserved
1	WDT
2	AP-MAILBOX
3	DMAC
4	Timer counter 0
5	Timer counter 1
6	Timer counter 2
7	Timer counter 3
8	VAD-FIFO
9	VAD-WK
10	I2S0
11	I2S1
12	I2S2
13	I2S_8CH
14	TDM
15	SPDIF0
16	SPDIF1
17	GPIO
18	I2C0
19	I2C1
20	UART
21	Bus monitor
22	Reserved

Input Wakeup Interrupt Signal Bit	Interrupt Source
23	NPU[0]
24	NPU[1]
25	NPU[2]
26	PMU_REQ (E902)

2.3.2.43 WKINTR_MASK_REG [0xAC]

- Description: Wakeup interrupt mask register

Figure & Table 2-45 Register WKINTR_MASK_REG description

Bits	Name	Access	Description
31:27	Reserved	RSV	Reserved Reset Value: 0x0
26:1	wk_intr_mask	RW	Wakeup interrupt mask register bit[n] = 0, mask interrupt[n]. Reset Value: 0x0400200
0	Reserved	RSV	Reserved Reset Value: 0x0

2.3.2.44 MEM_CTRL_REG [0xB0]

- Description: Memory control register

Figure & Table 2-46 Register MEM_CTRL_REG description

Bits	Name	Access	Description
31:15	Reserved	RSV	Reserved Reset Value: 0x0
14	VAD_MEM_DSLP	RW	VAD memory deep sleep mode, active high. Reset Value: 0x0
13	VAD_MEM_SLP	RW	VAD memory sleep mode, active high. Reset Value: 0x0
12	VAD_MEM_SD	RW	VAD memory shut down mode, active high. Reset Value: 0x0
11	Reserved	RSV	Reserved Reset Value: 0x0

Bits	Name	Access	Description
10	SRAM1_MEM_DSLP	RW	SRAM1 memory deep sleep mode, active high. Reset Value: 0x0
9	SRAM1_MEM_SLP	RW	SRAM1 memory sleep mode, active high. Reset Value: 0x0
8	SRAM1_MEM_SD	RW	SRAM1 memory shut down mode, active high. Reset Value: 0x0
7	Reserved	RSV	Reserved Reset Value: 0x0
6	SRAM0_MEM_DSLP	RW	SRAM0 memory deep sleep mode, active high. Reset Value: 0x0
5	SRAM0_MEM_SLP	RW	SRAM0 memory sleep mode, active high. Reset Value: 0x0
4	SRAM0_MEM_SD	RW	SRAM0 memory shut down mode, active high. Reset Value: 0x0
3	Reserved	RSV	Reserved Reset Value: 0x0
2	CPU_MEM_DSLP	RW	CPU memory deep sleep mode, active high. The bit auto changes to 0 during C906 run. Reset Value: 0x0
1	CPU_MEM_SLP	RW	CPU memory sleep mode, active high. The bit auto changes to 0 during C906 run. Reset Value: 0x0
0	CPU_MEM_SD	RW	CPU memory shut down mode, active high. The bit auto changes to 0 during C906 run.

NOTE

Three low power modes of memory:

- Deep sleep mode: Peripheral circuits will be powered down and the memory array will retain internal data retention with low voltage.
- Sleep mode: Peripheral circuits will be powered down, with data retention.
- Shut down mode: highest leakage reduction, no data retention.

2.3.2.45 DMA_ST0_REG [0xB4]

- Description: DMA status register 0

Figure & Table 2-47 Register DMA_ST0_REG description

Bits	Name	Access	Description
31:16	debug_ch_wr_arb_req_m1	RO	AXI master interface write arbitration request Reset Value: 0x0
15:0	debug_ch_wr_arb_req_m1	RO	AXI master interface read arbitration request Reset Value: 0x0

The register data comes from the asynchronous clock domain and is not synchronized.

2.3.2.46 DMA_ST1_REG [0xB8]

- Description: DMA status register 1

Figure & Table 2-48 Register DMA_ST1_REG description

Bits	Name	Access	Description
31:30	Reserved	RSV	Reserved Reset Value: 0x0
29:24	debug_grant_index_ar_ch_m1	RO	AXI master interface write address channel arbitration grant Reset Value: 0x0
23:22	Reserved	RSV	Reserved Reset Value: 0x0
21:16	debug_grant_index_aw_ch_m1	RO	AXI master interface read address channel arbitration grant Reset Value: 0x0
15:0	debug_ch_lli_rd_req_m1	RO	AXI master interface LLI arbitration request Reset Value: 0x0

The register data comes from the asynchronous clock domain and is not synchronized.

2.3.2.47 DMA_ST2_REG [0xBC]

- Description: DMA status register 2

Figure & Table 2-49 Register DMA_ST2_REG description

Bits	Name	Access	Description
31	Reserved	RSV	Reserved Reset Value: 0x0
30	mxif_r_ch_idle	RO	AXI master interface read data channel IDLE status Reset Value: 0x0

Bits	Name	Access	Description
29	mxif_b_ch_idle	RO	AXI master interface write data channel IDLE status Reset Value: 0x0
28	debug_ch_src_blk_tfr_done	RO	Source block transfer is done, selected through debug_ch_num. Reset Value: 0x0
27	debug_ch_dst_blk_tfr_done	RO	Destination block transfer is done, selected through debug_ch_num. Reset Value: 0x0
26	debug_ch_blk_tfr_done	RO	Block transfer is done, selected through debug_ch_num. Reset Value: 0x0
25	debug_ch_src_trans_done	RO	Source trans transfer is done, selected through debug_ch_num. Reset Value: 0x0
24	debug_ch_dst_trans_done	RO	Destination trans transfer is done, selected through debug_ch_num. Reset Value: 0x0
23	debug_ch_dma_tfr_done	RO	trans transfer is done, selected through debug_ch_num. Reset Value: 0x0
22	debug_ch_src_trans_req	RO	Source trans transfer request, selected through debug_ch_num. Reset Value: 0x0
21	debug_ch_dst_trans_req	RO	Destination trans transfer request, selected through debug_ch_num. Reset Value: 0x0
20	debug_ch_src_is_in_str	RO	The source state machine is in a single transfer Reset Value: 0x0
19	debug_ch_dst_is_in_str	RO	The destination state machine is in a single transfer Reset Value: 0x0
18	debug_ch_shadowreg_or_lli_invalid_err	RO	- Reset Value: 0x0
17	debug_ch_aborted	RO	DMA channel abort Reset Value: 0x0

Bits	Name	Access	Description
16	debug_ch_suspended	RO	DMA channel suspend Reset Value: 0x0
15:0	debug_ch_lli_rd_req_m1	RO	DMA channel enable Reset Value: 0x0

The register data comes from the asynchronous clock domain and is not synchronized.

2.3.2.48 DMA_DBG_CTRL_REG [0xA0]

- Description: DMA debug channel control register

Figure & Table 2-50 Register DMA_ST2_REG description

Bits	Name	Access	Description
31:4	Reserved	RSV	Reserved Reset Value: 0x0
3:0	dma_dbg_ch	RW	DMA debug channel select register Reset Value: 0x0

The data in this register is output to the asynchronous clock domain, used for debug and not synchronized.

3 I2S

3.1 Features

The I2S bus interface has the following features:

- APB data bus widths of 32 bits
- I2S transmitter and receiver based on the Philips I2S serial protocol
- Serial-master or serial-slave operation
- FIFO – The depth of the transmit and receive FIFO is 32 while the width is 32 bits.
- Programmable FIFO thresholds
- The resolution of the audio data is 16, 24 or 32 bits. IIS can transform data from 16 bits to 24 bits or 32 bits and vice-versa. When I2S works in slave mode, it can auto detect whether the data in transmission is 16 bits, 24 bits or 32 bits.
- DMA Controller Interface – Enables the I2S to interface to a DMA controller over the APB bus using a handshaking interface for transfer requests.
- Independent masking of interrupts and errors – All individual interrupt and error can all be masked independently.
- One combined interrupt line from the I2S to the interrupt controller
- One combined error line from the I2S to the error controller
- Compatible with three serial audio formats: left-justified, I2S, right-justified
- I2s enable signal for multi-blocks synchronous
- Supports audio sample compress.

3.2 Block Diagram

Figure & Table 3-1 illustrates a block diagram of the I2S.

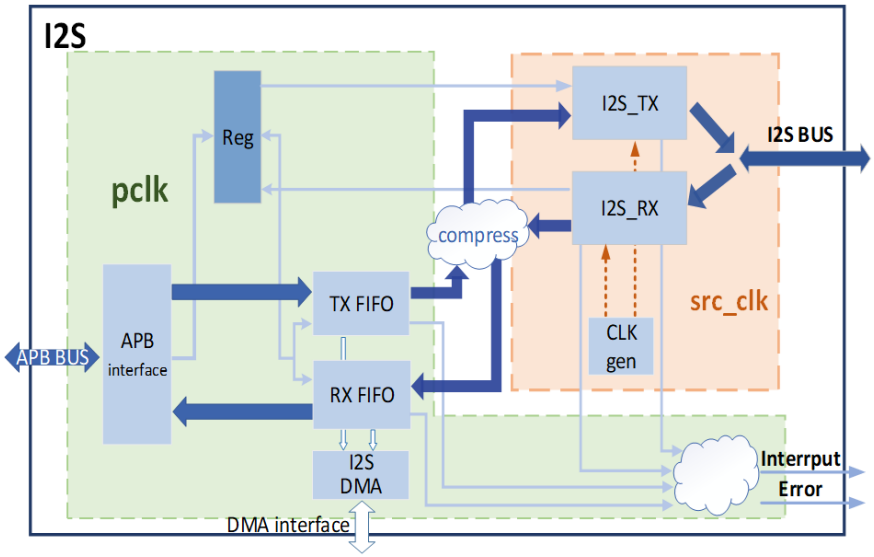


Figure & Table 3-1 Block Diagram of I2S

This I2S module is made up of APB interface, TX FIFO, RX FIFIO, register file, clock generator, receiver, transmitter and DMA interface module.
I2S data path:

- TX: APB Bus --> APB interface --> TX FIFO --> compress --> I2S TX --> I2S BUS
- RX: I2S Bus --> I2S RX --> compress --> RX FIFO --> APB interface --> APB Bus

3.3 Register

3.3.1 Register Memory Map

Figure & Table 3-2 Memory map of I2S

Register	Offset	Width	Access	Description	Section/Page
IISEN	0x00	32 bits	R/W	IIS_IO enable register Reset Value: 0x00	3.3.2.1/49
FUNCMODE	0x04	32 bits	R/W	IIS_IO function mode Reset Value: 0x00	3.3.2.2/50
IISCNF_IN	0x08	32 bits	R/W	IIS interface configuration in (on RX side) Reset Value: 0x00	3.3.2.3/50
FSSTA	0x0C	32 bits	R/W	IIS ATX audio input control/state register Reset Value: 0xf0	3.3.2.4/52
IISCNF_OUT	0x10	32 bits	R/W	IIS interface configuration in (on TX side) Reset Value: 0x00	3.3.2.5/57
FADTLR	0x14	32 bits	R/W	IIS Fs auto detected threshold level register Reset Value: 0x00	3.3.2.6/58
SCCR	0x18	32 bits	R/W	Sample compress control register Reset Value: 0x00	3.3.2.7/59
TXFTLR	0x1C	32 bits	R/W	Transmit FIFO threshold level Reset Value: 0x10	3.3.2.8/62
RXFTLR	0x20	32 bits	R/W	Receive FIFO threshold level Reset Value: 0x10	3.3.2.9/63
TXFLR	0x24	32 bits	R	Transmit FIFO level register Reset Value: 0x00	3.3.2.10/63

Register	Offset	Width	Access	Description	Section/Page
RXFLR	0x28	32 bits	R	Receive FIFO level register Reset Value: 0x00	3.3.2.11/63
SR	0x2C	32 bits	R	Status register Reset Value: 0x0C	3.3.2.12/64
IMR	0x30	32 bits	R/W	Interrupt mask register Reset Value: 0x7F	3.3.2.13/65
ISR	0x34	32 bits	R	Interrupt status register Reset Value: 0x20	3.3.2.14/66
RISR	0x38	32 bits	R	Raw interrupt status register Reset Value: 0x20	3.3.2.15/67
ICR	0x3C	32 bits	W	Interrupt clear register Reset Value: 0x00	3.3.2.16/69
DMACR	0x40	32 bits	R/W	DMA control register Reset Value: 0x00	3.3.2.17/70
DMATDLR	0x44	32 bits	R/W	DMA transmit data level Reset Value: 0x10	3.3.2.18/70
DMARDLR	0x48	32 bits	R/W	DMA receive data level Reset Value: 0x00	3.3.2.19/71
DR	0x4C	32 bits	R/W	FIFO data register Reset Value: 0x00	3.3.2.20/71
DIV0_LEVEL	0x50	32 bits	R/W	Divide source clock, get mclk Reset Value: 0x00	3.3.2.21/72
DIV3_LEVEL	0x54	32 bits	R/W	Divide source clock, get reference clock Reset Value: 0x00	3.3.2.22/72

3.3.2 Register and Field Description

3.3.2.1 IISEN

- Name: I2S enable register
- Description: This register controls the I2S enable, the I2S is enabled and disabled by writing to the I2SEN bit.
- Address Offset: 0x00

Figure & Table 3-3 IISEN field description

Bits	Name	Access	Description
31:1	Reserved and read as zero.		
0	I2SEN	R/W	I2S enable bit 1: Enable 0: Disable (default)

3.3.2.2 FUNCMODE

- Name: Function mode register
- Description: This register controls the function mode, it is impossible to write to this register when I2S is enabled. The MODE bit can only be written when the corresponding MODE_wen is asserted at the same time. A single writing to the MODE bit or the MODE_wen bit is useless and be ignored. Read the MODE_wen bit will always return 0.
- Address Offset: 0x04

Figure & Table 3-4 FUNCMODE field description

Bits	Name	Access	Description
31:2	Reserved and read as zero.		
1	MODE_wen	W	MODE write enable bit 0: The value write to MODE bit invalid. (default) 1: The value write to MODE bit valid.
0	I2S_MODE	R/W	Active level ATX mode 0: Module in receive mode (default) 1: Module in transmit mode

3.3.2.3 IISCNF_IN

- Name: I2S receiver input interface format
- Description: This register controls the IIS input interface format. It is impossible to write to this register when I2S is enabled.
- Address Offset: 0x08

Figure & Table 3-5 IISCNF_IN field description

Bits	Name	Access	Description
31:14	Reserved and read as zero.		
13:12	RDELAY[1]	R/W	I2S receiver s_sclk and s_ws delay level 00: No delay (default) 01: Add 1 src_clk cycle delay

Bits	Name	Access	Description
			10: Add 2 src_clk cycle delay 11: Add 3 src_clk cycle delay
11:9	Reserved and read as zero.		
8	I2S_RXMODE	R/W	I2S receiver operation mode select 0: Slave mode (default) 1: Master mode
7:5	Reserved and read as zero.		
4	RX_VOICE_EN	R/W	I2S sample source type select 0: Source is stereo, has different right and left channel signal. (default) 1: Source is mono, the data of left and right channels are same, only receive and store one of them.
3	-	N/A	Reserved
2	RALOLRC	R/W	Active level of left/right channel 0: Low for left channel (default) 1: High for left channel (Low for right channel)
1:0	RSAFS	R/W	Serial-audio format select 0x0: I2S (default) 0x1: Right-justified 0x2: Left-justified
NOTE [1]: In I2S receiver mode, the SD signal is provided by other devices. It can cause a delay during the signal input by PAD.			

The left channel audio data always comes first, Figure & Table 3-6 shows the I2S bus format when RALOLRC = 1.

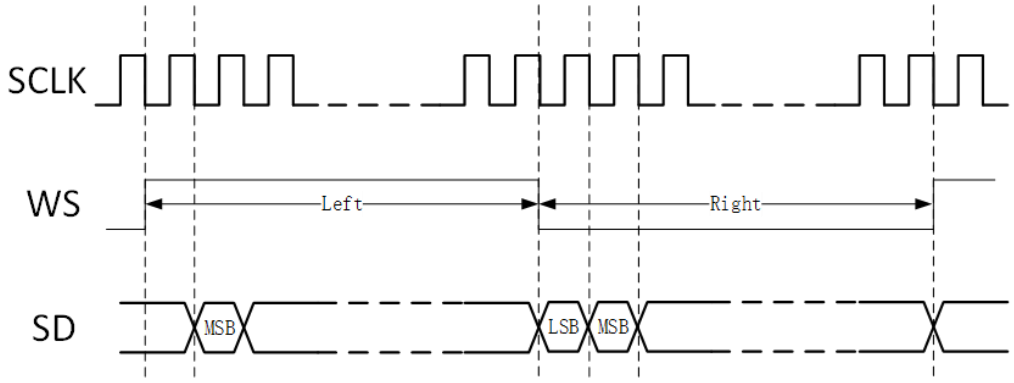


Figure & Table 3-6 I2S standard stereo frame format @ RALOLRC = 1

3.3.2.4 FSSTA

- Name: I2S serial audio input control register
- Description: This register controls the data width mode of I2S and the auto detecting of slave clock. It is impossible to write to this register when I2S is enabled.
- Address Offset: 0x0C

Figure & Table 3-7 FSSTA field description

Bits	Name	Access	Description
31:17	Reserved and read as zero.		
16	MCLK_SEL	R/W	Mclk frequency select 0: mclk = 256*fs (default) 1: mclk = 384*fs
15:14	Reserved and read as zero.		
13:12	SCLK_SEL	R/W	sclk frequency select 00: sclk = 32*fs (default) 01: sclk = 48*fs 1?: sclk = 64*fs
11:8	DATAWTH	R/W	I2S data width mode 0000: 16-bit input/output (both right and left channel) and FIFO store data in 16-bit. (default) 0001: 16-bit input/output (both right and left channel) and FIFO store data in 24-bit. 001?: 16-bit input/output (both right and left channel) and FIFO store data in 32-bit. 0100: 24-bit input/output (both right and left channel) and FIFO store data in 16-bit. 0101: 24-bit input/output (both right and left channel) and FIFO store data in 24-bit. 011?: 24-bit input/output (both right and left channel) and FIFO store data in 32-bit. 1000: 32-bit input/output (both right and left channel) and FIFO store data in 16-bit. 1001: 32-bit input/output (both right and left channel) and FIFO store data in 24-bit. 1?1?: 32-bit input/output (both right and left channel) and FIFO store data in 32-bit.
7:6	ARS	R	Audio rate scale factor (RX mode only) 00: 1 (default)

Bits	Name	Access	Description
			01: 0.5 10: 0.25 11: 0.125 See details in Figure & Table 3-17.
5:4	AFR	R	Input audio fs fundamental rate (RX mode only) 00: 88.2KHz (default) 01: 96KHz 10: 64KHz 11: 192KHz See details in Figure & Table 3-17.
3:1	Reserved and read as zero.		
0	AIRAD	R/W	Audio input rate auto detected bit (RX mode only) 0: No detect (default) 1: Audio input rate is auto detected by hardware (RX mode only)

With FIFO data-width of 32-bit, FIFO store data in 16-bit means that it can store two samples once. FIFO store data in 24-bit and 32-bit means that it can store one sample once. The data width changes as Figure & Table 3-8 to Figure & Table 3-16:

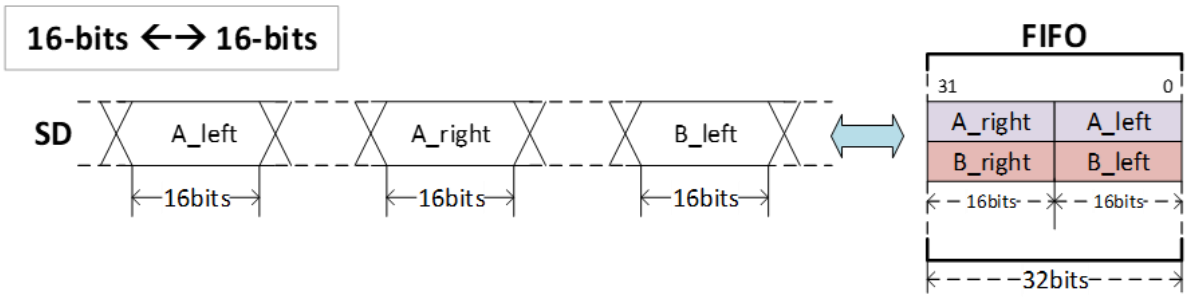


Figure & Table 3-8 16-bit input/output and FIFO store data in 16-bit

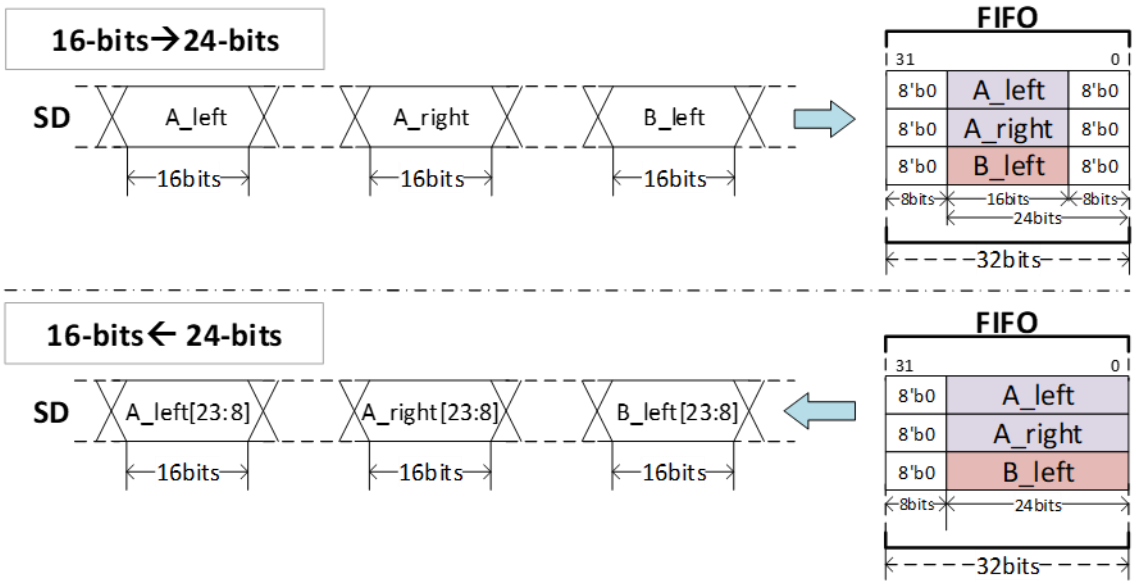


Figure & Table 3-9 16-bit input/output and FIFO store data in 24-bit

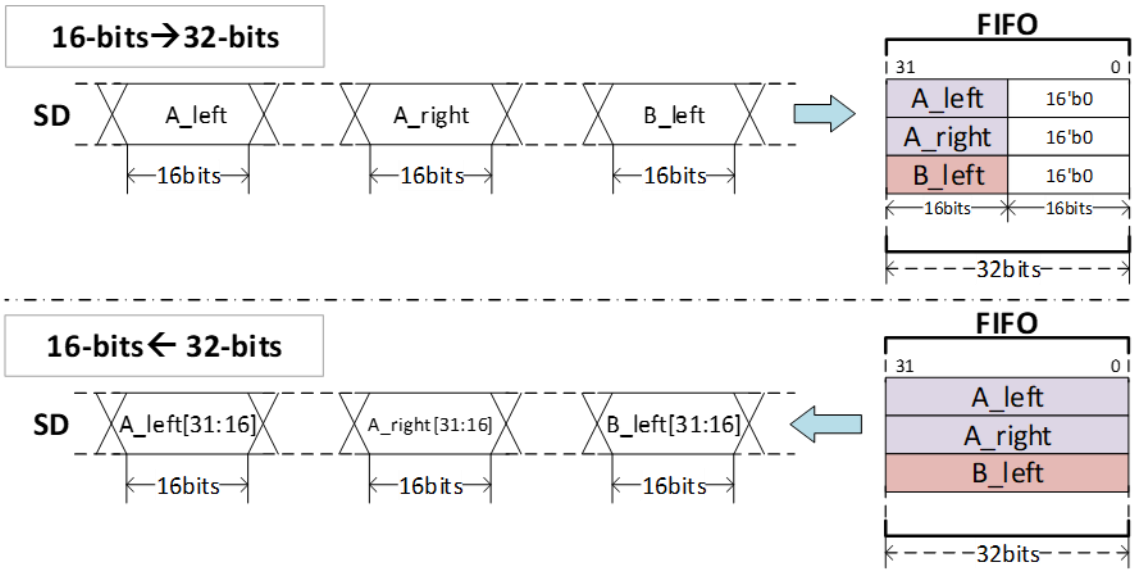


Figure & Table 3-10 16-bit input/output and FIFO store data in 32-bit

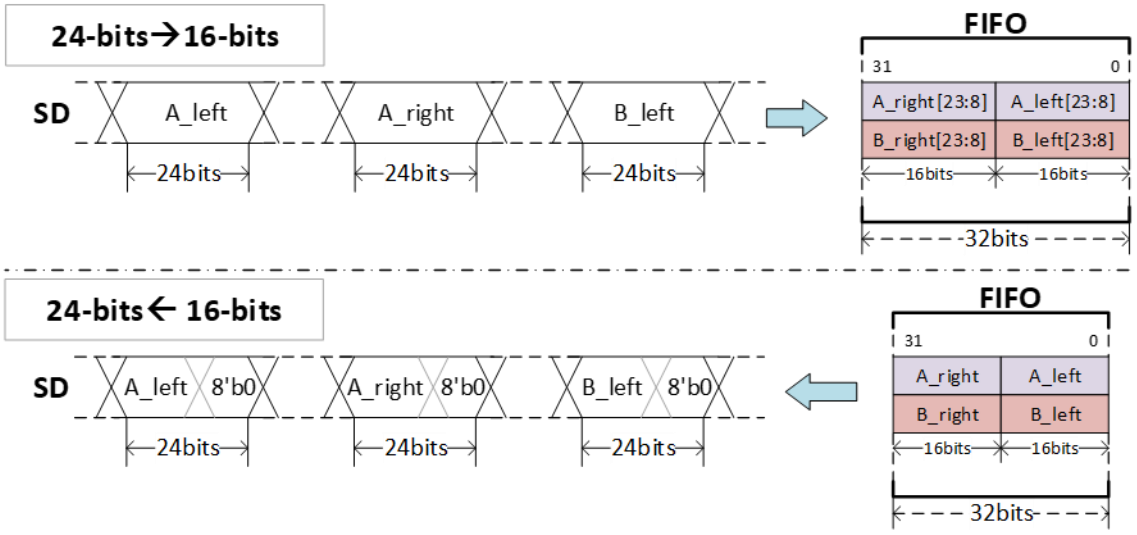


Figure & Table 3-11 24-bit input/output and FIFO store data in 16-bit

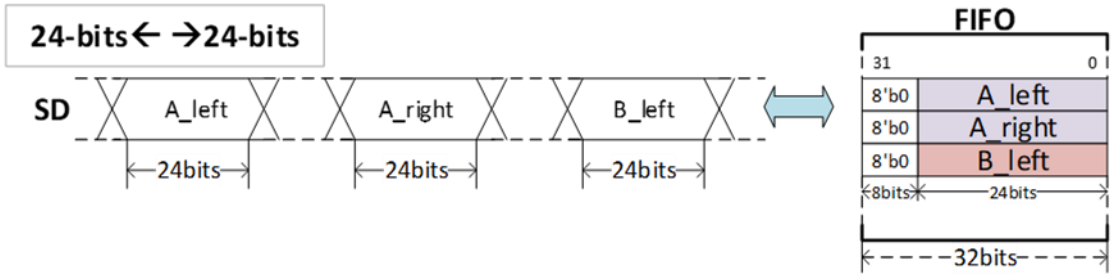


Figure & Table 3-12 24-bit input/output and FIFO store data in 24-bit

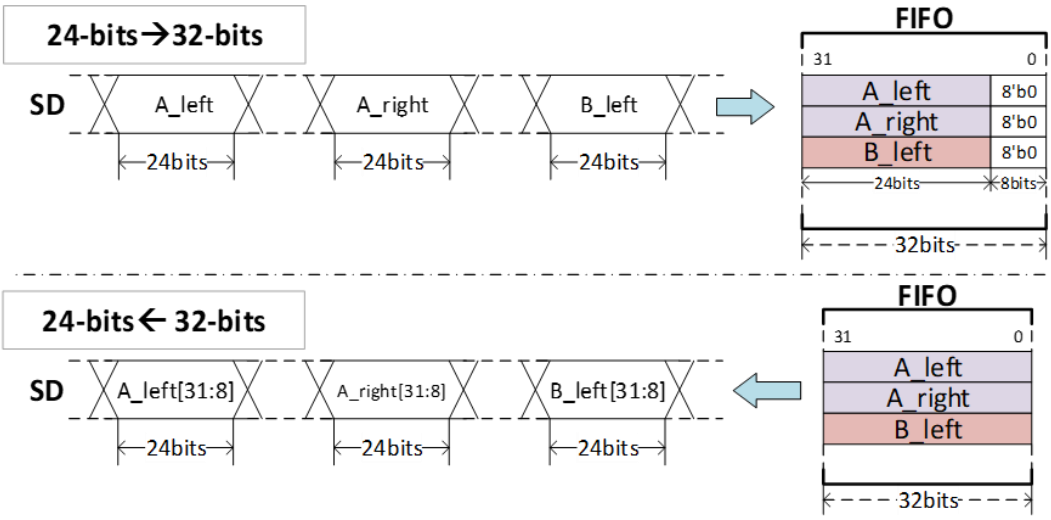


Figure & Table 3-13 24-bit input/output and FIFO store data in 32-bit

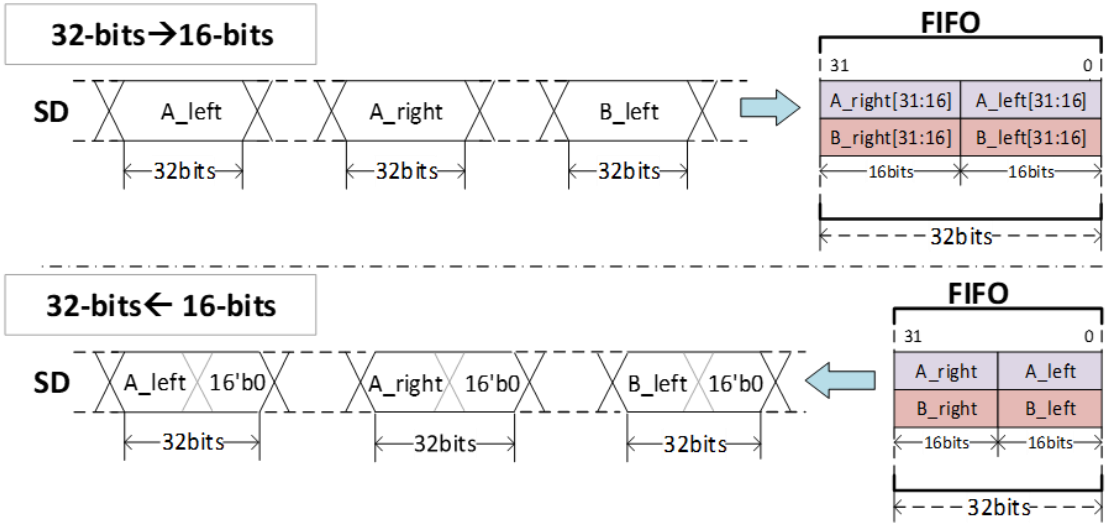


Figure & Table 3-14 32-bit input/output and FIFO store data in 16-bit

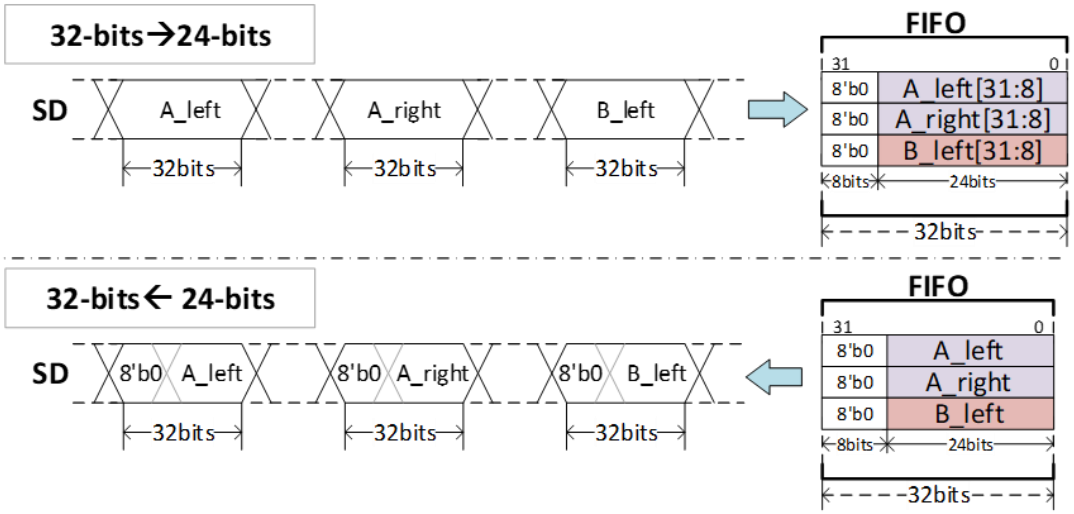


Figure & Table 3-15 32-bit input/output and FIFO store data in 24-bit

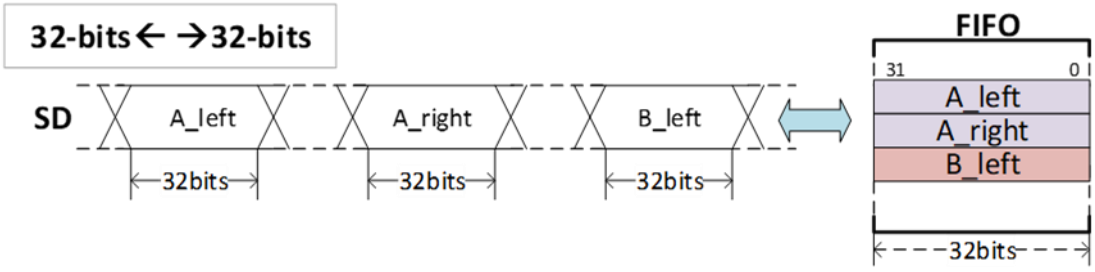


Figure & Table 3-16 32-bit input/output and FIFO store data in 32-bit

The actual value of input sample frequency is resulted from AFR and ARS:

Figure & Table 3-17 Actual input sample frequency

AFR	ARS	Fs (kHz)
2'b00	2'b00	88.2

AFR	ARS	Fs (kHz)
	2'b01	44.1
	2'b10	22.05
	2'b11	11.025
2'b01	2'b00	96
	2'b01	48
	2'b10	24
	2'b11	12
2'b10	2'b00	64
	2'b01	32
	2'b10	16
	2'b11	8
2'b11	2'b00	192
	2'b10	error
	2'b11	default

3.3.2.5 IISCNF_OUT

- Name: I2S transmitter interface format register
- Description: This register controls the I2S output interface format. It is impossible to write to this register when I2S is enabled.
- Address Offset: 0x10

Figure & Table 3-18 IISCNF_OUT field description

Bits	Name	Access	Description
31:5	Reserved and read as zero.		
4	I2S_TXMODE	R/W	TX work mode select signal 0: Chip is master. (default) 1: Chip is slave.
3	TX_VOICE_EN	R/W	Sample source type select 0: Source is stereo, has different right and left channel signal. (default) 1: Source is mono, the data of left and right channels are same, take one data from TX FIFO and extend it into stereo.

Bits	Name	Access	Description
2	TALOLRC	R/W	Active level of left/right channel 0: Low for left channel (default) 1: High for left channel
1:0	TSAFS	R/W	Serial audio format select 0x0: I2S (default) 0x1: Right-justified 0x2: Left-justified

3.3.2.6 FADTLR

- Name: I2S FS auto detection threshold level
- Description: This register reflects the IIS FS auto detection threshold level, which controls the judgement of the input IIS audio sample frequency in receive mode. A quick reference clock between 3.072MHz and 4.032MHz is used to count the period of the input I2S audio FS (s_ws). Through the count value, the input I2S audio sample frequency can be judged. It is impossible to write to this register when IIS is enabled.
- Address Offset: 0x14

Figure & Table 3-19 FADTLR field description

Bits	Name	Access	Description
31:29	Reserved and read as zero.		
28:24	192FTR	R/W	192KHz FS threshold register These bits set the center count of 192kHz FS. 192FTR = ref_clk/192k If the reference clock frequency is 3.072MHz, because 192K*16 = 3.072M, usually this register should be set to 0x10. When the count value is in the range [14, 18], the input I2S audio FS is regarded as 192kHz.
23:22	Reserved and read as zero.		
21:16	64FTR	R/W	64K FS threshold register These bits set the center count of 64kHz, 32kHz, 16kHz and 8kHz FS. 64FTR = ref_clk/64k If the reference clock frequency is 3.072MHz, because 64K*48 = 3.072M, usually this register should be set to 0x30. When the count value is in the range [46, 50], the input I2S fs is regarded as (64*ARS)kHz.
15:14	Reserved and read as zero.		

Bits	Name	Access	Description
13:8	88FTR	R/W	88.2K FS threshold register These bits set the center count of 88.2kHz, 44.1kHz, 22.05kHz and 11.025kHz FS. 88FTR = ref_clk/88.2k If the reference clock frequency is 3.072MHz, because 88.2K*35 = 3.072M, usually this register should be set to 0x23. When the count value is in the range [33, 37], the input I2S fs is regarded as (88.2*ARS)KHz.
7:6	Reserved and read as zero.		
5:0	96FTR	R/W	96K FS threshold register These bits set the center count of 96kHz, 48kHz, 24kHz and 12kHz FS. 96FTR = ref_clk/96k If the reference clock frequency is 3.072MHz, because 96K*32 = 3.072M, this register should be set to 0x20. When the count value is in the range [30, 34], the input I2S FS is regarded as (96*ARS)kHz.

3.3.2.7 SCCR

- Name: I2S sample compress control register
- Description: This register controls the compression of audio sample data.
- Address Offset: 0x18

Figure & Table 3-20 SCCR field description

Bits	Name	Access	Description
31:13	Reserved and read as zero.		
12:8	TVCCR	R/W	TX volume compress control register Based on this register value, right shift the output sample data, the blank bits on the left side are filled with the original MSB, that's bit 15 or bit 23 or bit 31, it depends on the data width (16/24/32-bit). 0: No compress 1: Shift the sample length from 16/24/32 bits to 15/23/31 bits 2: Shift the sample length from 16/24/32 bits to 14/22/30 bits ... 15: Shift the sample length from 16/24/32 bits to

Bits	Name	Access	Description
			1/9/17 bit Else: Shift the sample length from 16/24/32 bits to 0/8/16 bit See Figure & Table 3-21, Figure & Table 3-22, Figure & Table 3-23.
7	Reserved and read as zero.		
6:5	SSRCR	R/W	RX Sub sample rate compress control register Based on this register value, compress the input sample data. 0: No compress 1: Compress the sample data one time, that means discard one of every two samples, receive the first data of two 2: Compress the sample data two times, that means discard two of every three samples, receive the first data of three 3: No compress See Figure & Table 3-24, Figure & Table 3-25, Figure & Table 3-26, Figure & Table 3-27, Figure & Table 3-28 and Figure & Table 3-29.
4:0	RVCCR	R/W	RX volume compress control register Based on this register value, right shift the input sample data, the blank bits on the left side are filled with the original MSB, that's bit 15 or bit 23 or bit 31, it depends on the data width (16/24/32-bit). 0: No compress 1: Shift the sample data from 16/24/32 bits to 15/23/31 bits 2: Shift the sample data from 16/24/32 bits to 14/22/30 bits ... 15: Shift the sample data from 16/24/32 bits to 1/9/17 bit Else: Shift the sample length from 16/24/32 bits to 0/8/16 bit See Figure & Table 3-21, Figure & Table 3-22, Figure & Table 3-23.

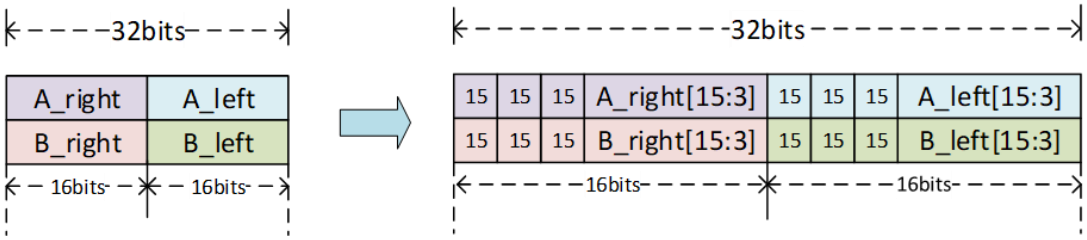


Figure & Table 3-21 Data compress @T/RVCCR = 3, DATAWTH[1:0] = 00

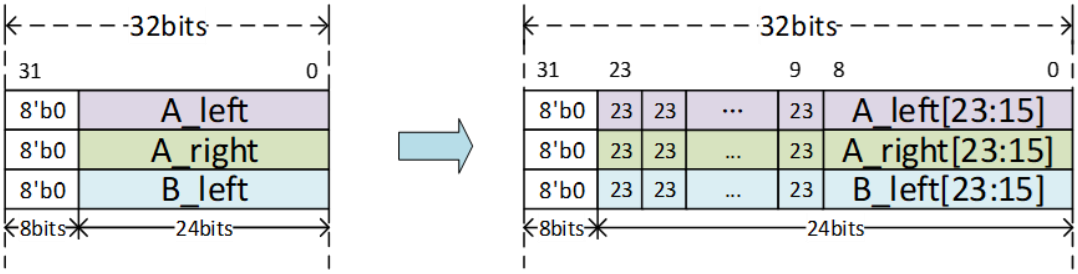


Figure & Table 3-22 Data compress@T/RVCCR = 15, DATAWTH[1:0] = 01

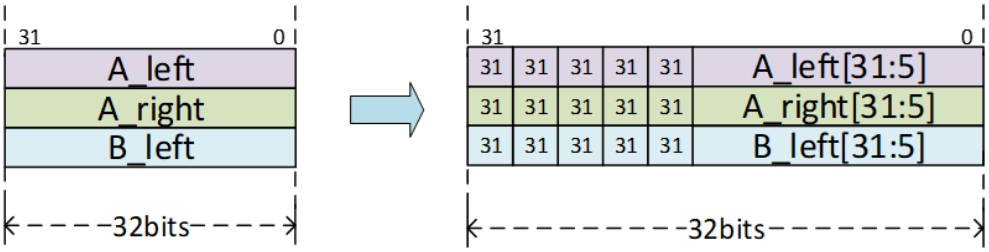


Figure & Table 3-23 Data compress@T/RVCCR = 5, DATAWTH[1:0] = 1?

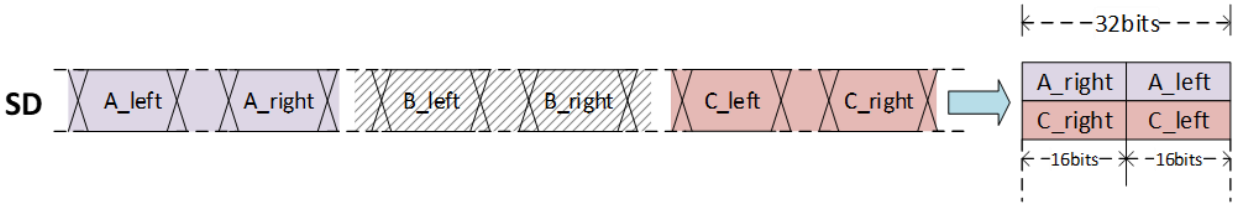


Figure & Table 3-24 Data compress@SSRCR = 1, DATAWTH[1:0] = 00,@stereo source

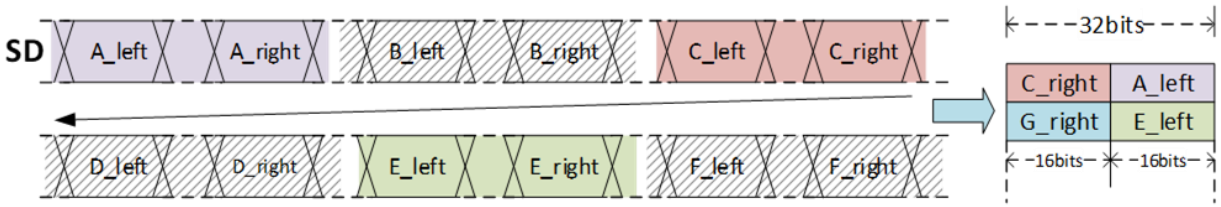


Figure & Table 3-25 Data compress @SSRCR = 1, DATAWTH[1:0] = 00 @mono source

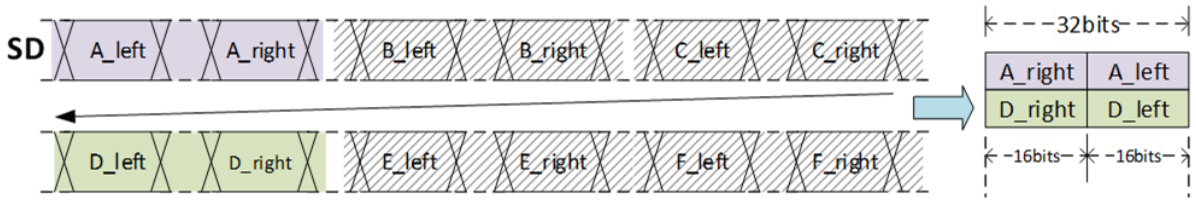


Figure & Table 3-26 Data compress @SSRCR = 2, DATAWTH[1:0] = 00 @stereo source

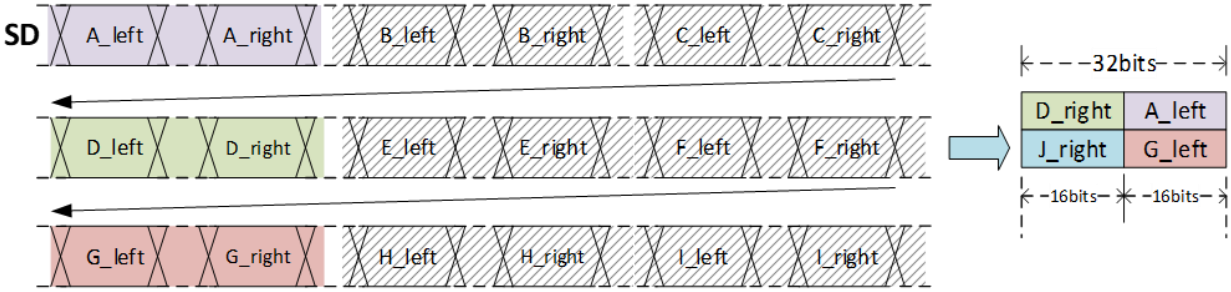


Figure & Table 3-27 Data compress@SSRCR=2, DATAWTH[1:0] = 00 @mono source

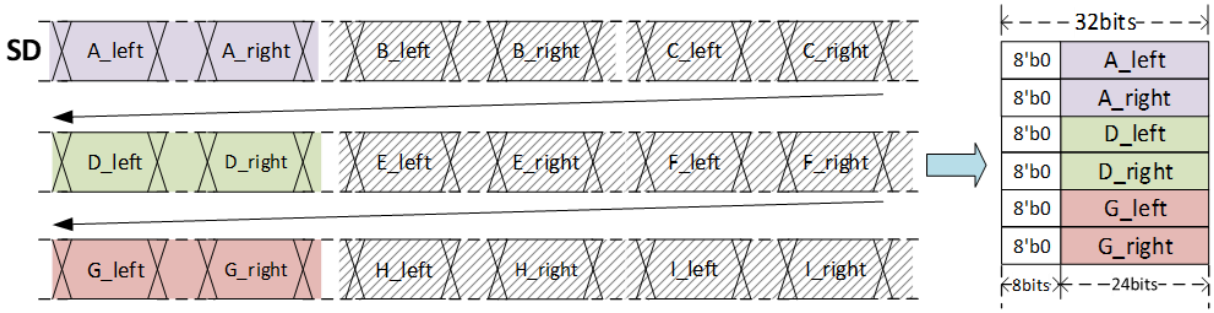


Figure & Table 3-28 Data compress @SSRCR = 2, DATAWTH[1:0] = 01@stereo source

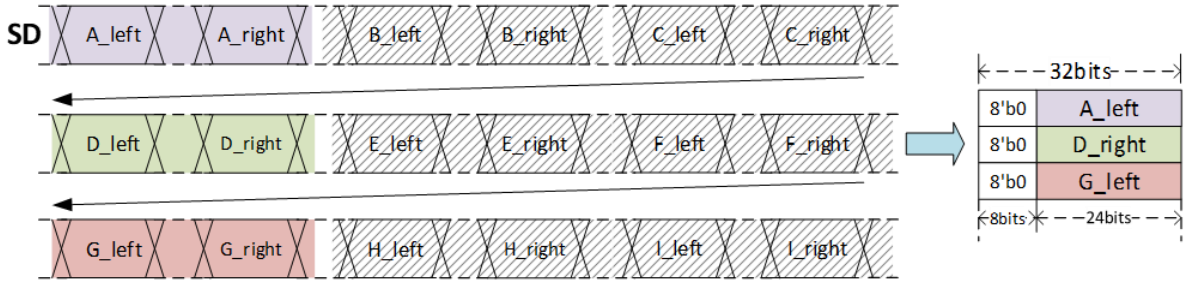


Figure & Table 3-29 Data compress@SSRCR = 2, DATAWTH[1:0] = 01@mono source

3.3.2.8 TXFTLR

- Name: I2S transmit FIFO threshold register
- Description: This register controls the threshold value of the transmit FIFO. It is impossible to write to this register when IIS (or SPDIF) is enabled.
- Address Offset: 0x1C

Figure & Table 3-30 TXFTLR field description

Bits	Name	Access	Description
31:5	Reserved and read as zero.		
4:0	TFT	R/W	Transmit FIFO threshold Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt. The FIFO threshold is configurable in the range 0-31. The default value is 16.

3.3.2.9 RXFTLR

- Name: I2S receive FIFO threshold register
- Description: This register controls the threshold value for the receive FIFO. It is impossible to write to this register when IIS (or SPDIF) is enabled.
- Address Offset: 0x20

Figure & Table 3-31 RXFTLR field description

Bits	Name	Access	Description
31:5	Reserved and read as zero.		
4:0	RFT	R/W	Receive FIFO threshold Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. The FIFO threshold is configurable in the range 1-31, when set to 0, threshold = 32. The default value is 16.

3.3.2.10 TXFLR

- Name: I2S transmit FIFO level register
- Description: This register contains the number of valid data entries in the transmit FIFO.
- Address Offset: 0x24

Figure & Table 3-32 TXFLR field description

Bits	Name	Access	Description
31:6	Reserved and read as zero.		
5:0	TXTFL	R	Transmit FIFO level Contains the current number of valid data entries in the transmit FIFO.

3.3.2.11 RXFLR

- Name: I2S receive FIFO level register

- Description: This register contains the number of valid data entries in the receive FIFO.
- Address Offset: 0x28

Figure & Table 3-33 RXFLR field description

Bits	Name	Access	Description
31:6	Reserved and read as zero.		
5:0	RXTFL	R	Receive FIFO level Contains the current number of valid data entries in the receive FIFO.

3.3.2.12 SR

- Name: I2S state register
- Description: This is a read-only register that is used to indicate the current transfer status, FIFO status, and any transmit/receive error that has occurred.
- Address Offset: 0x2C

Figure & Table 3-34 SR field description

Bits	Name	Access	Description
31:6	Reserved and read as zero.		
5	RFF	R	Receive FIFO Full When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0: Receive FIFO is not full. 1: Receive FIFO is full.
4	RFNE	R	Receive FIFO Not Empty Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. 0: Receive FIFO is empty. 1: Receive FIFO is not empty.
3	TFE	R	Transmit FIFO Empty When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. 0: Transmit FIFO is not empty. 1: Transmit FIFO is empty.

Bits	Name	Access	Description
2	TFNF	R	Transmit FIFO Not Full Set when the transmit FIFO contains one or more empty entries, and is cleared when the FIFO is full. 0: Transmit FIFO is full. 1: Transmit FIFO is not full.
1	TX_BUSY	R	IIS Tx Busy Flag 0: I2S TX is idle or disabled. 1: I2S TX is transmitting data.
0	RX_BUSY	R	IIS Rx Busy Flag 0: I2S RX is idle or disabled. 1: I2S RX is receiving data.

3.3.2.13 IMR

- Name: I2S interrupt mask register
- Description: This read/write register masks or enables all interrupts generated by the I2S.
- Address Offset: 0x3

Figure & Table 3-35 IMR field description

Bits	Name	Access	Description
31:10	Reserved and read as zero.		
9	IFSCM	R/W	Input Sample Frequency Change Mask 0: in_fsc_intr interrupt is masked. (in auto detect mode) (default) 1: in_fsc_intr interrupt is not masked. (in auto detect mode)
8	ITBFCM	R/W	I2S TX Busy Flag Change Mask 0: i2s_txbfc_intr interrupt is masked. (default) 1: i2s_txbfc_intr interrupt is not masked.
7	IRBFCM	R/W	I2S RX Busy Flag Change Mask 0: i2s_rxbfc_intr interrupt is masked. (default) 1: i2s_rxbfc_intr interrupt is not masked.
6	RXFIM	R/W	Receive FIFO Threshold Full Interrupt Mask 0: i2s_rxf_intr interrupt is masked. 1: i2s_rxf_intr interrupt is not masked. (default)

Bits	Name	Access	Description
5	TXEIM	R/W	Transmit FIFO Threshold Empty Interrupt Mask 0: i2s_txe_intr interrupt is masked 1: i2s_txe_intr interrupt is not masked. (default)
4	RXOIM	R/W	Receive FIFO Overflow Error Mask 0: i2s_rxo_err error is masked. 1: i2s_rxo_err error is not masked. (default)
3	RXUIM	R/W	Receive FIFO Underflow Error Mask 0: i2s_rxu_err error is masked. 1: i2s_rxu_err error is not masked. (default)
2	TXOIM	R/W	Transmit FIFO Overflow Error Mask 0: i2s_txo_err error is masked. 1: i2s_txo_err error is not masked. (default)
1	TXUIRM	R/W	Transmit FIFO Underflow Error Mask 0: i2s_txu_err error is masked. 1: i2s_txu_err error is not masked. (default)
0	WADEM	R/W	I2S Wrong Address Error Mask 0: i2s_waddr_err error is masked. 1: i2s_waddr_err error is not masked. (default)

3.3.2.14 ISR

- Name: I2S interrupt status register
- Description: This register indicates the status of the I2S interrupts after they have been masked.
- Address Offset: 0x34

Figure & Table 3-36 ISR field description

Bits	Name	Access	Description
31:10	Reserved and read as zero.		
9	IFSCS	R	Input Sample Frequency Change Interrupt Status after masking 0: in_fsc_intr interrupt is activated. (in auto detect mode) 1: in_fsc_intr interrupt is not activated. (in auto detect mode)

Bits	Name	Access	Description
8	ITBFCS	R	I2S TX Busy Flag Change Interrupt Status after masking 0: i2s_txbfc_intr interrupt is activated. 1: i2s_txbfc_intr interrupt is not activated.
7	IRBFCS	R	I2S RX Busy Flag Change Interrupt Status after masking 0: i2s_rxbfc_intr interrupt is activated. 1: i2s_rxbfc_intr interrupt is not activated.
6	RXFIS	R	Receive FIFO Threshold Full Interrupt Status after masking 0: i2s_rxf_intr interrupt is not activated. 1: i2s_rxf_intr interrupt is activated.
5	TXEIS	R	Transmit FIFO Threshold Empty Interrupt Status after masking 0: i2s_txe_intr interrupt is not activated. 1: i2s_txe_intr interrupt is activated.
4	RXOIS	R	Receive FIFO Overflow Error Status after masking 0: i2s_rxo_err error is not activated. 1: i2s_rxo_err error is activated.
3	RXUIS	R	Receive FIFO Underflow Error Status after masking 0: i2s_rxu_err error is not activated. 1: i2s_rxu_err error is activated.
2	TXOIS	R	Transmit FIFO Overflow Error Status after masking 0: i2s_txo_err error is not activated. 1: i2s_txo_err error is activated.
1	TXUIRS	R	Transmit FIFO Underflow Error Status after masking 0: i2s_txu_err error is not activated. 1: i2s_txu_err error is activated.
0	WADES	R	I2S wrong address Error Status after masking 0: i2s_waddr_err error is not activated. 1: i2s_waddr_err error is activated.

3.3.2.15 RISR

- Name: I2S raw interrupt status register
- Description: This read-only register reports the status of the IIS interrupts prior to masking.
- Address Offset: 0x38

Figure & Table 3-37 RISR field description

Bits	Name	Access	Description
31:10	Reserved and read as zero.		
9	RIFSCS	R	Input Sample Frequency Change Raw Interrupt Status prior to masking 0: in_fsc_intr interrupt is activated. (in auto detect mode) 1: in_fsc_intr interrupt is not activated. (in auto detect mode)
8	RITBFCS	R	I2S TX Busy Flag Change Raw Interrupt Status prior to masking 0: i2s_txbfc_intr interrupt is activated. 1: i2s_txbfc_intr interrupt is not activated.
7	RIRBFCS	R	I2S RX Busy Flag Change Raw Interrupt Status prior to masking 0: i2s_rxbfc_intr interrupt is activated. 1: i2s_rxbfc_intr interrupt is not activated.
6	RXFIR	R	Receive FIFO Threshold Full Raw Interrupt Status prior to masking 0: i2s_rxf_intr interrupt is not activated. 1: i2s_rxf_intr interrupt is activated.
5	TXEIR	R	Transmit FIFO Threshold Empty Raw Interrupt Status prior to masking 0: i2s_txe_intr interrupt is not activated. 1: i2s_txe_intr interrupt is activated prior to masking.
4	RXOIR	R	Receive FIFO Overflow Raw Error Status prior to masking 0: i2s_rxo_err interrupt is not activated. 1: i2s_rxo_err error is activated.
3	RXUIR	R	Receive FIFO Underflow Raw Error Status prior to masking 0: i2s_rxu_err error is not activated. 1: i2s_rxu_err error is activated.
2	TXOIR	R	Transmit FIFO Overflow Raw Error Status prior to masking 0: i2s_txo_err error is not activated 1: i2s_txo_err error is activated.

Bits	Name	Access	Description
1	TXUIR	R	Transmit FIFO Underflow Raw Error Status prior to masking 0: i2s_txu_err error is not activated. 1: i2s_txu_err error is activated.
0	RWADES	R	I2S wrong address Raw Error Status prior to masking 0: i2s_waddr_err error is not activated. 1: i2s_waddr_err error is activated.

3.3.2.16 ICR

- Name: I2S interrupt clear register
- Description: This write-only register is used to clear IIS interrupts.
- Address Offset: 0x3C

Figure & Table 3-38 ICR field description

Bits	Name	Access	Description
31:10	Reserved and read as zero.		
9	CRIFSC	W	Clear Input Sample Frequency Change Interrupt 0: Not clear in_fsc_intr interrupt. 1: Clear in_fsc_intr interrupt.
8	CRITBFC	W	Clear I2S TX Busy Flag Change Interrupt 0: Not clear i2s_txbfc_intr interrupt. 1: Clear i2s_txbfc_intr interrupt.
7	CRIRBFC	W	Clear I2S RX Busy Flag Change Interrupt 0: Not clear i2s_rxbfc_intr interrupt. 1: Clear i2s_rxbfc_intr interrupt.
6	RXFIC	W	Clear Receive FIFO Threshold Full Interrupt 0: Not clear i2s_rxf_intr interrupt. 1: Clear i2s_rxf_intr interrupt.
5	TXEIC	W	Clear Transmit FIFO Threshold Empty Interrupt 0: Not clear i2s_txe_intr interrupt. 1: Clear i2s_txe_intr interrupt.
4	RXOIC	W	Clear Receive FIFO Overflow Error 0: Not clear i2s_rxo_err error. 1: Clear i2s_rxo_err error.

Bits	Name	Access	Description
3	RXUIC	W	Clear Receive FIFO Underflow Error 0: Not clear i2s_rxu_err interrupt. 1: Clear i2s_rxu_err interrupt.
2	TXOIC	W	Clear Transmit FIFO Overflow Error Status 0: Not clear i2s_txo_err interrupt. 1: Clear i2s_txo_err interrupt.
1	TXUIC	W	Clear Transmit FIFO Underflow Error 0: Not clear i2s_txu_err interrupt. 1: Clear i2s_txu_err interrupt.
0	CWADEC	W	Clear I2S wrong address Error 0: Not clear i2s_waddr_err interrupt. 1: Clear i2s_waddr_err interrupt.

3.3.2.17 DMACR

- Name: I2S DMA control register
- Description: The register is used to enable the DMA controller interface operation.
- Address Offset: 0x40

Figure & Table 3-39 DMACR field description

Bits	Name	Access	Description
31:2	Reserved and read as zero.		
1	TDMAE	R/W	Transmit DMA Enable This bit enables/disables the transmit FIFO DMA channel. 0: Transmit DMA disabled. (default) 1: Transmit DMA enabled.
0	RDMAE	R/W	Receive DMA Enable This bit enables/disables the receive FIFO DMA channel. 0: Receive DMA disabled. (default) 1: Receive DMA enabled.

3.3.2.18 DMATDLR

- Name: I2S DMA transmit data level register
- Description: This register controls the I2S DMA transmit data level.

- Address Offset: 0x44

Figure & Table 3-40 DMATDLR field description

Bits	Name	Access	Description
31:5	Reserved and read as zero.		
4:0	DMATDL	R/W	Transmit Data Level This bit field controls the level at which a DMA request is made by the transmit logic. The watermark level = DMATDL; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1. The default value is 16, it can be configured in the range 0-31. When set to 0, threshold =32.

3.3.2.19 DMARDLR

- Name: I2S DMA receive data level register
- Description: This register controls the I2S DMA receive data level.
- Address Offset: 0x48

Figure & Table 3-41 DMARDLR field description

Bits	Name	Access	Description
31:5	Reserved and read as zero.		
4:0	DMARDL	R/W	DMA Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value, and RDMAE = 1. The default value is 0, it can be configured in the range 1-31. When set to 0, threshold = 32.

3.3.2.20 DR

- Name: I2S DMA transmit data level register
- Description: The IIS data register is a 32-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when I2SEN = 1. FIFOs are reset when I2SEN = 0.
- Address Offset: 0x4C

Figure & Table 3-42 DR field description

Bits	Name	Access	Description
31: 0	DR	R/W	Data Register Data of the right channel. Read: Receive FIFO buffer Write: Transmit FIFO buffer

3.3.2.21 DIV0_LEVEL

- Name: I2S divider0 control register
- Description: Write to this register as a divider divide src_clk then get mclk.
- Address Offset: 0x50

Figure & Table 3-43 DIV0_LEVEL field description

Bits	Name	Access	Description
31:8	Reserved and read as zero.		
7:0	DIV0	R/W	A divider for getting mclk from src_clk 0: No divide (default) Else: divide = DIV0

3.3.2.22 DIV3_LEVEL

- Name: I2S divider3 control register
- Description: Write to this register as a divider which divide src_clk then get ref_clk.
- Address Offset: 0x54

Figure & Table 3-44 DIV3_LEVEL field description

Bits	Name	Access	Description
31:8	Reserved and read as zero.		
7:0	DIV3	R/W	A divider for getting ref_clk from src_clk divide = (DIV3+1)*2

4 TDM

4.1 Features

- Supports TDM receive function.
- Supports master and slave modes.
- Supports 16/24/32-bit data width.
- Up to 8-channel data. Offet can be configured separately.
- Eight 32-bit FIFOs with depth of 8. The threshold is configurable.
- DMA handshake signal

4.2 Operating Mode

1. System configuration:
   a) Configure PLL_frac frequency, the default is 49.152MHz.
   b) Configure PIN MUX.
   c) Open TDM CG.
2. Configure the control registers: TDMCTL, DIV0_LEVEL, CHOFFSET1, CHOFFSET2, CHOFFSET3 and CHOFFSET4.
3. Configure FIFO registers: FIFOTL1, FIFOTL2, FIFOTL3, and FIFOTL4.
4. Configure interrupt registers: TDM_IMR, TDM_ICR.
5. Configure DMA handshake signal registers: TDM_DMACTL, TDM_DMADL.
6. Enable TDM, set TDMEN to 0x1, and start operating.

4.3 Register

4.3.1 Register Memory Map

Figure & Table 4-1 Memory map of TDM registers

Register	Offset	Reset Value	Description	Section/Page
TDMEN	0x00	0x00000000	TDM enable register	4.3.2.1/74
TDMCTL	0x04	0x00000010	TDM control register	4.3.2.2/75
CHOFFSET1	0x08	0x00000000	TDM channel OFFSET register 1	4.3.2.3/77
CHOFFSET2	0x0C	0x00000000	TDM channel OFFSET register 2	4.3.2.4/78
CHOFFSET3	0x10	0x00000000	TDM channel OFFSET register 3	4.3.2.5/78
CHOFFSET4	0x14	0x00000000	TDM channel OFFSET register 4	4.3.2.6/79
FIFOTL1	0x18	0x00000000	TDM FIFO interrupt threshold register	4.3.2.7/80

Register	Offset	Reset Value	Description	Section/Page
			1	
FIFOTL2	0x1C	0x00000000	TDM FIFO interrupt threshold register 2	4.3.2.8/81
FIFOTL3	0x20	0x00000000	TDM FIFO interrupt threshold register 3	4.3.2.9/81
FIFOTL4	0x24	0x00000000	TDM FIFO interrupt threshold register 4	4.3.2.10/82
TDM_SR	0x28	0x00000000	TDM status register	4.3.2.11/82
TDM_IMR	0x2C	0x777777FE	TDM interrupt&error mask register	4.3.2.12/84
TDM_ISR	0x30	0x00000000	TDM interrupt&error status register	4.3.2.13/86
TDM_RISR	0x34	0x00000000	TDM interrupt&error raw status register	4.3.2.14/89
TDM_ICR	0x38	0x00000000	TDM interrupt&error clear register	4.3.2.15/92
TDM_DMAEN	0x3C	0x00000000	TDM DMA handshake signal enable register	4.3.2.16/93
TDM_DMADL	0x40	0x00000004	TDM DMA handshake signal FIFO threshold register	4.3.2.17/94
LDR1	0x44	0x00000000	Left channel 1 data access register	4.3.2.18/94
RDR1	0x48	0x00000000	Right channel 1 data access register	4.3.2.19/94
LDR2	0x4C	0x00000000	Left channel 2 data access register	4.3.2.20/94
RDR2	0x50	0x00000000	Right channel 2 data access register	4.3.2.21/95
LDR3	0x54	0x00000000	Left channel 3 data access register	4.3.2.22/95
RDR3	0x58	0x00000000	Right channel 3 data access register	4.3.2.23/95
LDR4	0x5C	0x00000000	Left channel 4 data access register	4.3.2.24/95
RDR4	0x60	0x00000000	Right channel 4 data access register	4.3.2.25/95
DIV0_LEVEL	0x64	0x00000000	Divider configuration register	4.3.2.26/96

4.3.2 Register and Field Description

4.3.2.1 TDMEN_REG

- Name: TDMEN_REG
- Address Offset: 0x00
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:1	RESERVED	RO	Reserved
0	TDMEN	WO	TDM enable 0x0: TDM is disabled. 0x1: TDM is enabled.

4.3.2.2 TDMCTL_REG

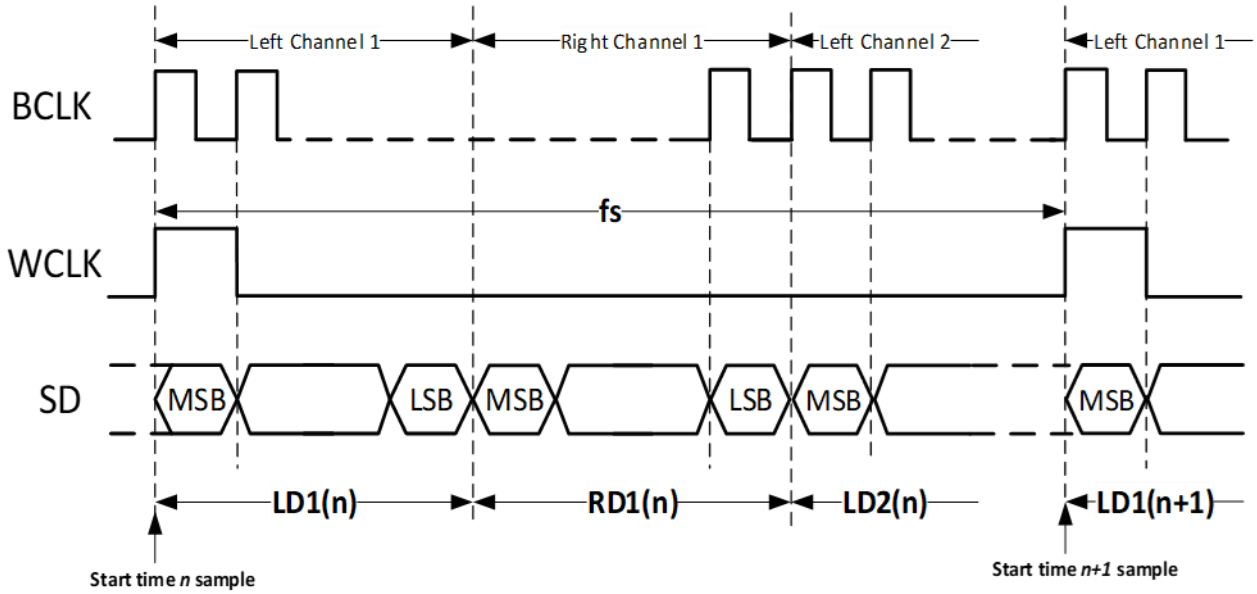
- Name: TDMCTL_REG
- Address Offset: 0x04
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:14	RESERVED	RO	Reserved
13	SPEDGE	R/W	Bclk transmit data edge 0x0: Rising edge 0x1: Falling edge
12	CHORD	R/W	Left and right channel order 0x0: Left channel comes first. 0x1: Right channel comes first.
11:10	RESERVED	RO	Reserved
9:8	CHNUM	R/W	Number of channels 0x0: 2 channels 0x1: 4 channels 0x2: 6 channels 0x3: 8 channels
7:6	RESERVED	RO	Reserved
5:4	DATAWTH	R/W	Data width select 0x0: 16-bit input, two data spliced into one 32-bit data and stored in FIFO. 0x1: 16-bit input, the upper 16 bits are filled with 0s to be 32-bit data and stored in FIFO. 0x2: 24-bit input, the upper eight bits are filled with 0s to be 32-bit data and stored in FIFO. 0x3: 32-bit input, stored in FIFO directly.
3:1	RESERVED	RO	Reserved

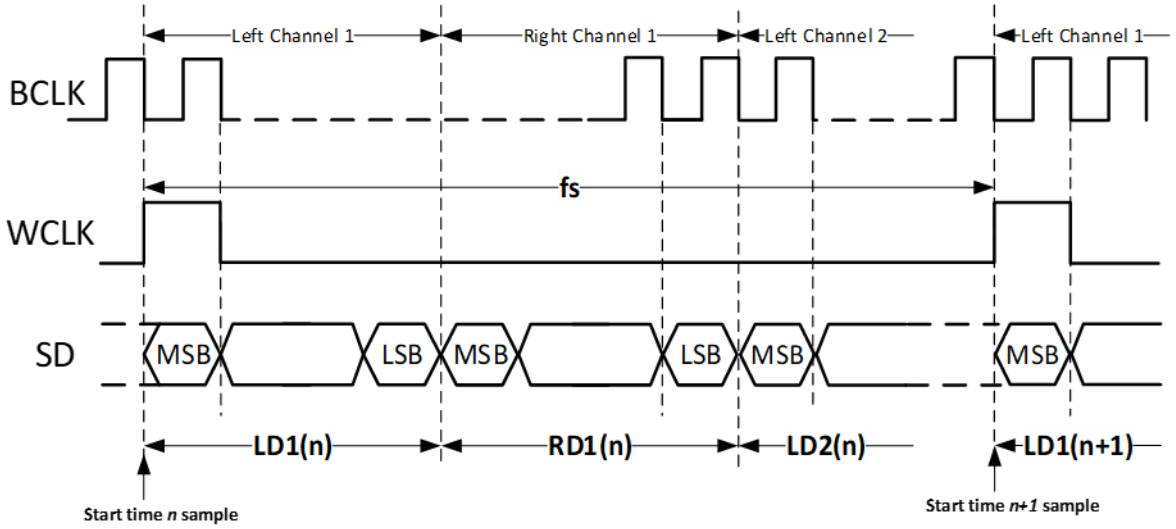
Bits	Name	Access	Description
0	MODE	R/W	TDM mode select 0x0: Slave mode 0x1: Master mode

NOTE

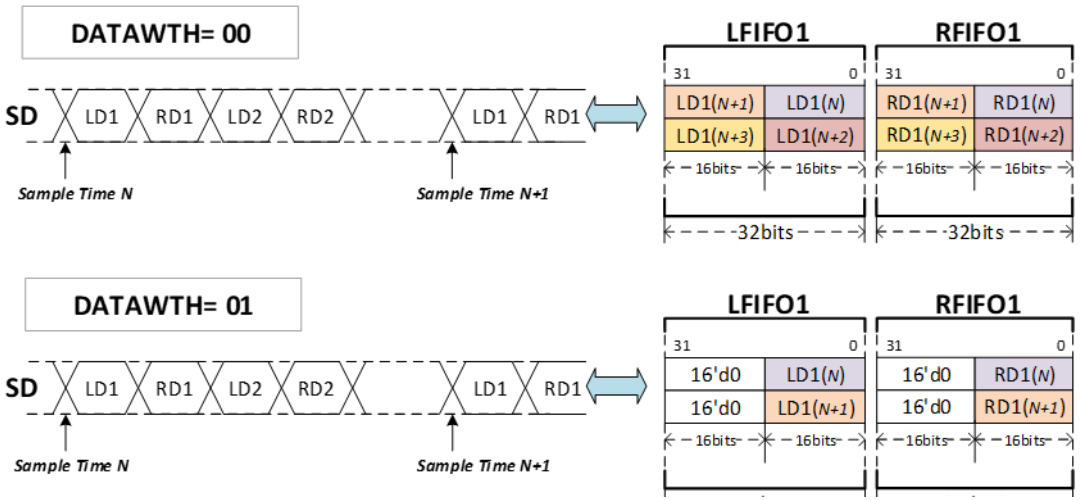
Transmit data on the rising edge:



Transmit data on the falling edge：



Data width formats：



4.3.2.3 CHOFFSET1_DR

- Name: CHOFFSET1_DR
- Address Offset: 0x08
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:13	RESERVED	RO	Reserved
12:8	OFFSET2	R/W	Offset of RD1 data (@CHORD=0) or LD1 data (@CHORD=1) relative to the first data. 0x00: offset = 0 BCLK cycle 0x01: offset = 1 BCLK cycle 0x02: offset = 2 BCLK cycles ... 0x1e: offset = 30 BCLK cycles 0x1f: offset = 31 BCLK cycles
7:5	RESERVED	RO	Reserved
4:0	OFFSET1	R/W	Offset of LD1 data (@CHORD=0) or RD1 data (@CHORD=1) relative to the rising edge of WCLK. 0x00: offset = 0 BCLK cycle 0x01: offset = 1 BCLK cycle 0x02: offset = 2 BCLK cycles ... 0x1e: offset = 30 BCLK cycles 0x1f: offset = 31 BCLK cycles

4.3.2.4 CHOFFSET2_DR

- Name: CHOFFSET2_DR
- Address Offset: 0x0C
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:13	RESERVED	RO	Reserved
12:8	OFFSET4	R/W	Offset of RD2 data (@CHORD=0) or LD2 data (@CHORD=1) relative to the three data. 0x00: offset = 0 BCLK cycle 0x01: offset = 1 BCLK cycle 0x02: offset = 2 BCLK cycles ... 0x1e: offset = 30 BCLK cycles 0x1f: offset = 31 BCLK cycles
7:5	RESERVED	RO	Reserved
4:0	OFFSET3	R/W	Offset of LD2 data (@CHORD=0) or RD2 data (@CHORD=1) relative to the second data. 0x00: offset = 0 BCLK cycle 0x01: offset = 1 BCLK cycle 0x02: offset = 2 BCLK cycles ... 0x1e: offset = 30 BCLK cycles 0x1f: offset = 31 BCLK cycles

4.3.2.5 CHOFFSET3_DR

- Name: CHOFFSET3_DR
- Address Offset: 0x10
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:13	RESERVED	RO	Reserved
12:8	OFFSET6	R/W	Offset of RD3 data (@CHORD=0) or LD3 data (@CHORD=1) relative to the fifth data. 0x00: offset = 0 BCLK cycle 0x01: offset = 1 BCLK cycle 0x02: offset = 2 BCLK cycles

Bits	Name	Access	Description
			... 0x1e: offset = 30 BCLK cycles 0x1f: offset = 31 BCLK cycles
7:5	RESERVED	RO	Reserved
4:0	OFFSET5	R/W	Offset of LD3 data (@CHORD=0) or RD3 data (@CHORD=1) relative to the fourth data. 0x00: offset = 0 BCLK cycle 0x01: offset = 1 BCLK cycle 0x02: offset = 2 BCLK cycles ... 0x1e: offset = 30 BCLK cycles 0x1f: offset = 31 BCLK cycles

4.3.2.6 CHOFFSET4_DR

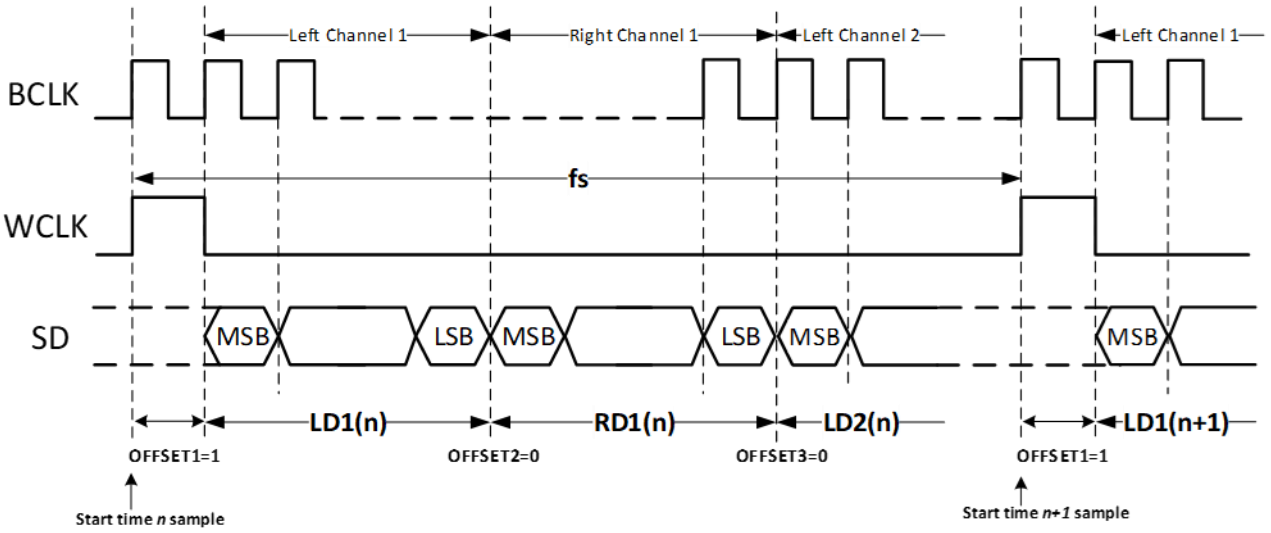
- Name: CHOFFSET4_DR
- Address Offset: 0x14
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:13	RESERVED	RO	Reserved
12:8	OFFSET8	R/W	Offset of RD4 data (@CHORD=0) or LD4 data (@CHORD=1) relative to the seventh data. 0x00: offset = 0 BCLK cycle 0x01: offset = 1 BCLK cycle 0x02: offset = 2 BCLK cycles ... 0x1e: offset = 30 BCLK cycles 0x1f: offset = 31 BCLK cycles
7:5	RESERVED	RO	Reserved
4:0	OFFSET7	R/W	Offset of LD4 data (@CHORD=0) or RD4 data (@CHORD=1) relative to the sixth data. 0x00: offset = 0 BCLK cycle 0x01: offset = 1 BCLK cycle 0x02: offset = 2 BCLK cycles ...

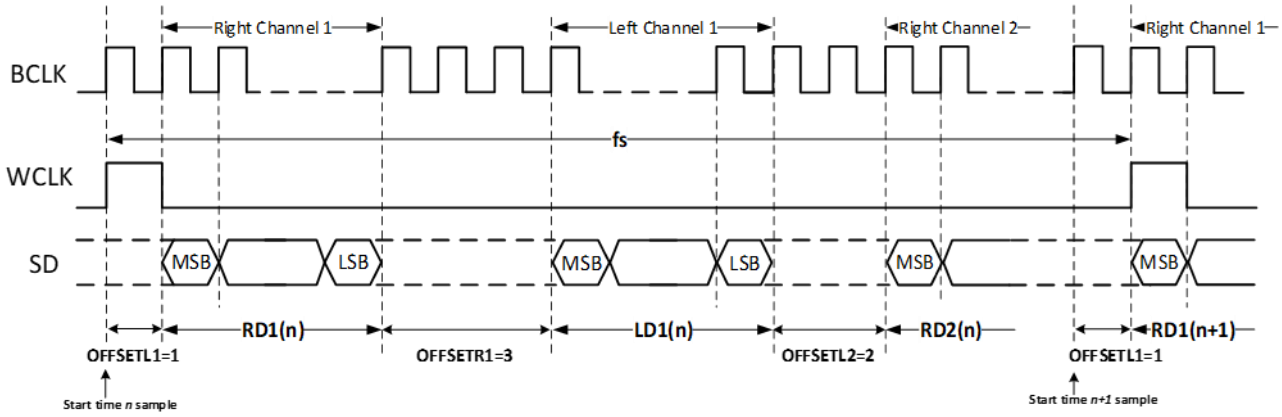
Bits	Name	Access	Description
			0x1e: offset = 30 BCLK cycles 0x1f: offset = 31 BCLK cycles

NOTE

Multiple offset timing for each channel@CHORD = 0, OFFSET1 = 1, OFFSET2 = 0, OFFSET3 = 0:



Multiple offset timing for each channel @CHORD = 1, OFFSET1 = 1, OFFSET2 = 3, OFFSET3 = 2：



4.3.2.7 FIFOTL1

- Name: FIFOTL1
- Address Offset: 0x18
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:7	RESERVED	RO	Reserved
6:4	RFT1	R/W	RFIFO1 threshold The configuration range is 1-7. When set to 0, the threshold is 8. The default value is 0.

Bits	Name	Access	Description
3	RESERVED	RO	Reserved
2:0	LFT1	R/W	LFIFO1 threshold It can be configured in the range 1-7. When set to 0, the threshold is 8. The default value is 0.

4.3.2.8 FIFOTL2

- Name: FIFOTL2
- Address Offset: 0x1C
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:7	RESERVED	RO	Reserved
6:4	RFT2	R/W	RFIFO2 threshold. It can be configured in the range 1-7. When set to 0, the threshold is 8. The default value is 0.
3	RESERVED	RO	Reserved
2:0	LFT2	R/W	LFIFO2 threshold It can be configured in the range 1-7. When set to 0, the threshold is 8. The default value is 0.

4.3.2.9 FIFOTL3

- Name: FIFOTL3
- Address Offset: 0x20
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:7	RESERVED	RO	Reserved
6:4	RFT3	R/W	RFIFO3 threshold It can be configured in the range 1-7. When set to 0, the threshold is 8. The default value is 0.
3	RESERVED	RO	Reserved
2:0	LFT3	R/W	LFIFO3 threshold It can be configured in the range 1-7. When set to 0, the threshold is 8. The default value is 0.

4.3.2.10 FIFOTL4

- Name: FIFOTL4
- Address Offset: 0x24
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:7	RESERVED	RO	Reserved
6:4	RFT4	R/W	RFIFO4 threshold It can be configured in the range 1-7. When set to 0, the threshold is 8. The default value is 0.
3	RESERVED	RO	Reserved
2:0	LFT4	R/W	LFIFO4 threshold It can be configured in the range 1-7. When set to 0, the threshold is 8. The default value is 0.

4.3.2.11 TDM_SR

- Name: TDM_SR
- Address Offset: 0x28
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:20	RESERVED	RO	Reserved
19	RFF4	RO	TDM RFIFO4 Full 0: TDM RFIFO4 is not full. 1: TDM RFIFO4 is full.
18	RFNE4	RO	TDM RFIFO4 Not Empty 0: TDM RFIFO4 is empty. 1: TDM RFIFO4 is not empty.
17	LFF4	RO	TDM LFIFO4 Full 0: TDM LFIFO4 is not full. 1: TDM LFIFO4 is full.
16	LFNE4	RO	TDM LFIFO4 Not Empty 0: TDM LFIFO4 is empty. 1: TDM LFIFO4 is not empty.
15	RFF3	RO	TDM RFIFO3 Full 0: TDM RFIFO3 is not full.

Bits	Name	Access	Description
			1: TDM RFIFO3 is full.
14	RFNE3	RO	TDM RFIFO3 Not Empty 0: TDM RFIFO3 is empty. 1: TDM RFIFO3 is not empty.
13	LFF3	RO	TDM LFIFO3 Full 0: TDM LFIFO3 is not full. 1: TDM LFIFO3 is full.
12	LFNE3	RO	TDM LFIFO3 Not Empty 0: TDM LFIFO3 is empty. 1: TDM LFIFO3 is not empty.
11	RFF2	RO	TDM RFIFO2 Full 0: TDM RFIFO2 is not full. 1: TDM RFIFO2 is full.
10	RFNE2	RO	TDM RFIFO2 Not Empty 0: TDM RFIFO2 is empty. 1: TDM RFIFO2 is not empty.
9	LFF2	RO	TDM LFIFO2 Full 0: TDM LFIFO2 is not full. 1: TDM LFIFO2 is full.
8	LFNE2	RO	TDM LFIFO2 Not Empty 0: TDM LFIFO2 is empty. 1: TDM LFIFO2 is not empty.
7	RFF1	RO	TDM RFIFO1 Full 0: TDM RFIFO1 is not full. 1: TDM RFIFO1 is full.
6	RFNE1	RO	TDM RFIFO1 Not Empty 0: TDM RFIFO1 is empty. 1: TDM RFIFO1 is not empty.
5	LFF1	RO	TDM LFIFO1 Full 0: TDM LFIFO1 is not full. 1: TDM LFIFO1 is full.
4	LFNE1	RO	TDM LFIFO1 Not Empty 0: TDM LFIFO1 is empty.

Bits	Name	Access	Description
			1: TDM LFIFO1 is not empty.
3:1	RESERVED	RO	Reserved
0	TDM_BUSY	RO	TDM Busy Flag 0x0: TDM is idle. 0x1: TDM is busy.

4.3.2.12 TDM_IMR

- Name: TDM_IMR
- Address Offset: 0x2C
- Reset Value: 0x7777_77FE

Bits	Name	Access	Description
31	RESERVED	RO	Reserved
30	RF4FIM	R/W	RFIFO4 threshold full interrupt mask 0: tdm_rf4f_intr interrupt is masked. 1: tdm_rf4f_intr interrupt is not masked.
29	RF4OEM	R/W	RFIFO4 overflow error mask 0: tdm_rf4o_err error is masked. 1: tdm_rf4o_err error is not masked.
28	RF4UEM	R/W	RFIFO4 underflow error mask. 0: tdm_rf4u_err error is masked. 1: tdm_rf4u_err error is not masked.
27	RESERVED	RO	Reserved
26	LF4FIM	R/W	LFIFO4 threshold full interrupt mask. 0: tdm_lf4f_intr interrupt is masked. 1: tdm_lf4f_intr interrupt is not masked.
25	LF4OEM	R/W	LFIFO4 overflow error mask. 0: tdm_lf4o_err error is masked. 1: tdm_lf4o_err error is not masked.
24	LF4UEM	R/W	LFIFO4 underflow error mask. 0: tdm_lf4u_err error is masked. 1: tdm_lf4u_err is not masked.
23	RESERVED	RO	Reserved

Bits	Name	Access	Description
22	RF3FIM	R/W	RFIFO3 threshold full interrupt mask 0: tdm_rf3f_intr interrupt is masked. 1: tdm_rf3f_intr interrupt is not masked.
21	RF3OEM	R/W	RFIFO3 overflow error mask 0: tdm_rf3o_err error is masked. 1: tdm_rf3o_err error is not masked.
20	RF3UEM	R/W	RFIFO3 underflow error mask 0: tdm_rf3u_err error is masked. 1: tdm_rf3u_err error is not masked.
19	RESERVED	RO	Reserved
18	LF3FIM	R/W	LFIFO3 threshold full interrupt mask 0: tdm_lf3f_intr interrupt is masked. 1: tdm_lf3f_intr interrupt is not masked.
17	LF3OEM	R/W	LFIFO3 overflow error mask 0: tdm_lf3o_err error is masked. 1: tdm_lf3o_err error is not masked.
16	LF3UEM	R/W	LFIFO3 underflow error mask 0: tdm_lf3u_err error is masked. 1: tdm_lf3u_err error is not masked.
15	RESERVED	RO	Reserved
14	RF2FIM	R/W	RFIFO2 threshold full interrupt mask 0: tdm_rf2f_intr interrupt is masked. 1: tdm_rf2f_intr interrupt is not masked.
13	RF2OEM	R/W	RFIFO2 overflow error mask 0: tdm_rf2o_err error is masked. 1: tdm_rf2o_err error is not masked.
12	RF2UEM	R/W	RFIFO2 underflow error mask 0: tdm_rf2u_err error is masked. 1: tdm_rf2u_err error is not masked.
11	RESERVED	RO	Reserved
10	LF2FIM	R/W	LFIFO2 threshold full interrupt mask 0: tdm_lf2f_intr interrupt is masked. 1: tdm_lf2f_intr interrupt is not masked.

Bits	Name	Access	Description
9	LF2OEM	R/W	LFIFO2 overflow error mask 0: tdm_lf2o_err error is masked. 1: tdm_lf2o_err error is not masked.
8	LF2UEM	R/W	LFIFO2 underflow error mask 0: tdm_lf2u_err error is masked. 1: tdm_lf2u_err error is not masked.
7	RF1FIM	R/W	RFIFO1 threshold full interrupt mask 0: tdm_rf1f_intr interrupt is masked. 1: tdm_rf1f_intr interrupt is not masked.
6	RF1OEM	R/W	RFIFO1 overflow error mask 0: tdm_rf1o_err error is masked. 1: tdm_rf1o_err error is not masked.
5	RF1UEM	R/W	RFIFO1 underflow error mask 0: tdm_rf1u_err error is masked. 1: tdm_rf1u_err error is not masked.
4	LF1FIM	R/W	LFIFO1 threshold full interrupt mask 0: tdm_lf1f_intr interrupt is masked. 1: tdm_lf1f_intr interrupt is not masked.
3	LF1OEM	R/W	LFIFO1 overflow error mask 0: tdm_lf1o_err error is masked. 1: tdm_lf1o_err error is not masked.
2	LF1UEM	R/W	LFIFO1 underflow error mask 0: tdm_lf1u_err error is masked. 1: tdm_lf1u_err error is not masked.
1	TDMWAEM	R/W	TDM access address error mask 0: tdm_waddr_err error is masked. 1: tdm_waddr_err error is not masked.
0	TDMBIM	R/W	TDM busy flag change interrupt mask 0: tdm_busy_intr interrupt is masked. 1: tdm_busy_intr interrupt is not masked.

4.3.2.13 TDM_ISR

- Name: TDM_ISR

- Address Offset: 0x30
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31	RESERVED	RO	Reserved
30	RF4FIS	RO	RFIFO4 threshold full interrupt status 0: tdm_rf4f_intr interrupt = 0 1: tdm_rf4f_intr interrupt = 1
29	RF4OES	RO	RFIFO4 overflow error status 0: tdm_rf4o_err error = 0 1: tdm_rf4o_err error = 1
28	RF4UES	RO	RFIFO4 underflow error status 0: tdm_rf4u_err error = 0 1: tdm_rf4u_err error = 1
27	RESERVED	RO	Reserved
26	LF4FIS	RO	LFIFO4 threshold full interrupt status 0: tdm_lf4f_intr interrupt = 0 1: tdm_lf4f_intr interrupt = 1
25	LF4OES	RO	LFIFO4 overflow error status 0: tdm_lf4o_err error = 0 1: tdm_lf4o_err error = 1
24	LF4UES	RO	LFIFO4 underflow error status 0: tdm_lf4u_err error = 0 1: tdm_lf4u_err error = 1
23	RESERVED	RO	Reserved
22	RF3FIS	RO	RFIFO3 threshold full interrupt status 0: tdm_rf3f_intr interrupt = 0 1: tdm_rf3f_intr interrupt = 1
21	RF3OES	RO	RFIFO3 overflow error status 0: tdm_rf3o_err error = 0 1: tdm_rf3o_err error = 1
20	RF3UES	RO	RFIFO3 underflow error status 0: tdm_rf3u_err error = 0 1: tdm_rf3u_err error = 1

Bits	Name	Access	Description
19	RESERVED	RO	Reserved
18	LF3FIS	RO	LFIFO3 threshold full interrupt status 0: tdm_lf3f_intr interrupt = 0 1: tdm_lf3f_intr interrupt = 1
17	LF3OES	RO	LFIFO3 overflow error status 0: tdm_lf3o_err error = 0 1: tdm_lf3o_err error = 1
16	LF3UES	RO	LFIFO3 underflow error status 0: tdm_lf3u_err error = 0 1: tdm_lf3u_err error = 1
15	RESERVED	RO	Reserved
14	RF2FIS	RO	RFIFO2 threshold full interrupt status 0: tdm_rf2f_intr interrupt = 0 1: tdm_rf2f_intr interrupt = 1
13	RF2OES	RO	RFIFO2 overflow error status 0: tdm_rf2o_err error = 0 1: tdm_rf2o_err error = 1
12	RF2UES	RO	RFIFO2 underflow error status 0: tdm_rf2u_err error = 0 1: tdm_rf2u_err error = 1
11	RESERVED	RO	Reserved
10	LF2FIS	RO	LFIFO2 threshold full interrupt status 0: tdm_lf2f_intr interrupt = 0 1: tdm_lf2f_intr interrupt = 1
9	LF2OES	RO	LFIFO2 overflow error status 0: tdm_lf2o_err error = 0 1: tdm_lf2o_err error = 1
8	LF2UES	RO	LFIFO2 underflow error status. 0: tdm_lf2u_err error = 0 1: tdm_lf2u_err error = 1
7	RF1FIS	RO	RFIFO1 threshold full interrupt status 0: tdm_rf1f_intr interrupt = 0 1: tdm_rf1f_intr interrupt = 1

Bits	Name	Access	Description
6	RF1OES	RO	RFIFO1 overflow error status 0: tdm_rf1o_err error = 0 1: tdm_rf1o_err error = 1
5	RF1UES	RO	RFIFO1 underflow error status 0: tdm_rf1u_err error = 0 1: tdm_rf1u_err error = 1
4	LF1FIS	RO	LFIFO1 threshold full interrupt status 0: tdm_lf1f_intr interrupt = 0 1: tdm_lf1f_intr interrupt = 1
3	LF1OES	RO	LFIFO1 overflow error status 0: tdm_lf1o_err error = 0 1: tdm_lf1o_err error = 1
2	LF1UES	RO	LFIFO1 underflow error status 0: tdm_lf1u_err error = 0 1: tdm_lf1u_err error = 1
1	TDMWAES	RO	TDM access address error status 0: tdm_waddr_err error = 0 1: tdm_waddr_err error = 1
0	TDMBIS	RO	TDM busy flag change interrupt status 0: tdm_busy_intr interrupt = 0 1: tdm_busy_intr interrupt = 1

4.3.2.14 TDM_RISR

- Name: TDM_RISR
- Address Offset: 0x34
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31	RESERVED	RO	Reserved
30	RRF4FIS	RO	RFIFO4 threshold full RAW interrupt status 0: tdm_rf4f_intr RAW interrupt = 0 1: tdm_rf4f_intr RAW interrupt = 1
29	RRF4OES	RO	RFIFO4 overflow raw error status 0: tdm_rf4o_err RAW error = 0

Bits	Name	Access	Description
			1: tdm_rf4o_err RAW error = 1
28	RRF4UES	RO	RFIFO4 underflow Raw error status 0: tdm_rf4u_err RAW error = 0 1: tdm_rf4u_err RAW error = 1
27	RESERVED	RO	Reserved
26	RLF4FIS	RO	LFIFO4 threshold full RAW interrupt status 0: tdm_lf4f_intr RAW interrupt = 0 1: tdm_lf4f_intr RAW interrupt = 1
25	RLF4OES	RO	LFIFO4 overflow RAW error status 0: tdm_lf4o_err RAW error = 0 1: tdm_lf4o_err RAW error = 1
24	RLF4UES	RO	LFIFO4 underflow RAW error status 0: tdm_lf4u_err RAW error = 0 1: tdm_lf4u_err RAW error = 1
23	RESERVED	RO	Reserved
22	RRF3FIS	RO	RFIFO3 threshold full RAW interrupt status 0: tdm_rf3f_intr RAW interrupt = 0 1: tdm_rf3f_intr RAW interrupt = 1
21	RRF3OES	RO	RFIFO3 overflow RAW error status 0: tdm_rf3o_err RAW error = 0 1: tdm_rf3o_err RAW error = 1
20	RRF3UES	RO	RFIFO3 underflow RAW error status 0: tdm_rf3u_err RAW error = 0 1: tdm_rf3u_err RAW error = 1
19	RESERVED	RO	Reserved
18	RLF3FIS	RO	LFIFO3 threshold full RAW interrupt status 0: tdm_lf3f_intr RAW interrupt = 0 1: tdm_lf3f_intr RAW interrupt = 1
17	RLF3OES	RO	LFIFO3 overflow RAW error status 0: tdm_lf3o_err RAW error = 0 1: tdm_lf3o_err RAW error = 1
16	RLF3UES	RO	LFIFO3 underflow RAW error status

Bits	Name	Access	Description
			0: tdm_lf3u_err RAW error = 0 1: tdm_lf3u_err RAW error = 1
15	RESERVED	RO	Reserved
14	RRF2FIS	RO	RFIFO2 threshold full RAW interrupt status 0: tdm_rf2f_intr RAW interrupt = 0 1: tdm_rf2f_intr RAW interrupt = 1
13	RRF2OES	RO	RFIFO2 overflow RAW error status 0: tdm_rf2o_err RAW error = 0 1: tdm_rf2o_err RAW error = 1
12	RRF2UES	RO	RFIFO2 uderflow RAW error status 0: tdm_rf2u_err RAW error = 0 1: tdm_rf2u_err RAW error = 1
11	RESERVED	RO	Reserved
10	RLF2FIS	RO	LFIFO2 threshold full RAW interrupt status 0: tdm_lf2f_intr RAW interrupt = 0 1: tdm_lf2f_intr RAW interrupt = 1
9	RLF2OES	RO	LFIFO2 overflow RAW error status 0: tdm_lf2o_err RAW error = 0 1: tdm_lf2o_err RAW error = 1
8	RLF2UES	RO	LFIFO2 underflow RAW error status 0: tdm_lf2u_err RAW error = 0 1: tdm_lf2u_err RAW error = 1
7	RRF1FIS	RO	RFIFO1 threshold full RAW interrupt status 0: tdm_rf1f_intr RAW interrupt = 0 1: tdm_rf1f_intr RAW interrupt = 1
6	RRF1OES	RO	RFIFO1 overflow RAW error status 0: tdm_rf1o_err RAW error = 0 1: tdm_rf1o_err RAW error = 1
5	RRF1UES	RO	RFIFO1 underflow RAW error status 0: tdm_rf1u_err RAW error = 0 1: tdm_rf1u_err RAW error = 1
4	RLF1FIS	RO	LFIFO1 threshold full RAW interrupt status 0: tdm_lf1f_intr RAW interrupt = 0

Bits	Name	Access	Description
			1: tdm_lf1f_intr interrupt = 1
3	RLF1OES	RO	LFIFO1 overflow RAW error status 0: tdm_lf1o_err RAW error = 0 1: tdm_lf1o_err RAW error = 1
2	RLF1UES	RO	LFIFO1 underflow RAW error status 0: tdm_lf1u_err RAW error = 0 1: tdm_lf1u_err RAW error = 1
1	RTDMWAES	RO	TDM access address RAW error status 0: tdm_waddr_err RAW error = 0 1: tdm_waddr_err RAW error = 1
0	RTDMBIS	RO	TDM busy flag change RAW interrupt status 0: tdm_busy_intr RAW interrupt = 0 1: tdm_busy_intr RAW interrupt = 1

4.3.2.15 TDM_ICR

- Name: TDM_ICR
- Address Offset: 0x38
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31	RESERVED	WO	Reserved
30	RF4FIC	WO	Write 1 clear RFIFO4 threshold full interrupt
29	RF4OEC	WO	Write 1 clear RFIFO4 overflow error
28	RF4UEC	WO	Write 1 clear RFIFO4 underflow error
27	RESERVED	WO	Reserved
26	LF4FIC	WO	Write 1 clear LFIFO4 threshold full interrupt
25	LF4OEC	WO	Write 1 clear LFIFO4 overflow error
24	LF4UEC	WO	Write 1 clear LFIFO4 underflow error
23	RESERVED	WO	Reserved
22	RF3FIC	WO	Write 1 clear RFIFO3 threshold full interrupt
21	RF3OEC	WO	Write 1 clear RFIFO3 overflow error
20	RF3UEC	WO	Write 1 clear RFIFO3 underflow error

Bits	Name	Access	Description
19	RESERVED	WO	Reserved
18	LF3FIC	WO	Write 1 clear LFIFO3 threshold full interrupt
17	LF3OEC	WO	Write 1 clear LFIFO3 overflow error
16	LF3UEC	WO	Write 1 clear LFIFO3 underflow error
15	RESERVED	WO	Reserved
14	RF2FIC	WO	Write 1 clear RFIFO2 threshold full interrupt
13	RF2OEC	WO	Write 1 clear RFIFO2 overflow error
12	RF2UEC	WO	Write 1 clear RFIFO2 underflow error
11	RESERVED	WO	Reserved
10	LF2FIC	WO	Write 1 clear LFIFO2 threshold full interrupt
9	LF2OEC	WO	Write 1 clear LFIFO2 overflow error
8	LF2UEC	WO	Write 1 clear LFIFO2 underflow error
7	RF1FIC	WO	Write 1 clear RFIFO1 threshold full interrupt
6	RF1OEC	WO	Write 1 clear RFIFO1 overflow error
5	RF1UEC	WO	Write 1 clear RFIFO1 underflow error
4	LF1FIC	WO	Write 1 clear LFIFO1 threshold full interrupt
3	LF1OEC	WO	Write 1 clear LFIFO1 overflow error
2	LF1UES	WO	Write 1 clear LFIFO1 underflow error
1	TDMWAEC	WO	Write 1 clear TDM access address error
0	TDMBIC	WO	Write 1 clear TDM busy flag change interrupt

4.3.2.16 TDM_DMAEN

- Name: TDM_DMAEN
- Address Offset: 0x3C
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:1	RESERVED	RO	Reserved
0	DMAEN	RW	TDM DMA handshake signal enable 0x0: TDM DMA handshake signal is disabled. 0x1: TDM DMA handshake signal is enabled.

4.3.2.17 TDM_DMADL

- Name: TDM_DMADL
- Address Offset: 0x40
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:3	RESERVED	RO	Reserved
2:0	DMADL	RW	PDM all FIFO DMA threshold configuration register When data in FIFO is greater than or equal to the threshold, a threshold full interrupt is generated. Configuration range 1-7. When set to 0, the threshold is 8. The default value is 0.

4.3.2.18 LDR1

- Name: LDR1
- Address Offset: 0x44
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	LDR1	RO	L FIFO 1 data read register

4.3.2.19 RDR1

- Name: RDR1
- Address Offset: 0x48
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	RDR1	RO	R FIFO 1 data read register

4.3.2.20 LDR2

- Name: LDR2
- Address Offset: 0x4C
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	LDR2	RO	L FIFO 2 data read register

4.3.2.21 RDR2

- Name: RDR2
- Address Offset: 0x50
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	RDR2	RO	R FIFO 2 data read register

4.3.2.22 LDR3

- Name: LDR3
- Address Offset: 0x54
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	LDR3	RO	L FIFO 3 data read register

4.3.2.23 RDR3

- Name: RDR3
- Address Offset: 0x58
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	RDR3	RO	R FIFO 3 data read register

4.3.2.24 LDR4

- Name: LDR4
- Address Offset: 0x5C
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	LDR4	RO	L FIFO 4 data read register

4.3.2.25 RDR4

- Name: RDR4
- Address Offset: 0x60
- Reset Value: 0x0000_0000

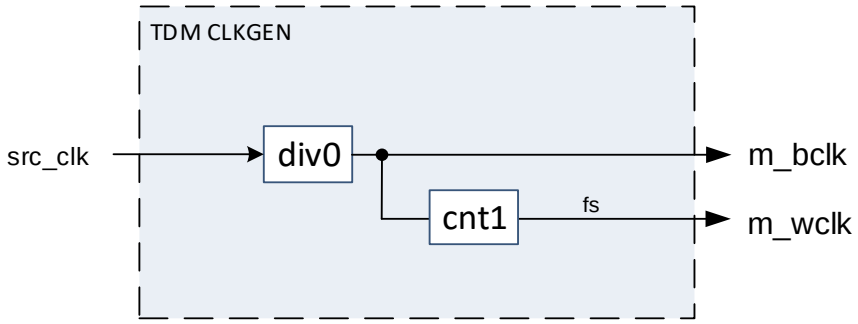
Bits	Name	Access	Description
31:0	RDR4	RO	R FIFO 4 data read register

4.3.2.26 DIV0_LEVEL

- Name: DIV0_LEVEL
- Address Offset: 0x64
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:12	RESERVED	WO	Reserved
11:0	DIV0	RW	BCLK divider configuration. If the value is 0 or 1, no frequency division.

NOTE



m_bclk = src_clk/DIV0 = Fs*(bits*channels+all_offsets)
bits = 16, 24, 32
channels = 2, 4, 6, 8
all_offsets = OFFSETL1+OFFSETL2+OFFSETL3+OFFSETL4+OFFSETR1+OFFSETR2+OFFSETR3+OFFSETR4
m_wclk = fs

5 VAD

5.1 Features

- The operating frequency of mclk is 2.56MHz.
- APB bus, pclk: greater than 15MHz.
- Reset: preset_n, mrst_n, active low.
- PDM2PCM interface:
  - Supports 2-wire PDM master receive function: pdm_clk/sdin.
  - The operating frequency of mclk is 2.56MHz.
  - Supports mono and dual channels.
  - Standard mode and low power mode
  - pdm_clk output is 640kHz (low power mode) or 1.28MHz (standard mode).
  - Configurable CIC filter
  - CIC downsampling multiple: 10x or 20x
  - HBF, LPF, and IIR with fixed coefficients
  - The output audio is 16kHz 16-bit PCM audio data. The gain can be configured.
  - Auto enter standard mode after low power wakeup
- VAD:
  - PCM data, 16kHz sampling, 16bit/32bit (mono/dual)
  - A ping-pong cache (32x320 SRAM), to ensure that the memory compiler can generate a moderately sized SRAM.
  - Three-port SRAM arbitration, DMA path, PCM path, and VAD path, PCM path has the highest priority. When PCM accesses SRAM, other paths need to wait.
  - Low pass filter (4kHz)
  - VAD algorithm
    - Short time energy (STE) with double thresholds
    - Zero crossing rate (ZCR) with double thresholds
  - Interrupt
    - Vad_trigger: STE and ZCR, three frames up two frames, vad trigger is pulled up.
    - Fifo_intr: FIFO related interrupts and data_overflow_err
- DMA handshake signal (req&ack): When data stored in FIFO reaches the threshold, dma_req will be pulled up.
- Two FIFOs store left/right channel data separately, 32-bit width and 8-bit depth:
  - With WAIT_BUS function: When vad_trig is pulled up and bus_ready signal is written to 1, data in SRAM will be stored in FIFO. (Need to add define WAIT_BUS)
  - Without WAIT_BUS function: When vad_trig is pulled up, data in SRAM will be automatically stored in FIFO.
- I2S interface:

- Supports 3-wire I2S receive function.
- Supports mono and dual channels.
- Only slave mode is supported.
- Supports I2S, left-adjusted, right-adjusted, PCM format.
- Supports 16, 24, 32, and 8-bit audio data receive, converts to 16-bit data output.

5.2 Register

5.2.1 Register Memory Map

Figure & Table 5-1 Memory map of VAD registers

Register	Offset	Reset Value	Description	Section/Page
VAD_CTRL	0x00	0x0000_0000	VAD control register	5.2.2.1/99
ZCR_TH_CTRL	0x04	0x0000_461E	ZCR threshold control register	5.2.2.2/100
STE_HTH_CTRL	0x08	0x0000_4844	STE high threshold control register	5.2.2.3/100
STE_LTH_CTRL	0x0C	0x0000_036B	STE low threshold control register	5.2.2.4/100
VAD_INTR_CLR	0x10	0x0000_0000	VAD interrupt clear register	5.2.2.5/101
VAD_INTR_FLAG	0x14	0x0000_0000	VAD interrupt flag	5.2.2.6/101
VAD_INTR_MASK	0x18	0x0000_0001	VAD interrupt mask register	5.2.2.7/101
DAI_EN_REG	0x1C	0x0000_0000	DAI enable register	5.2.2.8/102
DAI_CTL_REG	0x20	0x0440_0000	DAI control register	5.2.2.9/102
FIFO_CNT	0x24	0x0000_0000	FIFO count register	5.2.2.10/104
FIFO_TH_CTRL	0x28	0x0000_0007	FIFO threshold control register	5.2.2.11/105
RESERVED	0x2C	-	-	
FIFO_INTR_CLR	0x30	0x0000_0000	FIFO interrupt clear register	5.2.2.12/105
FIFO_INTR_FLAG	0x34	0x0000_0008	FIFO interrupt flag register	5.2.2.13/105
FIFO_INTR_MASK	0x38	0x0000_0007	FIFO interrupt mask register	5.2.2.14/106
CIC_L_ST_OFFSET	0x3c	0x00184868	Left channel CIC filter standard mode offset	5.2.2.15/107
CIC_L_LP_OFFSET	0x40	0x0000c256	Left channel CIC filter low power mode offset	5.2.2.16/108
CIC_R_ST_OFFSET	0x44	0x00184868	Right channel CIC filter standard mode offset	5.2.2.17/108
CIC_R_LP_OFFSET	0x48	0x0000c256	Right channel CIC filter low power	5.2.2.18/109

Register	Offset	Reset Value	Description	Section/Page
			mode offset	
FIFO_L_READ	0x4C	0x00000000	Left channel data FIFO read	5.2.2.19/109
FIFO_R_READ	0x50	0x00000000	Right channel data FIFO read	5.2.2.20/109

5.2.2 Register and Field Description

5.2.2.1 VAD_CTRL_REG

- Name: VAD_CTRL_REG
- Address Offset: 0x00
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:3	RESERVED	RO	Reserved
2	bus_ready	R/W	Bus Ready signal 0: Bus is not ready. 1: Bus is ready. This bit needs to be configured to 1 and data_trans_en = 1, to start automatically transferring SRAM data to FIFO. Note: (1) This function is optional and needs to add define WAIT_BUS. (2) In the absence of this function, this bit is reserved, READONLY, the default value is 0. After data_trans_en = 1, FIFO will start to automatically transfer data in a very short time. The first FIFO full interrupt will be issued about 14-15us later.
1	data_trans_en	R/W	Audio data transfer enable 0: Audio data transfer is disabled. 1: Audio data transfer is enabled. When vad_trig_raw is pulled up, this bit will automatically become 1 and FIFO will store SRAM data into FIFO (in WAIT_BUS mode, it needs to wait for bus_ready = 1 at the same time). When software writes this bit as 0, FIFO will stop reading, read and write pointers in FIFO will be cleared to 0.
0	vad_en	R/W	VAD enable 0: VAD is disabled.

Bits	Name	Access	Description
			1: VAD is enabled. When raw_vad_trig is pulled up, vad_en will become 0.

5.2.2.2 ZCR_TH_CTRL_REG

- Name: ZCR_TH_CTRL_REG
- Address Offset: 0x04
- Reset Value: 0x0000_461E

Bits	Name	Access	Description
31:16	RESERVED	RO	Reserved
15:8	zcr_hth	R/W	ZCR high threshold control
7:0	zcr_lth	R/W	ZCR low threshold control

NOTE

- When ZCR > zcr_hth and ste_lth < STE < ste_hth of a frame of data, the condition for ZCR to trigger VAD_trigger is met.
- When ZCR < zcr_lth and STE > ste_hth of a frame of data, the condition for STE to trigger VAD_trigger is met.

5.2.2.3 STE_HTH_CTRL_REG

- Name: STE_HTH_CTRL_REG
- Address Offset: 0x08
- Reset Value: 0x0000_4844

Bits	Name	Access	Description
31:16	Reserved	RO	Reserved
15:0	ste_hth	RW	STE high threshold control Can be configured at will, three gears are recommended. The smaller the value, the stronger the detection capability, a smaller sound can be used to wake up. 2580: Strong detection capability, can detect small sound. 4844: Medium detection capability, suitable for normal scenarios. 86C4: The detection capability is weak and requires a relatively loud sound to wake up.

5.2.2.4 STE_LTH_CTRL_REG

- Name: STE_LTH_CTRL_REG

- Address Offset: 0x0C
- Reset Value: 0x0000_036B

Bits	Name	Access	Description
31:16	Reserved	RO	Reserved
15:0	ste_lth	RW	STE low threshold control

5.2.2.5 VAD_INTR_CLR_REG

- Name: VAD_INTR_CLR_REG
- Address Offset: 0x10
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:1	Reserved	RO	Reserved
0	vad_clr	RW	A clock cycle signal, clear vad_trig

5.2.2.6 VAD_INTR_FLAG_REG

- Name: VAD_INTR_FLAG_REG
- Address Offset: 0x14
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:1	Reserved	RO	Reserved
0	vad_intr_flag	RO	0: vad_trig_raw is not pulled up. 1: vad_trig_raw is pulled up. This bit has nothing to do with vad_intr_unmask signal.

5.2.2.7 VAD_INTR_MASK_REG

- Name: VAD_INTR_MASK_REG
- Address Offset: 0x18
- Reset Value: 0x0000_0001

Bits	Name	Access	Description
31:1	Reserved	RO	Reserved
0	vad_intr_unmask	RW	0: VAD interrupt is masked. 1: VAD interrupt is not masked.

5.2.2.8 DAI_EN_REG

- Name: DAI_EN_REG
- Address Offset: 0x1C
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:1	Reserved	RO	Reserved
0	dai_en	RW	DAI enable 0: DAI is disabled. (default) 1: DAI is enabled.

5.2.2.9 DAI_CTRL_REG

- Name: DAI_CTRL_REG
- Address Offset: 0x20
- Reset Value: 0x0440_0000

Bits	Name	Access	Description
31:27	Reserved	RO	Reserved
26:24	st_gain	RW	pdm2pcm standard mode gain control 3'd0: 0dB 3'd1: 6dB 3'd2: 12dB 3'd3: 18dB 3'd4: 24dB 3'd5: 30dB 3'd6: 36dB 3'd7: 42dB
23	Reserved	RO	Reserved
22:20	lp_gain	RW	pdm2pcm low power mode gain control 3'd0: 0dB 3'd1: 6dB 3'd2: 12dB 3'd3: 18dB 3'd4: 24dB 3'd5: 30dB 3'd6: 36dB

Bits	Name	Access	Description
			3'd7: 42dB
19:17	Reserved	RO	Reserved
16	pdm_mode	RW	PDM2PCM mode 0: Low power mode (DIV0 4 frequency division, CIC decimation 10x) 1: Standard mode (DIV0 2 frequency division, CIC decimation 20x) When Vad_trig_raw=1, pdm_mode will be automatically switched to 1.
15:14	i2s_wdsel	RW	I2S input data width select 2'b00: 16bits 2'b01: 24bits 2'b10: 32bits 2'b11: 8bits
13:12	i2s_modesel	RW	I2S mode select 2'b00: i2s 2'b01: Right-adjusted 2'b10: Left-adjusted 2'b11: PCM
11:9	Reserved	RO	Reserved
8	ch_sel	RW	Mono channel select 0: Left channel. PDM mode selects pdm_clk high-level data, I2S mode selects ws low-level data. STE&ZCR modules will detect based on left channel data. 1: Right channel. PDM mode select pdm_clk low-level data, I2S mode selects ws high-level data. STE&ZCR modules will detect based on right channel data.
7:5	Reserved	RO	Reserved
4	mono_en	RW	Mono mode enable. When this bit is 0, it is dual channel mode.
3:1	Reserved	RO	Reserved
0	funcmode	RW	Function mode select 0: PDM interface (default) 1: I2S interface

The intput data supports 8/16/24/32 bits, and the output data is unified to 16 bits, data is intercepted and filled with 0, as shown in Figure & Table 5-2:

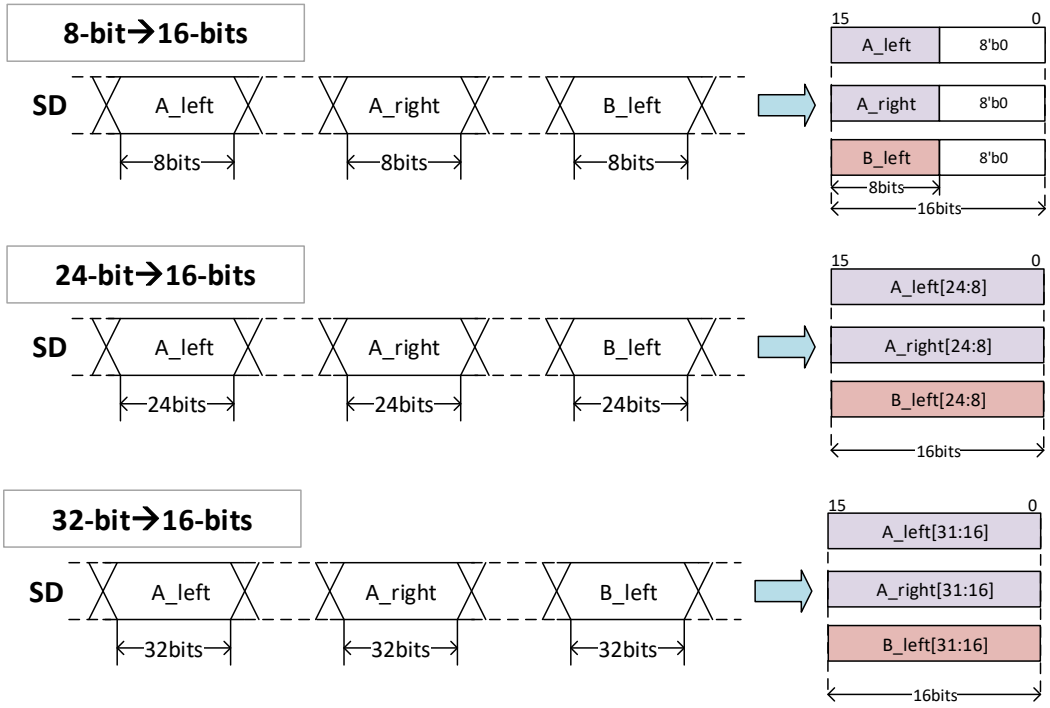


Figure & Table 5-2 I2S data interception

5.2.2.10 FIFO_CNT_REG

- Name: FIFO_CNT_REG
- Address Offset: 0x24
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:8	Reserved	RO	Reserved
7:4	fifo_l_cnt	RO	Left channel FIFO count status register, indicating how many numbers are in FIFO. 0: 0 1: 1 ... 7: 7 8: 8
3:0	fifo_r_cnt	RO	Right channel FIFO count status register, indicating how many numbers are in FIFO. 0: 0 1: 1 ...

Bits	Name	Access	Description
			7: 7 8: 8

5.2.2.11 FIFO_TH_CTRL_REG

- Name: FIFO_TH_CTRL_REG
- Address Offset: 0x28
- Reset Value: 0x0000_0007

Bits	Name	Access	Description
31:3	Reserved	RO	Reserved
2:0	fifo_th	RW	FIFO DMA handshake request threshold control 0: 1 1: 2 ... 7: 8

5.2.2.12 FIFO_INTR_REG

- Name: FIFO_INTR_REG
- Address Offset: 0x30
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:8	Reserved	RO	Reserved
7	fifo_l_empty_clr	RW	One clock cycle signal, clear fifo_l_empty
6	fifo_l_full_clr	RW	One clock cycle signal, clear fifo_l_full
5	Reserved	RO	Reserved
4	fifo_l_empty_err_clr	RW	One clock cycle signal, clear fifo_l empty_err
3	fifo_r_empty_clr	RW	One clock cycle signal, clear fifo_r_empty
2	fifo_r_full_clr	RW	One clock cycle signal, clear fifo_r_full
1	data_overflow_err_clr	RW	One clock cycle signal, clear data_overflow_err
0	fifo_r_empty_err_clr	RW	One clock cycle signal, clear fifo_r_empty_err

5.2.2.13 FIFO_INTR_FLAG_REG

- Name: FIFO_INTR_FLAG_REG

- Address Offset: 0x34
- Reset Value: 0x0000_0008

Bits	Name	Access	Description
31:8	Reserved	RO	Reserved
7	fifo_l_empty	RO	Left channel FIFO empty raw signal, write FIFO_CLR[3] = 1 to clear.
6	fifo_l_full	RO	Left channel FIFO full raw signal, write FIFO_CLR[2] = 1 to clear.
5	Reserved	RO	Reserved
4	fifo_l_empty_err	RO	Left channel FIFO empty read error raw signal, write FIFO_CLR[0] = 1 to clear.
3	fifo_r_empty	RO	Right channel FIFO empty raw signal, write FIFO_CLR[3] = 1 to clear.
2	fifo_r_full	RO	Right channel FIFO full raw signal, write FIFO_CLR[2] = 1 to clear.
1	data_overflow_err	RO	Data overflow error raw signal, write FIFO_CLR[1] = 1 to clear.
0	fifo_r_empty_err	RO	FIFO empty read error raw signal, write FIFO_CLR[0] = 1 to clear.

5.2.2.14 FIFO_INTR_MASK_REG

- Name: FIFO_INTR_MASK_REG
- Address Offset: 0x38
- Reset Value: 0x0000_0007

Bits	Name	Access	Description
31:8	Reserved	RO	Reserved
7	fifo_l_empty_unmask	RW	1: Interrupt is not masked. 0: Interrupt is masked.
6	fifo_l_full_unmask	RW	1: Interrupt is not masked. 0: Interrupt is masked.
5	Reserved	RO	Reserved
4	fifo_l_empty_err_unmask	RW	1: Interrupt is not masked. 0: Interrupt is masked.
3	fifo_r_empty_unmask	RW	1: Interrupt is not masked.

Bits	Name	Access	Description
			0: Interrupt is masked.
2	fifo_r_full_unmask	RW	1: Interrupt is not masked. 0: Interrupt is masked.
1	data_overflow_err_unmask	RW	1: Interrupt is not masked. 0: Interrupt is masked.
0	fifo_r_empty_err_unmask	RW	1: Interrupt is not masked. 0: Interrupt is masked.

5.2.2.15 CIC_L_ST_OFFSET_REG

- Name: CIC_L_ST_OFFSET_REG
- Address Offset: 0x3C
- Reset Value: 0x0018_4868

Bits	Name	Access	Description
31:23	Reserved	RO	Reserved
22:0	l_st_offset	RW	Standard mode offset of left channel CIC filter. The default value is recommended. When the DC bias of DMIC is too large, the signal needs to be calibrated according to the characteristics of DMIC.

Offset adjustment reference:
The filtered PCM data with 16k sample rate should be close to 0 in quiet conditions.
The PCM data after sinusoidal signal filtering should be 0 at the center point.
As shown in Figure & Table 5-3, the central axis of the correct audio waveform is 0. When the waveform reaches 1, PCM data corresponds to 0x7FFF. When the waveform reaches -1, PCM data corresponds to 0x8000:

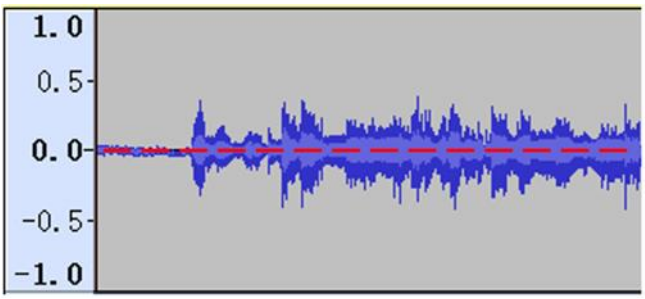


Figure & Table 5-3 Correct PCM data

If all PCM data is 0x7FFF, the offset needs to be appropriately increased. As shown in Figure & Table 5-4, the central axis of the audio waveform is greater than 0 (see the red dotted line in the figure), and the offset needs to be appropriately increased.

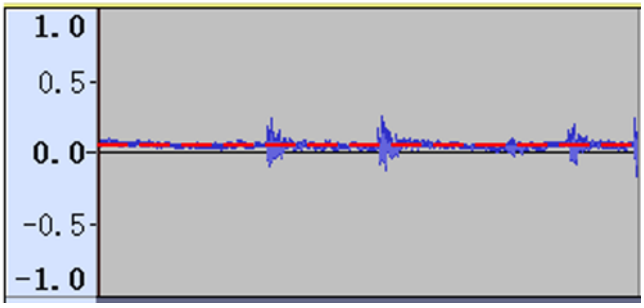


Figure & Table 5-4 PCM data with offset greater than 0

If all PCM data is 0x8000, the offset needs to be appropriately reduced. As shown in Figure & Table 5-5, the central axis of the audio waveform is less than 0 (see the red dotted line in the figure), the offset needs to be appropriately reduced.

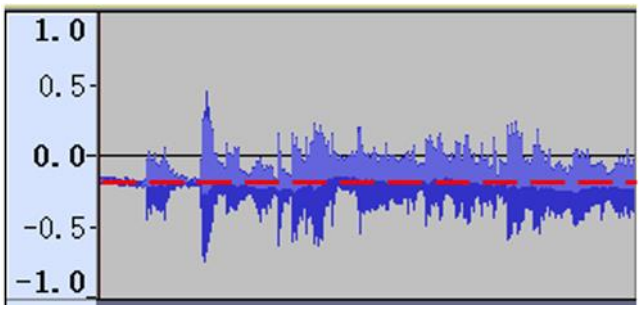


Figure & Table 5-5 PCM data with offset less than 0

5.2.2.16 CIC_L_LP_OFFSET_REG

- Name: CIC_L_LP_OFFSET_REG
- Address Offset: 0x40
- Reset Value: 0x0000_C256

Bits	Name	Access	Description
31:16	Reserved	RO	Reserved
15:0	l_lp_offset	RW	Low power mode offset of left channel CIC filter. The default value is recommended. When the DC bias of DMIC is too large, the signal needs to be calibrated according to the characteristics of DMIC.

5.2.2.17 CIC_R_ST_OFFSET_REG

- Name: CIC_R_ST_OFFSET_REG
- Address Offset: 0x44
- Reset Value: 0x0018_4868

Bits	Name	Access	Description
31:23	Reserved	RO	Reserved
22:0	r_st_offset	RW	Standard mode offset of right channel CIC filter. The

Bits	Name	Access	Description
			default value is recommended. When the DC bias of DMIC is too large, the signal needs to be calibrated according to the characteristics of DMIC.

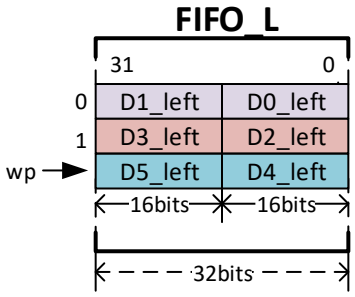
5.2.2.18 CIC_R_LP_OFFSET_REG

- Name: CIC_R_LP_OFFSET_REG
- Address Offset: 0x48
- Reset Value: 0x0000_C256

Bits	Name	Access	Description
31:16	Reserved	RO	Reserved
15:0	r_lp_offset	RW	Low power mode offset of right channel CIC filter. The default value is recommended. When the DC bias of DMIC is too large, the signal needs to be calibrated according to the characteristics of DMIC.

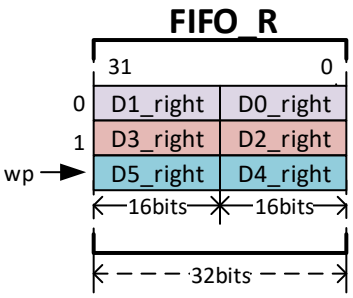
5.2.2.19 FIFO_L_READ

- Name: FIFO_L_READ
- Address Offset: 0x4C
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	fifo_read	RO	FIFO read left channel data register. Used to get left channel data in VAD. Two 16-bit data are spliced and stored in FIFO. 

5.2.2.20 FIFO_R_READ

- Name: FIFO_R_READ
- Address Offset: 0x50
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	fifo_read	RO	FIFO read right channel data register. Used to get right channel data in VAD. Two 16-bit data are spliced and stored in FIFO. 

6 SPDIF

6.1 Features

- Supports IEC-60958 protocol SPDIF-OUT and SPDIF-IN.
- Supports duplex.
- Supports 32kHz/44.1kHz/48kHz/88.2kHz/96kHz/192kHz sampling rate.
- SPDIF-OUT supports 16/20/24-bit width data, mono/dual channel, even parity, 192-bit user information data, 32-bit channel status data.
- SPDIF-IN supports valid bit, Preamble bit check, even parity, 192-bit user information data, 32-bit channel status data and discontinuous transfer.
- Two 32-bit FIFOs with a depth of 16. The threshold is configurable.
- DMA handshake signal
- ISPDIF module control register and register memory map

6.2 Operating Mode

1. System configuration:
   a) Configure PLL_frac frequency, the default is 49.152MHz.
   b) Configure PIN MUX.
   c) Open SPDIF CG.
2. Configure SPDIF_EN_REG.
3. Configure TX registers: TX_CTL_REG, TX_CS_*_REG, TX_USER_*_REG.
   Configure RX register: RX_CTL_REG.
4. Configure FIFO registers: TX_FIFO_TH, RX_FIFO_TH.
5. Configure interrupt registers: SPDIF_IMR, SPDIF_ICR.
6. Configure DMA handshake signal registers: TX_DMA_EN, TX_DMA_TH, RX_DMA_EN, RX_DMA_TH.
7. Enable SPDIF, configure TX_EN_REG and RX_EN_REG to 0x1, and start operating.

6.3 Register

6.3.1 Register Memory Map

Figure & Table 6-1 Memory map of TDM registers

Register	Offset	Reset Value	Description	Section/Page
SPDIF_EN_REG	0x00	0x00000000	SPDIF enable register	6.3.2.1/114
TX_EN_REG	0x04	0x00000000	SPDIF_OUT enable register	6.3.2.2/114
TX_CTL_REG	0x08	0x00000000	SPDIF_OUT control register	6.3.2.3/115

Register	Offset	Reset Value	Description	Section/Page
TX_CS_A_REG	0x0C	0x01000000	SPDIF_OUT channel A channel status register	6.3.2.4/116
TX_USER_A0_REG	0x10	0x00000000	SPDIF_OUT channel A user data bit [31:0]	6.3.2.5/117
TX_USER_A1_REG	0x14	0x00000000	SPDIF_OUT channel A user data bit [63:32]	6.3.2.6/117
TX_USER_A2_REG	0x18	0x00000000	SPDIF_OUT channel A user data bit [95:64]	6.3.2.7/118
TX_USER_A3_REG	0x1C	0x00000000	SPDIF_OUT channel A user data bit [127:96]	6.3.2.8/118
TX_USER_A4_REG	0x20	0x00000000	SPDIF_OUT channel A user data bit [159:128]	6.3.2.9/118
TX_USER_A5_REG	0x24	0x00000000	SPDIF_OUT channel A user data bit [191:160]	6.3.2.10/118
TX_FIFO_DR	0x28	0x00000000	SPDIF_OUT FIFO write data register	6.3.2.11/118
TX_FIFO_TH	0x2C	0x00000008	SPDIF_OUT FIFO threshold configuration register	6.3.2.12/119
TX_FIFO_DL	0x30	0x00000000	SPDIF_OUT FIFO data level register	6.3.2.13/119
TX_DMA_EN	0x34	0x00000000	SPDIF_OUT DMA handshake signal enable register	6.3.2.14/119
TX_DMA_TH	0x38	0x00000008	SPDIF_OUT DMA handshake signal threshold configuration register	6.3.2.15/119
SPDIF_SR	0x3C	0x00000006	SPDIF status register	6.3.2.16/120
SPDIF_IMR	0x40	0x00003770	SPDIF interrupt & error mask register	6.3.2.17/121
SPDIF_ISR	0x44	0x00000000	SPDIF interrupt & error status register	6.3.2.18/122
SPDIF_RISR	0x48	0x00000000	SPDIF raw interrupt & error status register	6.3.2.19/123
SPDIF_ICR	0x4C	0x00000000	SPDIF clear interrupt & error register	6.3.2.20/125
RX_EN_REG	0x50	0x00000000	SPDIF_IN enable register	6.3.2.21/125
RX_CTL_REG	0x54	0x00000000	SPDIF_IN control register	6.3.2.22/126
RX_CS_A_REG	0x58	0x00000000	SPDIF_IN channel A channel status register	6.3.2.23/126
RX_USER_A0_REG	0x5C	0x00000000	SPDIF_IN channel A user data bit	6.3.2.24/127

Register	Offset	Reset Value	Description	Section/Page
			[31:0]	
RX_USER_A1_REG	0x60	0x00000000	SPDIF_IN channel A user data bit [63:32]	6.3.2.25/127
RX_USER_A2_REG	0x64	0x00000000	SPDIF_IN channel A user data bit [95:64]	6.3.2.26/127
RX_USER_A3_REG	0x68	0x00000000	SPDIF_IN channel A user data bit [127:96]	6.3.2.27/127
RX_USER_A4_REG	0x6C	0x00000000	SPDIF_IN channel A user data bit [159:128]	6.3.2.28/127
RX_USER_A5_REG	0x70	0x00000000	SPDIF_IN channel A user data bit [191:160]	6.3.2.29/128
RX_FIFO_DR	0x74	0x00000000	SPDIF_IN FIFO data read register	6.3.2.30/128
RX_FIFO_TH	0x78	0x00000008	SPDIF_IN FIFO threshold configuration register	6.3.2.31/128
RX_FIFO_DL	0x7C	0x00000000	SPDIF_IN FIFO data level register	6.3.2.32/128
RX_DMA_EN	0x80	0x00000000	SPDIF_IN DMA handshake signal enable register	6.3.2.33/129
RX_DMA_TH	0x84	0x00000000	SPDIF_IN DMA handshake signal FIFO threshold register	6.3.2.34/129
TX_CS_B_REG	0x88	0x01000000	SPDIF_OUT channel B channel status register	6.3.2.35/129
TX_USER_B0_REG	0x8C	0x00000000	SPDIF_OUT channel B user data bit [31:0]	6.3.2.36/130
TX_USER_B1_REG	0x90	0x00000000	SPDIF_OUT channel B user data bit [63:32]	6.3.2.37/130
TX_USER_B2_REG	0x94	0x00000000	SPDIF_OUT channel B user data bit [95:64]	6.3.2.38/131
TX_USER_B3_REG	0x98	0x00000000	SPDIF_OUT channel B user data bit [127:96]	6.3.2.39/131
TX_USER_B4_REG	0x9C	0x00000000	SPDIF_OUT channel B user data bit [159:128]	6.3.2.40/131
TX_USER_B5_REG	0xa0	0x00000000	SPDIF_OUT channel B user data bit [191:160]	6.3.2.41/131
RX_CS_B_REG	0xa4	0x00000000	SPDIF_IN channel B channel status register	6.3.2.42/132

Register	Offset	Reset Value	Description	Section/Page
RX_USER_B0_REG	0xa8	0x00000000	SPDIF_IN channel B user data bit [31:0]	6.3.2.43/132
RX_USER_B1_REG	0xaC	0x00000000	SPDIF_IN channel B user data bit [63:32]	6.3.2.44/132
RX_USER_B2_REG	0xb0	0x00000000	SPDIF_IN channel B user data bit [95:64]	6.3.2.45/132
RX_USER_B3_REG	0xb4	0x00000000	SPDIF_IN channel B user data bit [127:96]	6.3.2.46/132
RX_USER_B4_REG	0xb8	0x00000000	SPDIF_IN channel B user data bit [159:128]	6.3.2.47/133
RX_USER_B5_REG	0xbC	0x00000000	SPDIF_IN channel B user data bit [191:160]	6.3.2.48/133

6.3.2 Register and Field Description

6.3.2.1 SPDIF_EN_REG

- Name: SPDIF_EN_REG
- Address Offset: 0x00
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:1	RESERVED	RO	Reserved
0	SPDIFEN	WO	SPDIF enable 0x0: SPDIF is disabled. 0x1: SPDIF is enabled.

6.3.2.2 TX_EN_REG

- Name: TX_EN_REG
- Address Offset: 0x04
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:1	RESERVED	RO	Reserved
0	TXEN	WO	SPDIF-OUT enable 0x0: SPDIF-OUT is disabled. 0x1: SPDIF-OUT is enabled.

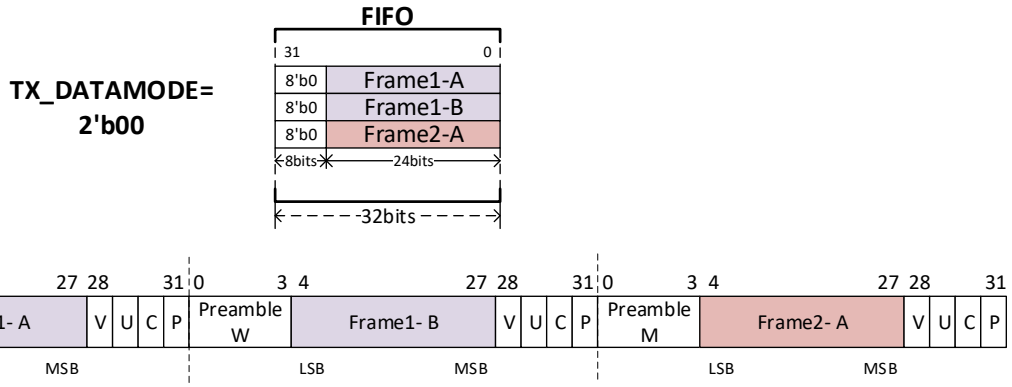
6.3.2.3 TX_CTL_REG

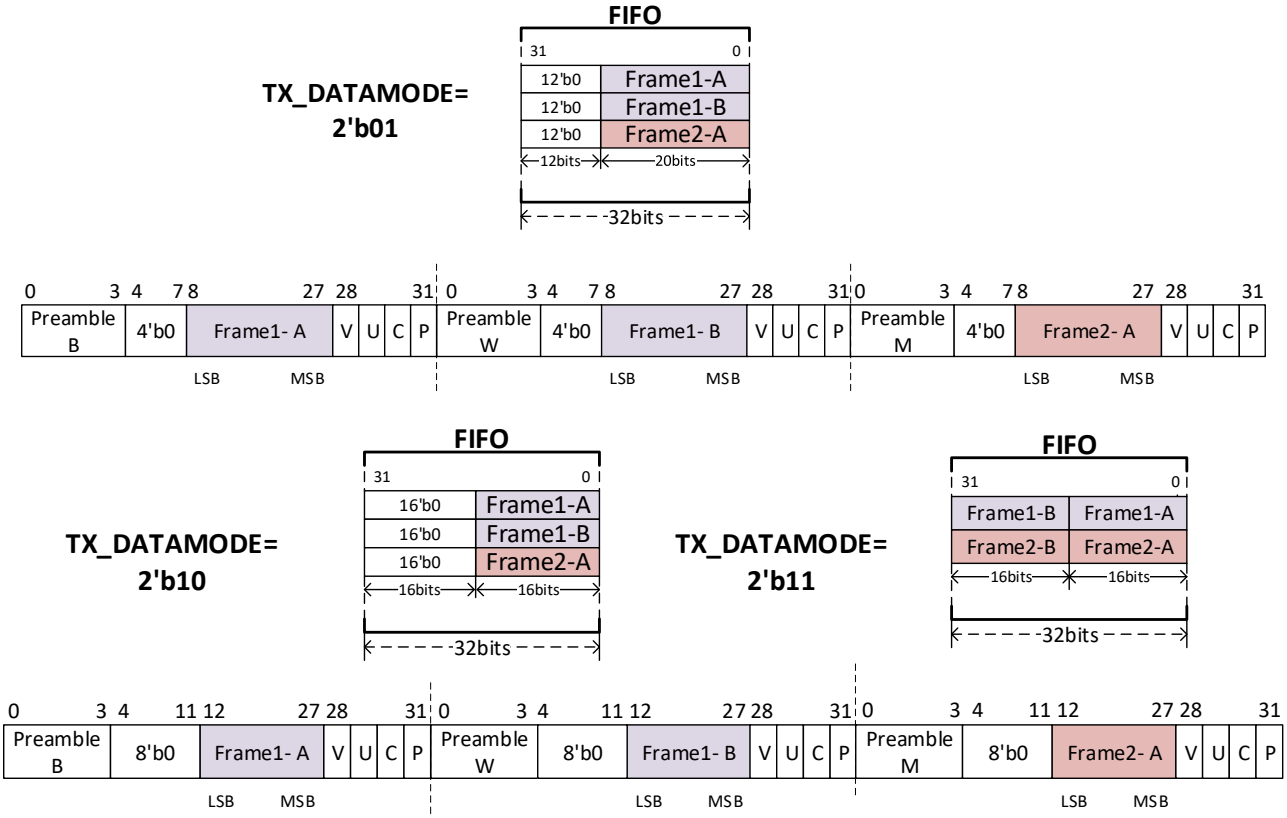
- Name: TX_CTL_REG
- Address Offset: 0x08
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:16	Reserved	RO	Reserved
15:9	TX_DIV	R/W	SPDIF-OUT divider configuration. Divide spdif_source_clk to generate spdif_tx_clk. Divider value = (TX_DIV + 1)*2
8	TX_DIV_BYPASS	R/W	SPDIF-OUT divider bypass 0x0: Bypass 0x1: Divider used
7:5	Reserved	RO	Reserved
4	TX_CH_SEL	R/W	SPDIF-OUT channel select 0x0: Dual channel, valid bit = 0 0x1: Mono, valid bit = 1 of the second sub-frame
3:2	Reserved	RO	Reserved
1:0	TX_DATAMODE	R/W	SPDIF-OUT data width select 0x0: 24-bit 0x1: 20-bit 0x2: 16-bit 0x3: Two 16-bits data spliced

NOTE

Data width formats:





6.3.2.4 TX_CS_A_REG

- Name: TX_CS_A_REG
- Address Offset: 0x0C
- Reset Value: 0x0100_0000

Bits	Name	Access	Description
31:30	RESERVED	RO	Reserved
29:28	T_CLK_ACC	RW	SPDIF-OUT clock accuracy, refer to IEC60958.
27:24	T_FS_SEL	RW	SPDIF-OUT sampling rate 0011: 32kHz 0000: 44.1kHz 0010: 48kHz 1000: 88.2kHz 1010: 96kHz 1110: 192kHz 0001: Not indicated (default) Other: Reserved
23:20	T_CH_NUM	RW	Number of SPDIF-OUT channels, refer to IEC60958.

Bits	Name	Access	Description
19:16	T_SRC_NUM	RW	Number of SPDIF-OUT sources, refer to IEC60958.
15:8	T_CC_SEL	RW	SPDIF-OUT type code, refer to IEC60958.
7:6	T_MODE	RW	SPDIF-OUT mode, refer to IEC60958.
5:4	RESERVED	RO	Reserved
3	T_EMP_MODE	RW	SPDIF-OUT emphasis mode 0: Not pre-emphasis 1: Pre-emphasis
2	T_COPY	RW	SPDIF-OUT copyright 0: Prohibited 1: Copyright licensed.
1	T_AUIDO_EN	RW	SPDIF-OUT signal type 0: Not audio 1: Audio
0	T_PRO_EN	RW	SPDIF-OUT signal format 0: Consumer 1: Professional

6.3.2.5 TX_USER_A0_REG

- Name: TX_USER_A0_REG
- Address Offset: 0x10
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	T_USER_A0_DATA	RW	SPDIF_OUT channel A user data bit [31:0]

6.3.2.6 TX_USER_A1_REG

- Name: TX_USER_A1_REG
- Address Offset: 0x14
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	T_USER_A1_DATA	RW	SPDIF_OUT channel A user data bit [63:32]

6.3.2.7 TX_USER_A2_REG

- Name: TX_USER_A2_REG
- Address Offset: 0x18
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	T_USER_A2_DATA	RW	SPDIF_OUT channel A user data bit [95:64]

6.3.2.8 TX_USER_A3_REG

- Name: TX_USER_A3_REG
- Address Offset: 0x1C
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	T_USER_A3_DATA	RW	SPDIF_OUT channel A user data bit [127:96]

6.3.2.9 TX_USER_A4_REG

- Name: TX_USER_A4_REG
- Address Offset: 0x20
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	T_USER_A4_DATA	RW	SPDIF_OUT channel A user data bit [159:128]

6.3.2.10 TX_USER_A5_REG

- Name: TX_USER_A5_REG
- Address Offset: 0x24
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	T_USER_A5_DATA	RW	SPDIF_OUT channel A user data bit [191:160]

6.3.2.11 TX_FIFO_DR

- Name: TX_FIFO_DR
- Address Offset: 0x28
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	TF_D	RW	SPDIF_OUT FIFO write data register, can only be written when SPDIFEN = 1.

6.3.2.12 TX_FIFO_TH

- Name: TX_FIFO_TH
- Address Offset: 0x2C
- Reset Value: 0x0000_0008

Bits	Name	Access	Description
31:4	RESERVED	RO	Reserved
3:0	TF_TH	R/W	TX FIFO threshold The configuration range is 0-15 and the default value is 8.

6.3.2.13 TX_FIFO_DL

- Name: TX_FIFO_DL
- Address Offset: 0x30
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:5	RESERVED	RO	Reserved
4:0	TF_DL	RO	TX FIFO current data level

6.3.2.14 TX_DMA_EN

- Name: TX_DMA_EN
- Address Offset: 0x34
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:1	RESERVED	RO	Reserved
0	TDMA_EN	RW	SPDIF OUT DMA handshake signal enable 0x0: Disabled 0x1: Enabled

6.3.2.15 TX_DMA_TH

- Name: TX_DMA_TH

- Address Offset: 0x38
- Reset Value: 0x0000_0008

Bits	Name	Access	Description
31:4	RESERVED	RO	Reserved
3:0	TDMA_TH	RW	PDM all FIFO DMA threshold configuration register When data in FIFO is greater than or equal to the threshold, a threshold full interrupt will be generated. The configuration range is 0-15 and the default value is 8.

6.3.2.16 SPDIF_SR

- Name: SPDIF_SR
- Address Offset: 0x3C
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:8	RESERVED	RO	Reserved
7	RX_CHNUM	RO	Number of SPDIF-IN channels 0: Dual channel, valid bit = 0 detected. 1: Mono, at least one valid bit = 1 detected.
6	RF_F	RO	RX FIFO full 0: RX FIFO is not full. 1: RX FIFO is full.
5	RF_NE	RO	RX FIFO not empty 0: RX FIFO is empty. 1: RX FIFO is not empty.
4	RX_BUSY	RO	SPDIF IN busy 0x0: Idle 0x1: Busy
3	Reserved	RO	Reserved
2	TF_E	RO	TX FIFO empty 0: TX FIFO is not empty. 1: TX FIFO is empty.
1	TF_NF	RO	TX FIFO not full 0: TX FIFO is full.

Bits	Name	Access	Description
			1: TX FIFO is not full.
0	TX_BUSY	RO	SPDIF OUT busy 0x0: Idle 0x1: Busy

6.3.2.17 SPDIF_IMR

- Name: SPDIF_IMR
- Address Offset: 0x40
- Reset Value: 0x0000_3770

Bits	Name	Access	Description
31:14	RESERVED	RO	Reserved
13	SPDIF_RPB_EM	R/W	RX header code detection error mask 0: spdif_rpb_err error is masked. 1: spdif_rpb_err error is not masked.
12	SPDIF_RCLK_EM	R/W	RX channel information change interrupt mask 0: spdif_rcs_intr interrupt is masked. 1: spdif_rcs_intr interrupt is not masked.
11	SPDIF_RPC_EM	R/W	RX even parity error mask 0: spdif_rp_err error is masked. 1: spdif_rp_err error is not masked.
10	SPDIF_RF_TF_IM	R/W	RX FIFO T threshold full interrupt mask 0: spdif_rftf_intr interrupt is masked. 1: spdif_rftf_intr interrupt is not masked.
9	SPDIF_RF_O_EM	RO	RX FIFO T overflow error mask 0: spdif_rfo_err error is masked. 1: spdif_rfo_err error is not masked.
8	SPDIF_RF_U_EM	R/W	RX FIFO T underflow error mask 0: spdif_rfu_err error is masked. 1: spdif_rfu_err error is not masked.
7	SPDIF_TX_DONE_IM	R/W	TX done and FIFO no data interrupt mask 0: spdif_tx_done_intr interrupt is masked. 1: spdif_tx_done_intr interrupt is not masked.
6	SPDIF_TF_TE_IM	R/W	TX FIFO threshold empty interrupt mask

Bits	Name	Access	Description
			0: spdif_tfte_intr interrupt is masked. 1: spdif_tfte_intr interrupt is not masked.
5	SPDIF_TF_U_EM	R/W	TX FIFO underflow error mask 0: spdif_tfu_err error is masked. 1: spdif_tfu_err error is not masked.
4	SPDIF_TF_O_EM	R/W	TX FIFO overflow error mask 0: spdif_tfo_err error is masked. 1: spdif_tfo_err error is not masked.
3:2	Reserved	RO	Reserved
1	SPDIF_ACCESS_EM	R/W	SPDIF access error mask 0: spdif_access_err error is masked. 1: spdif_access_err error is not masked.
0	SPDIF_WADDR_EM	R/W	SPDIF access address error mask 0: spdif_waddr_err error is masked. 1: spdif_waddr_err error is not masked.

6.3.2.18 SPDIF_ISR

- Name: SPDIF_ISR
- Address Offset: 0x44
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:14	RESERVED	RO	Reserved
13	SPDIF_RPB_ES	RO	RX header code detection error status 0: spdif_rpb_err error = 0 1: spdif_rpb_err error = 1
12	SPDIF_RCLK_ES	RO	RX channel information change interrupt status 0 - spdif_rcs_intr interrupt = 0 1 - spdif_rcs_intr interrupt = 1
11	SPDIF_RPC_ES	RO	RX even parity error status 0: spdif_rp_err error = 0 1: spdif_rp_err error = 1
10	SPDIF_RF_TF_IS	RO	RX FIFO T threshold full interrupt status 0: spdif_rftf_intr interrupt = 0

Bits	Name	Access	Description
			1: spdif_rftf_intr interrupt = 1
9	SPDIF_RF_O_ES	RO	RX FIFO T overflow error status 0: spdif_rfo_err error = 0 1: spdif_rfo_err error = 1
8	SPDIF_RF_U_ES	RO	RX FIFO T underflow error status 0: spdif_rfu_err error = 0 1: spdif_rfu_err error = 1
7	SPDIF_TX_DONE_IS	RO	TX done and FIFO no data interrupt 0: spdif_tx_done_intr interrupt = 0 1: spdif_tx_done_intr interrupt = 1
6	SPDIF_TF_TE_IS	RO	TX FIFO threshold empty interrupt status 0: spdif_tfte_intr interrupt = 0 1: spdif_tfte_intr interrupt = 1
5	SPDIF_TF_U_ES	RO	TX FIFO underflow error status 0: spdif_tfu_err error = 0 1: spdif_tfu_err error = 1
4	SPDIF_TF_O_ES	RO	TX FIFO overflow error status 0: spdif_tfo_err error = 0 1: spdif_tfo_err error = 1
3:2	Reserved	RO	Reserved
1	SPDIF_ACCESS_ES	RO	SPDIF access error status 0: spdif_access_err error = 0 1: spdif_access_err error = 1
0	SPDIF_WADDR_ES	RO	SPDIF access address error status 0: spdif_waddr_err error = 0 1: spdif_waddr_err error = 1

6.3.2.19 SPDIF_RISR

- Name: SPDIF_RISR
- Address Offset: 0x48
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:14	RESERVED	RO	Reserved

Bits	Name	Access	Description
13	SPDIF_RPB_RES	RO	RX header code detection raw error status 0: spdif_rpb_err RAW error = 0 1: spdif_rpb_err RAW error = 1
12	SPDIF_RCLK_RES	RO	RX channel information change raw interrupt status 0: spdif_rcs_intr RAW interrupt = 0 1: spdif_rcs_intr RAW interrupt = 1
11	SPDIF_RPC_RES	RO	RX even parity RAW error status 0: spdif_rp_err RAW error = 0 1: spdif_rp_err RAW error = 1
10	SPDIF_RF_TF_RIS	RO	RX FIFO T threshold full RAW interrupt status 0: spdif_rftf_intr RAW interrupt = 0 1: spdif_rftf_intr RAW interrupt = 1
9	SPDIF_RF_O_RES	RO	RX FIFO T overflow RAW error status 0: spdif_rfo_err RAW error = 0 1: spdif_rfo_err RAW error = 1
8	SPDIF_RF_U_RES	RO	RX FIFO T underflow RAW error status 0: spdif_rfu_err RAW error = 0 1: spdif_rfu_err RAW error = 1
7	SPDIF_TX_DONE_RIS	RO	TX done and FIFO no data RAW interrupt 0: spdif_tx_done_intr RAW interrupt = 0 1: spdif_tx_done_intr RAW interrupt = 1
6	SPDIF_TF_TE_RIS	RO	TX FIFO threshold empty RAW interrupt status 0: spdif_tfte_intr RAW interrupt = 0 1: spdif_tfte_intr RAW interrupt = 1
5	SPDIF_TF_U_RES	RO	TX FIFO underflow RAW error status 0: spdif_tfu_err RAW error = 0 1: spdif_tfu_err RAW error = 1
4	SPDIF_TF_O_RES	RO	TX FIFO overflow RAW error status 0: spdif_tfo_err RAW error = 0 1: spdif_tfo_err RAW error = 1
3:2	Reserved	RO	Reserved
1	SPDIF_ACCESS_RES	RO	SPDIF access RAW error status 0: spdif_access_err RAW error = 0

Bits	Name	Access	Description
			1: spdif_access_err RAW error = 1
0	SPDIF_WADDR_RES	RO	SPDIF access address RAW error status 0: spdif_waddr_err RAW error = 0 1: spdif_waddr_err RAW error = 1

6.3.2.20 SPDIF_ICR

- Name: SPDIF_ISR
- Address Offset: 0x4C
- Reset Value:0x0000_0000

Bits	Name	Access	Description
31:14	RESERVED	WO	Reserved
13	SPDIF_RPB_EC	WO	Write 1 clear RX header code detection error
12	SPDIF_RCLK_EC	WO	Write 1 clear RX channel information change interrupt
11	SPDIF_RPC_EC	WO	Write 1 clear RX even parity error
10	SPDIF_RF_TF_IC	WO	Write 1 clear RX FIFO T threshold full interrupt
9	SPDIF_RF_O_EC	WO	Write 1 clear RX FIFO T overflow error
8	SPDIF_RF_U_EC	WO	Write 1 clear RX FIFO T underflow error
7	SPDIF_TX_DONE_IC	WO	Write 1 clear TX done and FIFO no data interrupt
6	SPDIF_TF_TE_IC	WO	Write 1 clear TX FIFO threshold empty interrupt
5	SPDIF_TF_U_EC	WO	Write 1 clear TX FIFO underflow error
4	SPDIF_TF_O_EC	WO	Write 1 clear TX FIFO overflow error
3:2	Reserved	WO	Reserved
1	SPDIF_ACCESS_EC	WO	Write 1 clear SPDIF access error
0	SPDIF_WADDR_EC	WO	Write 1 clear SPDIF access address error

6.3.2.21 RX_EN_REG

- Name: RX_EN_REG
- Address Offset: 0x50
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:1	RESERVED	RO	Reserved

Bits	Name	Access	Description
0	RXEN	WO	SPDIF-IN enable 0x0: SPDIF-IN is disabled. 0x1: SPDIF-IN is enabled.

6.3.2.22 RX_CTL_REG

- Name: RX_CTL_REG
- Address Offset: 0x54
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:20	Reserved	RO	Reserved
19:13	RX_DIV	RW	SPDIF-IN divider configuration. Divide spdif_source_clk to generate spdif_rx_clk. Divider value = (RX_DIV + 1)*2
12	RX_DIV_BYPASS	RW	SPDIF-IN divider bypass 0x0: Bypass 0x1: Divider used
11:9	Reserved	RO	Reserved
8	RX_VALID_EN	RW	SPDIF-IN validity bit 0: When the validity bit is 1, no data is received. 1: All data is received.
7:5	Reserved	RO	Reserved
4	RX_PARITY_EN	RW	SPDIF-IN parity bit enable 0: Even parity is disabled. 1: Even parity is enabled.
3:2	Reserved	RO	Reserved
1:0	RX_DATAMODE	RW	SPDIF-IN data width select 0x0: 24-bit 0x1: 20-bit 0x2,0x3: 16-bit

6.3.2.23 RX_CS_REG

- Name: RX_CS_REG
- Address Offset: 0x58

- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	R_CS	RO	SPDIF-IN channel status

6.3.2.24 RX_USER_A0_REG

- Name: RX_USER_A0_REG
- Address Offset: 0x5C
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	R_USER_A0_DATA	RO	SPDIF_IN channel A user data bit [31:0]

6.3.2.25 RX_USER_A1_REG

- Name: RX_USER_A1_REG
- Address Offset: 0x60
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	R_USER_A1_DATA	RO	SPDIF_IN channel A user data bit [63:32]

6.3.2.26 RX_USER_A2_REG

- Name: RX_USER_A2_REG
- Address Offset: 0x64
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	R_USER_A2_DATA	RO	SPDIF_IN channel A user data bit [95:64]

6.3.2.27 RX_USER_A3_REG

- Name: RX_USER_A3_REG
- Address Offset: 0x68
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	R_USER_A3_DATA	RO	SPDIF_IN channel A user data bit [127:96]

6.3.2.28 RX_USER_A4_REG

- Name: RX_USER_A4_REG

- Address Offset: 0x6C
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	T_USER_A4_DATA	RO	SPDIF_IN channel A user data bit [159:128]

6.3.2.29 RX_USER_A5_REG

- Name: RX_USER_A5_REG
- Address Offset: 0x70
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	R_USER_A5_DATA	RO	SPDIF_IN channel A user data bit [191:160]

6.3.2.30 RX_FIFO_DR

- Name: RX_FIFO_DR
- Address Offset: 0x74
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	RF_D	RO	SPDIF_IN FIFO read data register, can only be written when SPDIFEN = 1.

6.3.2.31 RX_FIFO_TH

- Name: RX_FIFO_TH
- Address Offset: 0x78
- Reset Value: 0x0000_0008

Bits	Name	Access	Description
31:4	RESERVED	RO	Reserved
3:0	RF_TH	R/W	RX FIFO threshold The configuration range is 1-15. When set to 0, the threshold is16. The default value is 8.

6.3.2.32 RX_FIFO_DL

- Name: RX_FIFO_DL
- Address Offset: 0x7C
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:5	RESERVED	RO	Reserved
4:0	RF_DL	RO	RX FIFO current data level

6.3.2.33 RX_DMA_EN

- Name: RX_DMA_EN
- Address Offset: 0x80
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:1	RESERVED	RO	Reserved
0	RDMA_EN	RW	SPDIF IN DMA handshake signal enable 0x0: Disabled 0x1: Enabled

6.3.2.34 RX_DMA_TH

- Name: RX_DMA_TH
- Address Offset: 0x84
- Reset Value: 0x0000_0008

Bits	Name	Access	Description
31:4	RESERVED	RO	Reserved
3:0	RDMA_TH	RW	SPDIF IN FIFO DMA threshold configuration register When data in FIFO is greater than or equal to the threshold, a threshold full interrupt will be generated. The configuration range is 1-15. When set to 0, the threshold is 16. The default value is 8.

6.3.2.35 TX_CS_B_REG

- Name: TX_CS_B_REG
- Address Offset: 0x88
- Reset Value: 0x0100_0000

Bits	Name	Access	Description
31:30	RESERVED	RO	Reserved
29:28	T_B_CLK_ACC	RW	SPDIF-OUT channel B clock accuracy, refer to IEC60958.
27:24	T_B_FS_SEL	RW	SPDIF-OUT channel B sampling rate

Bits	Name	Access	Description
			0011: 32kHz 0000: 44.1kHz 0010: 48kHz 1000: 88.2kHz 1010: 96kHz 1110: 192kHz 0001: Not indicated (default) Other: Reserved
23:20	T_B_CH_NUM	RW	Number of SPDIF-OUT channel B channels, refer to IEC60958.
19:16	T_B_SRC_NUM	RW	Number of SPDIF-OUT channel B sources, refer to IEC60958.
15:8	T_B_CC_SEL	RW	SPDIF-OUT channel B type code, refer to IEC60958.
7:6	T_B_MODE	RW	SPDIF-OUT channel B mode, refer to IEC60958.
5:4	Reserved	RO	Reserved
3	T_B_EMP_MODE	RW	SPDIF-OUT channel B emphasis mode 0: Not pre-emphasis 1: Pre-emphasis
2	T_B_COPY	RW	SPDIF-OUT channel B copyright 0: Prohibited 1: Copyright licensed
1	T_B_AUIDO_EN	RW	SPDIF-OUT channel B signal type 0: Not audio 1: Audio

6.3.2.36 TX_USER_B0_REG

- Name: TX_USER_B0_REG
- Address Offset: 0x8C
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	T_USER_B0_DATA	RW	SPDIF_OUT channel B user data bit [31:0]

6.3.2.37 TX_USER_B1_REG

- Name: TX_USER_B1_REG

- Address Offset: 0x90
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	T_USER_B1_DATA	RW	SPDIF_OUT channel B user data bit [63:32]

6.3.2.38 TX_USER_B2_REG

- Name: TX_USER_B2_REG
- Address Offset: 0x94
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	T_USER_B2_DATA	RW	SPDIF_OUT channel B user data bit [95:64]

6.3.2.39 TX_USER_B3_REG

- Name: TX_USER_B3_REG
- Address Offset: 0x98
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	T_USER_B3_DATA	RW	SPDIF_OUT channel B user data bit [127:96]

6.3.2.40 TX_USER_B4_REG

- Name: TX_USER_B4_REG
- Address Offset: 0x9C
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	T_USER_B4_DATA	RW	SPDIF_OUT channel B user data bit [159:128]

6.3.2.41 TX_USER_B5_REG

- Name: TX_USER_B5_REG
- Address Offset: 0xa0
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	T_USER_B5_DATA	RW	SPDIF_OUT channel B user data bit [191:160]

6.3.2.42 RX_CS_REG

- Name: RX_CS_REG
- Address Offset: 0xa4
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	R_CS	RO	SPDIF-IN channel status

6.3.2.43 RX_USER_B0_REG

- Name: RX_USER_B0_REG
- Address Offset: 0xa8
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	R_USER_B0_DATA	RO	SPDIF_IN channel B user data bit [31:0]

6.3.2.44 RX_USER_B1_REG

- Name: TX RX USER_B1_REG
- Address Offset: 0xac
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	R_USER_B1_DATA	RO	SPDIF_IN channel B user data bit [63:32]

6.3.2.45 RX_USER_B2_REG

- Name: RX_USER_B2_REG
- Address Offset: 0xd0
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	R_USER_B2_DATA	RO	SPDIF_IN channel B user data bit [95:64]

6.3.2.46 RX_USER_B3_REG

- Name: RX_USER_B3_REG
- Address Offset: 0xb4
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	R_USER_B3_DATA	RO	SPDIF_IN channel B user data bit [127:96]

6.3.2.47 RX_USER_B4_REG

- Name: RX_USER_B4_REG
- Address Offset: 0xb8
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	T_USER_B4_DATA	RO	SPDIF_IN channel B user data bit [159:128]

6.3.2.48 RX_USER_B5_REG

- Name: RX_USER_B5_REG
- Address Offset: 0xbc
- Reset Value: 0x0000_0000

Bits	Name	Access	Description
31:0	R_USER_B5_DATA	RO	SPDIF_IN channel B user data bit [191:160]